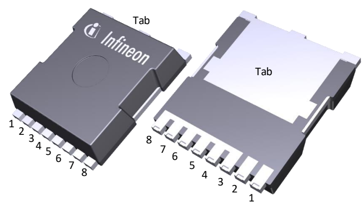
MOSFET

600V CoolMOS™ SJ Power Device

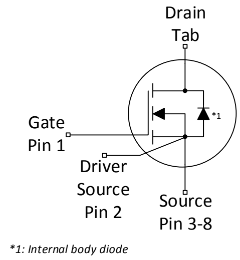
The C7 GOLD series (G7) for the first time brings together the benefits of the C7 GOLD CoolMOS™ technology, 4 pin Kelvin Source capability and the improved thermal properties of the TOLL package to enable a possible SMD solution for high current topologies such as PFC up to 3kW

TOLL



Features

- C7 Gold gives best in class FOM $R_{DS(on)}$*E_{oss} and $R_{DS(on)}$*Q_g.
- Suitable for hard and soft switching (PFC and high performance LLC)
- C7 Gold technology enables best in class $R_{DS(on)}$ in smallest footprint.
- TOLL package has inbuilt 4th pin Kelvin Source configuration and low parasitic source inductance (~1nH).
- TOLL package is MSL1 compliant, total Pb-free and has easy visual inspection grooved leads.
- TOLL SMD package combined with lead free die attach process enables improved thermal performance R_{th}.



Benefits

- C7 Gold FOM $R_{DS(on)}$*Q_g is 15% better than previous C7 600V enabling faster switching leading to higher efficiency.
- Increased economies of scale by use in PFC and PWM topologies in the application
- C7 Gold can reach 28mΩ in in TOLL 115mm^2 footprint, whereas previous BIC C7 600V was 40mΩ in 150mm^2 D^{2}PAK footprint.
- Reducing parasitic source inductance by Kelvin Source improves efficiency by faster switching and ease of use due to less ringing.
- TOLL package is easy to use and has the highest quality standards.
- Improved thermals enable SMD TOLL package to be used in higher current designs than has been previously possible.

Potential applications

PFC stages and PWM stages (TTF, LLC) for high power/performance SMPS e.g. Computing, Server, Telecom, UPS and Solar.

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	125	mΩ
$Q_{g.typ}$	27	nC
$I_{D,pulse}$	54	A
$I_{D,continuous}$ @ T_j<150°C	27	A
E_{oss}@400V	3.27	µJ
Body diode di/dt	720	A/µs

Part number	Package	Marking	Related links
IPT60R125G7	PG-HSOF-8	60R125G7	see Appendix A

Table of contents

1 Maximum ratings

at Tî = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	20	A	T_C=25°C
				12		T_C=100°C
Pulsed drain current [2]	$I_{D,pulse}$	-	-	54	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	64	mJ	I_D=3.8A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}			0.32		
Avalanche current, single pulse	I_{AS}	-	-	3.8	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	120	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55		150	°C	
Mounting torque	-	-		n.a.	Ncm	
Continuous diode forward current	I_S	-	-	20	A	T_C=25°C
Diode pulse current [2]	$I_{S,pulse}$			54		
Reverse diode dv/dt [3]	dv/dt	-	-	25	V/ns	V_{DS}=0...400V, I_{SD}≤5.9A, T_j=25°C see table 8
Maximum diode commutation speed	di_f/dt			720	A/µs	
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

1) Limited by $T_{j\ max}$.
2) Pulse width t_p limited by $T_{j,max}$
3) Identical low side and high side switch

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.04	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm^2 (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at Tî=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	V_{DS}=V_{GS}, I_D=0.32mA
Zero gate voltage drain current	I_{DSS}	-	-	1	µA	V_{DS}=600, V_{GS}=0V, T_j=25°C
			10	-		V_{DS}=600, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.108	0.125	Ω	V_{GS}=10V, I_D=6.4A, T_j=25°C
			0.269	-		V_{GS}=10V, I_D=6.4A, T_j=150°C
Gate resistance	R_G	-	0.8	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1080	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}		22			
Effective output capacitance, energy related [4)]	$C_{o(er)}$	-	41	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related [5)]	$C_{o(tr)}$	-	420	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	18	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=6.4A, R_G =10Ω; see table 9
Rise time	t_r		5			
Turn-off delay time	$t_{d(off)}$		60			
Fall time	t_f		5			

4) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

5) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5	-	nC	V_{DD}=400V, I_D=6.4A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}		10		nC	
Gate charge total	Q_g		27		nC	
Gate plateau voltage	$V_{plateau}$		5.0		V	

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.8	-	V	V_{GS}=0V, I_F=6.4A, T_j=25°C
Reverse recovery time	t_{rr}	-	280	-	ns	V_R=400V, I_F=6.4A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}		2.8		µC	
Peak reverse recovery current	I_{rrm}		20		A	

4 Electrical characteristics diagrams

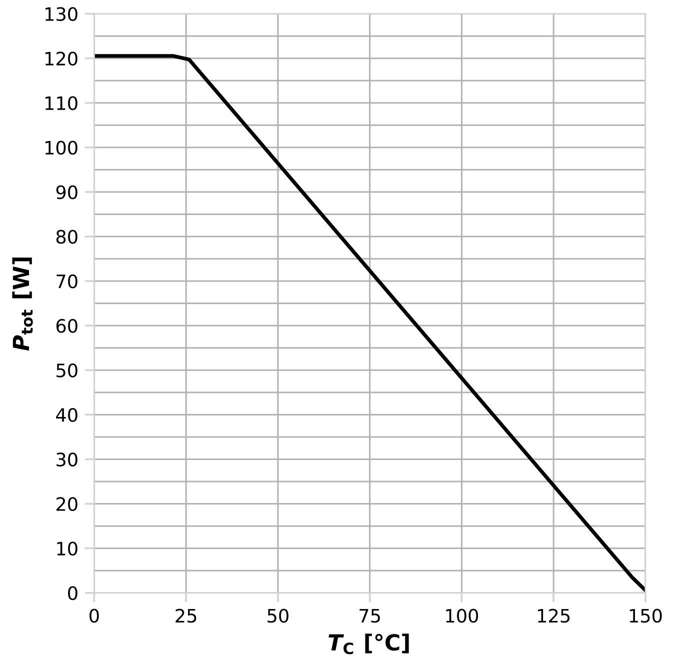
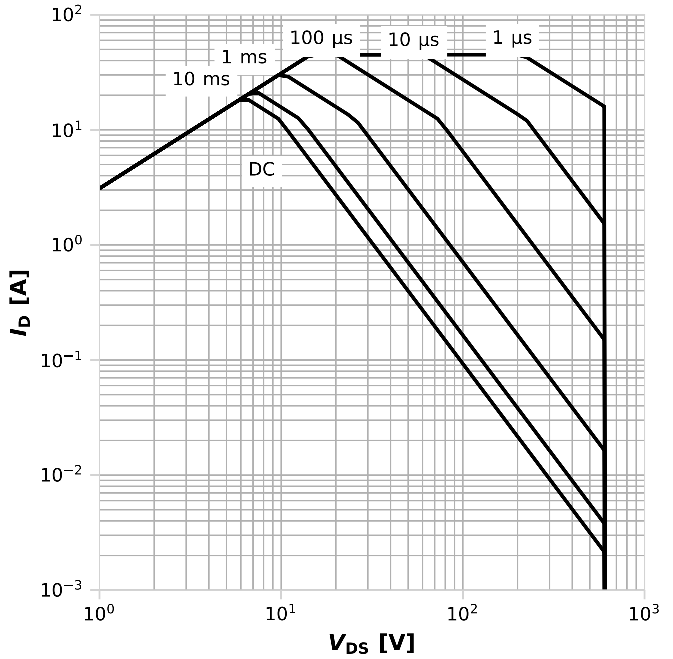
Diagram 1: Power dissipation	Diagram 2: Safe operating area
	
P_{tot}=f(T_C)	I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

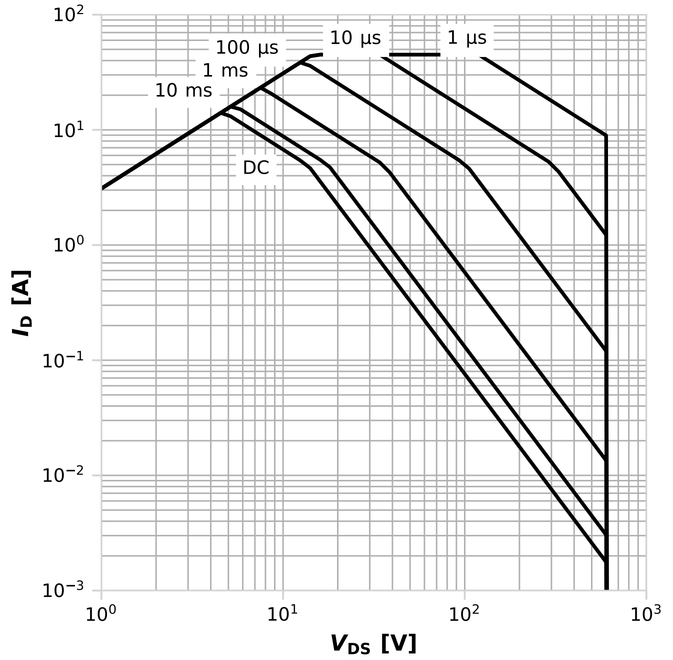
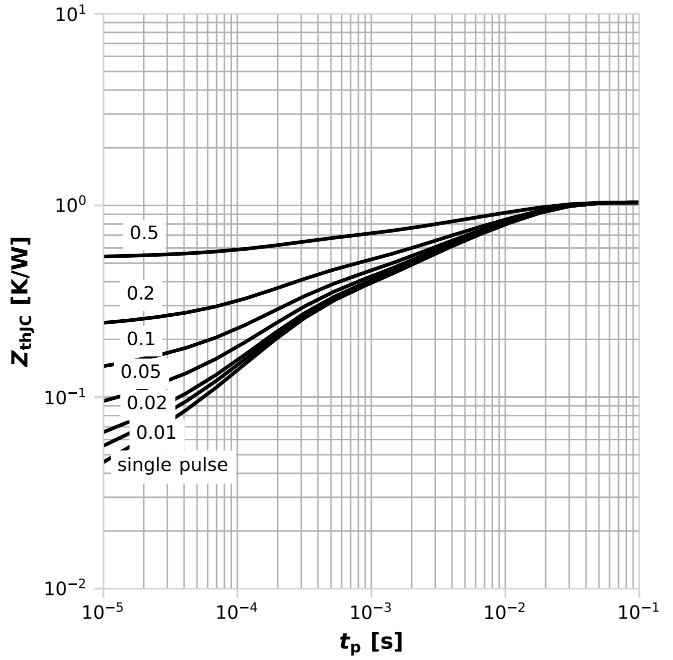
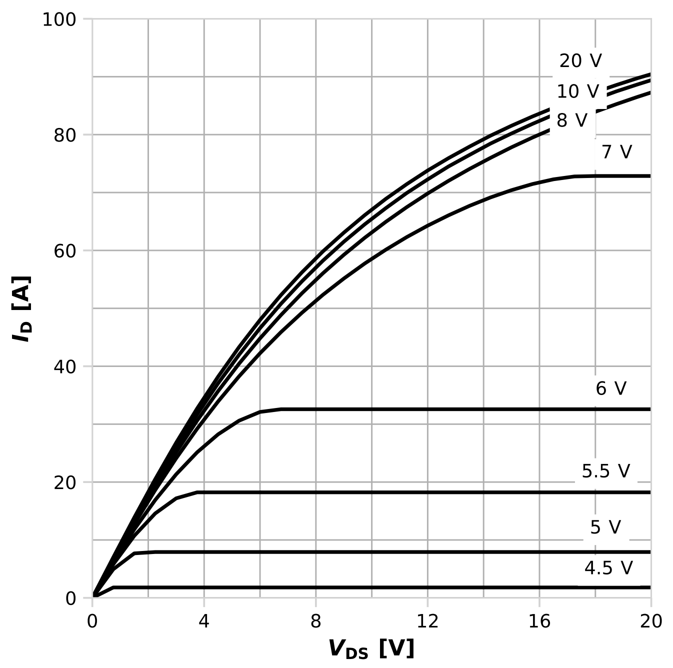
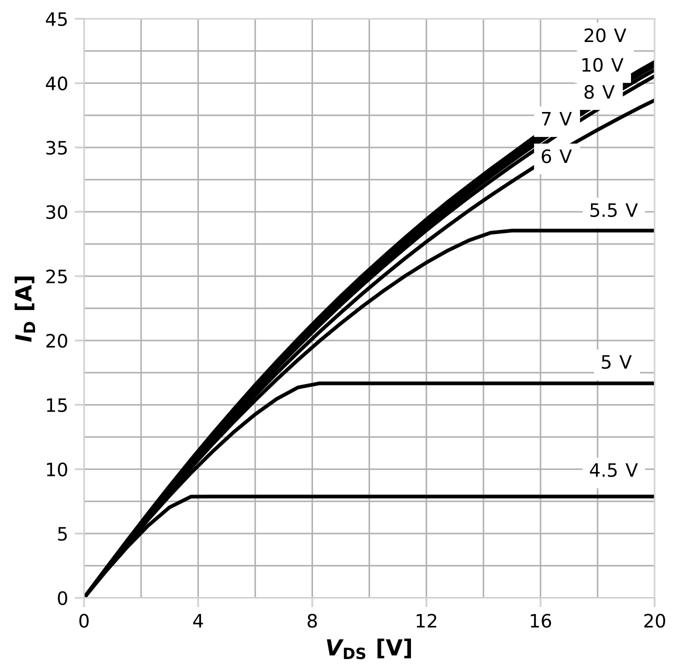
Diagram 3: Safe operating area	Diagram 4: Max. transient thermal impedance
	
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p	Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



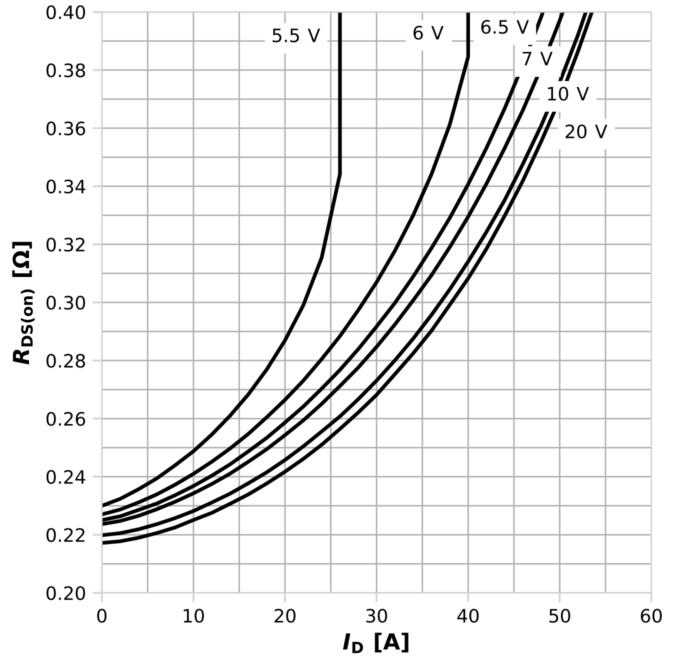
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



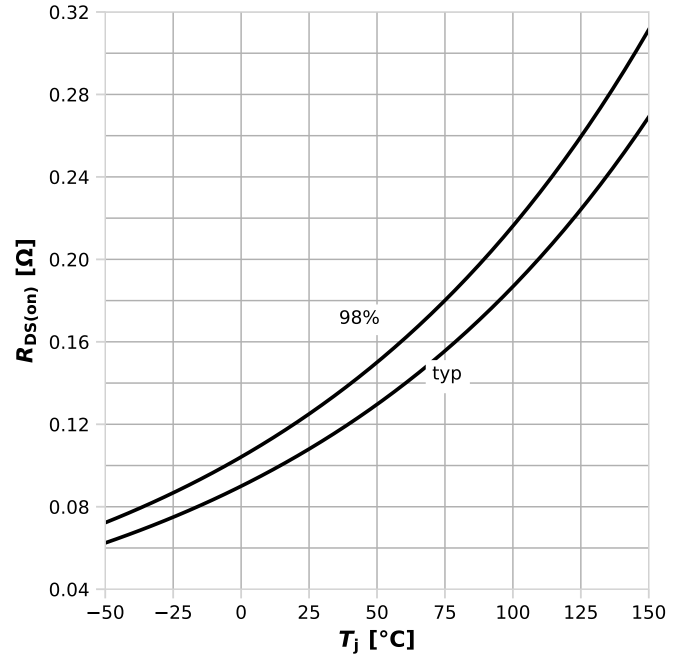
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



$R_{DS(on)}$=f(T_j); I_D=6.4 A; V_{GS}=10 V

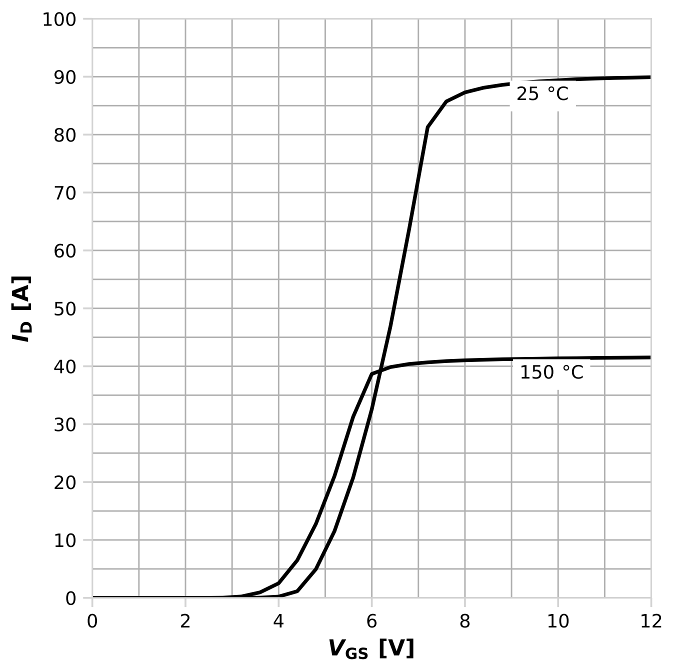
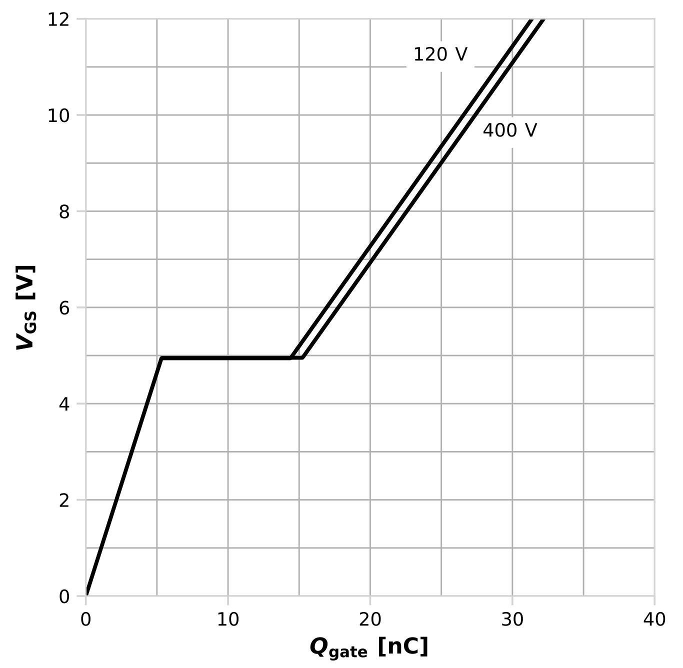
Diagram 9: Typ. transfer characteristics	Diagram 10: Typ. gate charge
	
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j	V_{GS}=f(Q_{gate}); I_D=6.4 A pulsed; parameter: V_{DD}

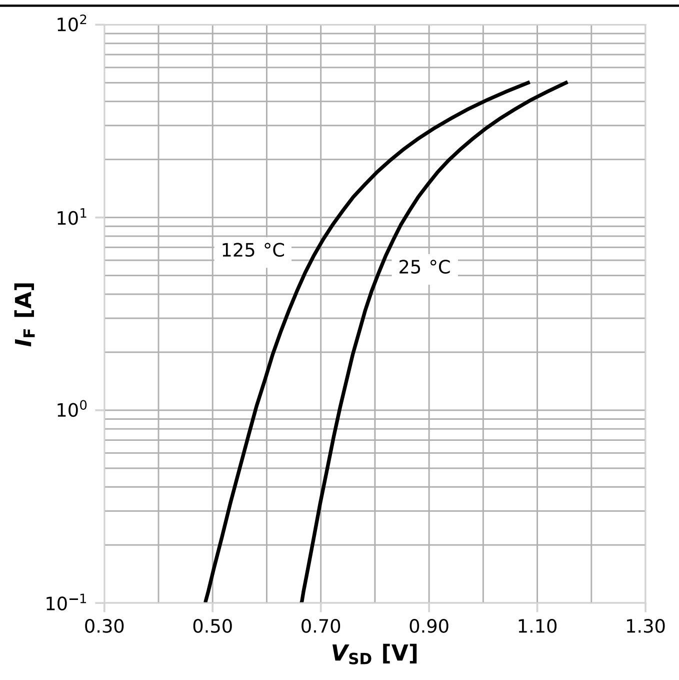
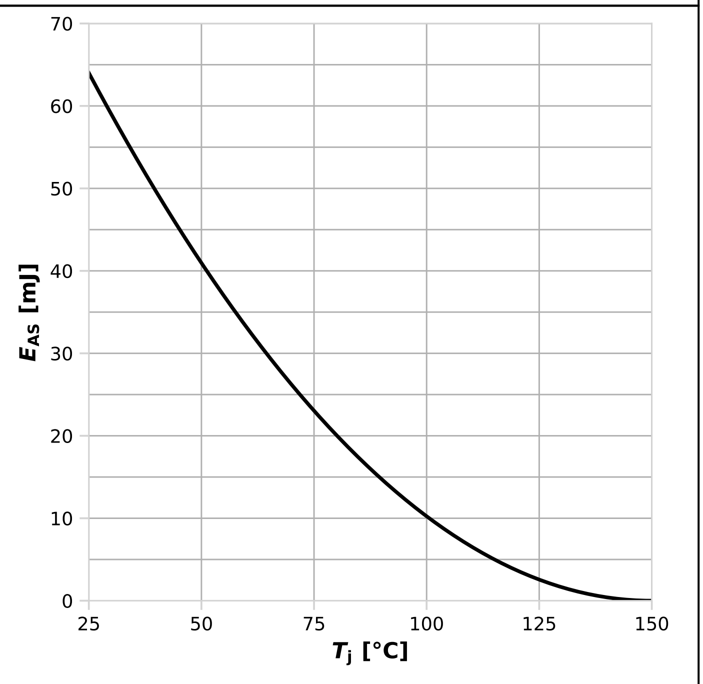
Diagram 11: Forward characteristics of reverse diode	Diagram 12: Avalanche energy
	
I_F=f(V_{SD}); parameter: T_j	E_{AS}=f(T_j); I_D=3.8 A; V_{DD}=50 V

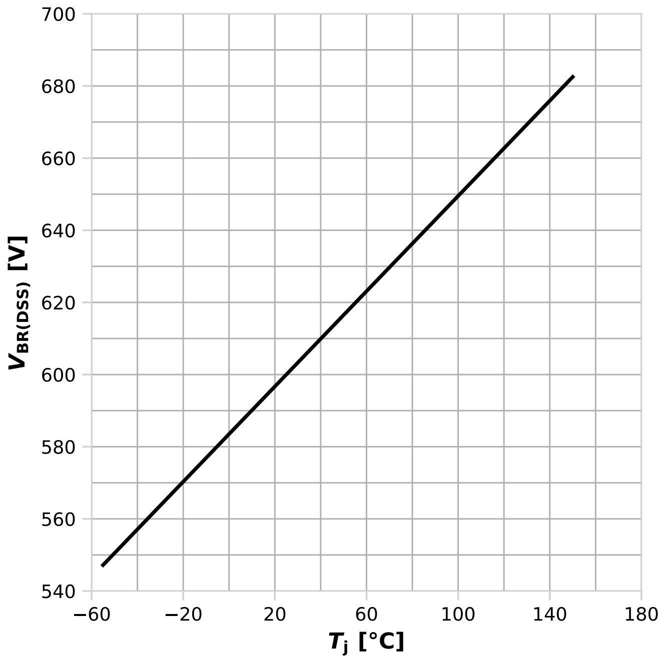
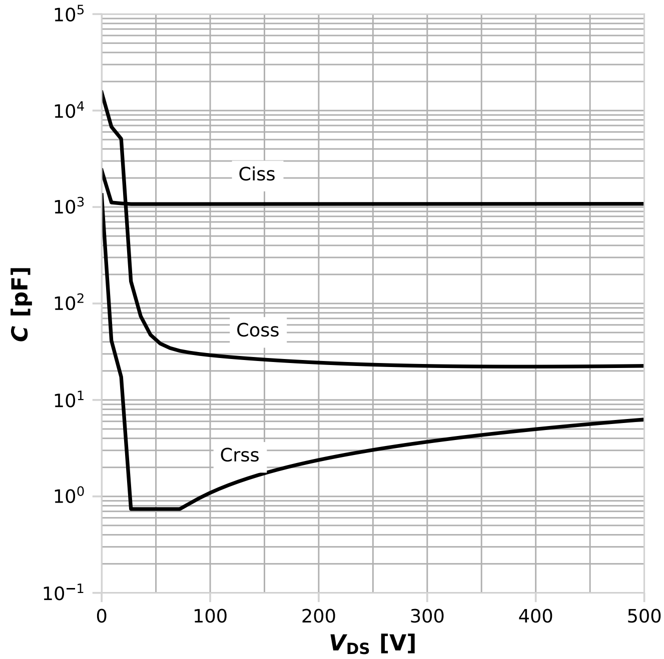
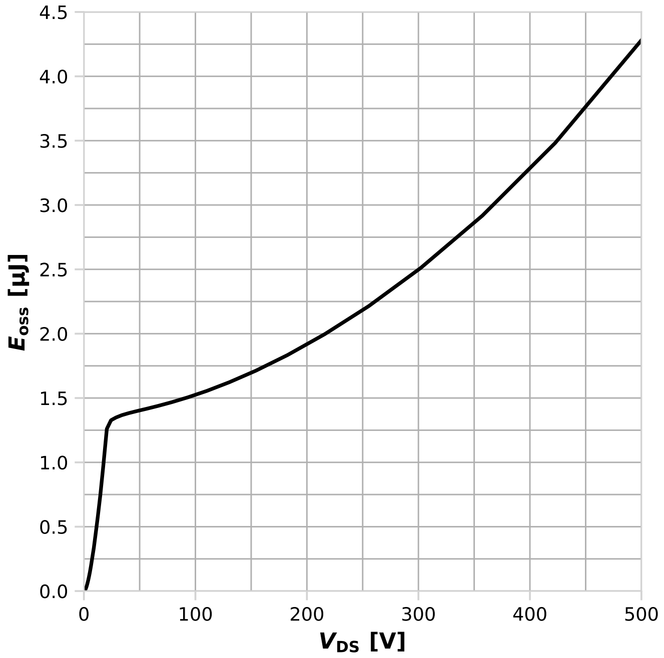
Diagram 13: Drain-source breakdown voltage	Diagram 14: Typ. capacitances
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy

E_{oss}=f(V_{DS})

5 Test circuits

Table 8 Diode characteristics

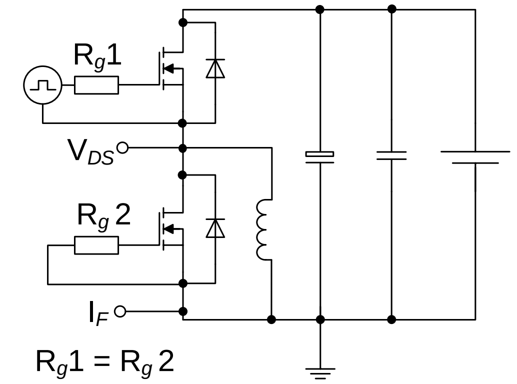
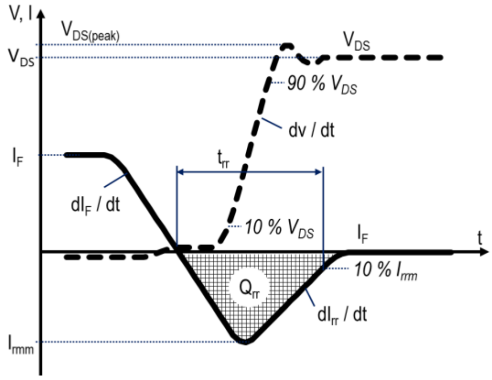
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times (ss)

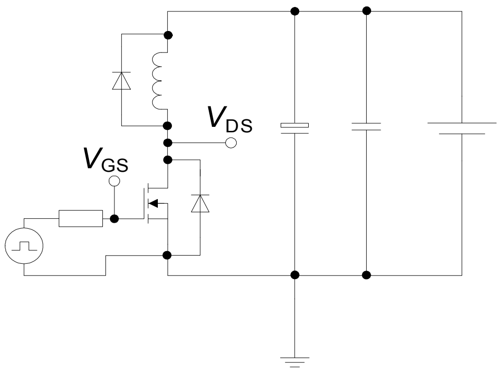
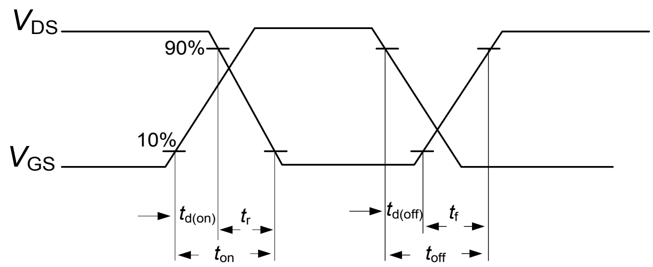
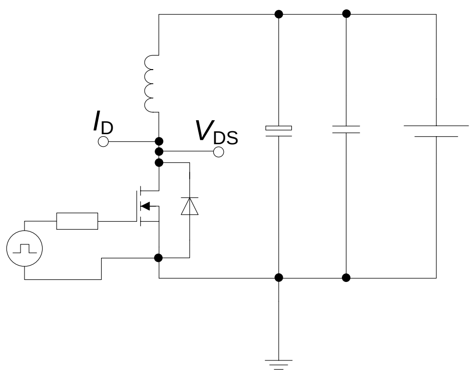
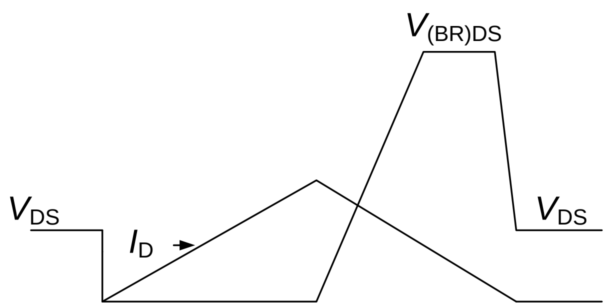
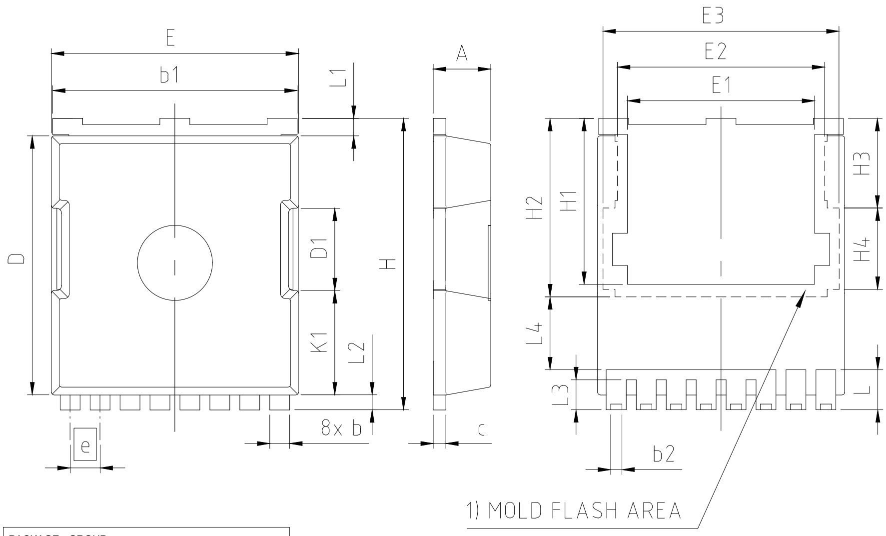
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load (ss)

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package outlines



PACKAGE - GROUP NUMBER:	PG-HSOF-8-U02	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D1	3.30	
E	9.70	10.10
E1	7.50	
E2	8.50	
E3	9.46	
e	1.20 (BSC)	
H	11.48	11.88
H1	6.55	6.95
H2	7.15	
H3	3.59	
H4	3.26	
N	8	
K1	4.18	
L	1.40	1.80
L1	0.50	0.90
L2	0.50	0.70
L3	1.00	1.30
L4	2.62	2.81

1) PARTIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm

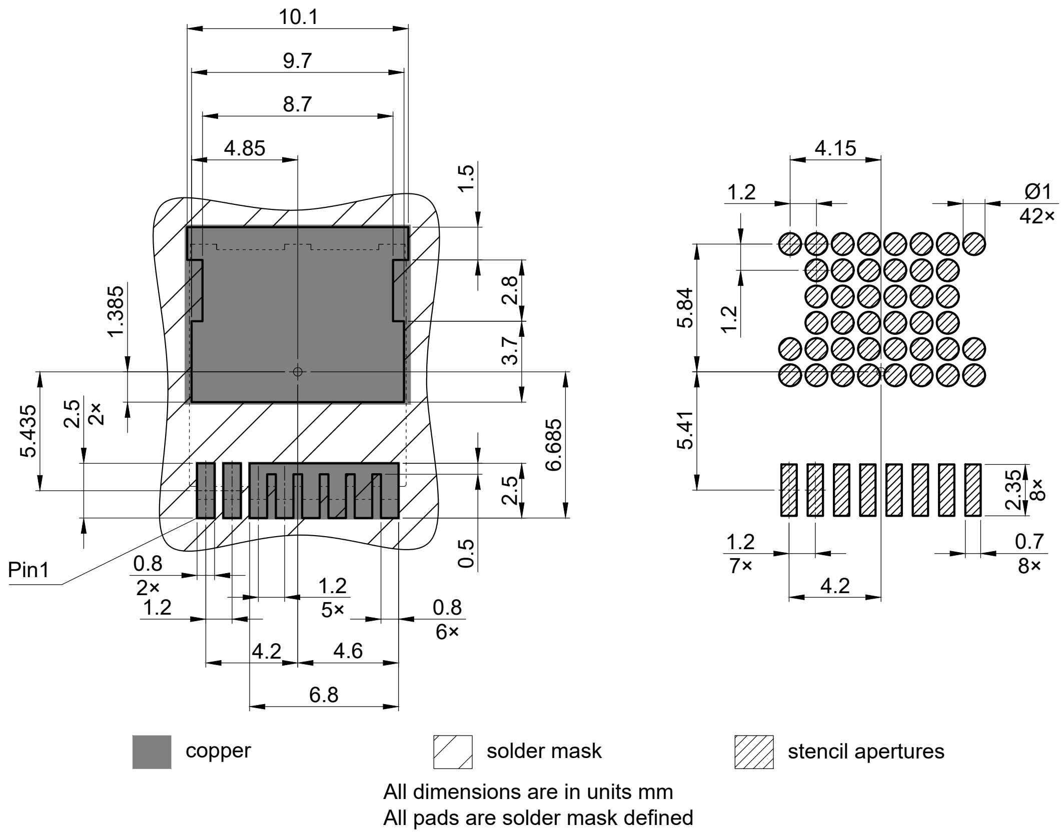


Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm

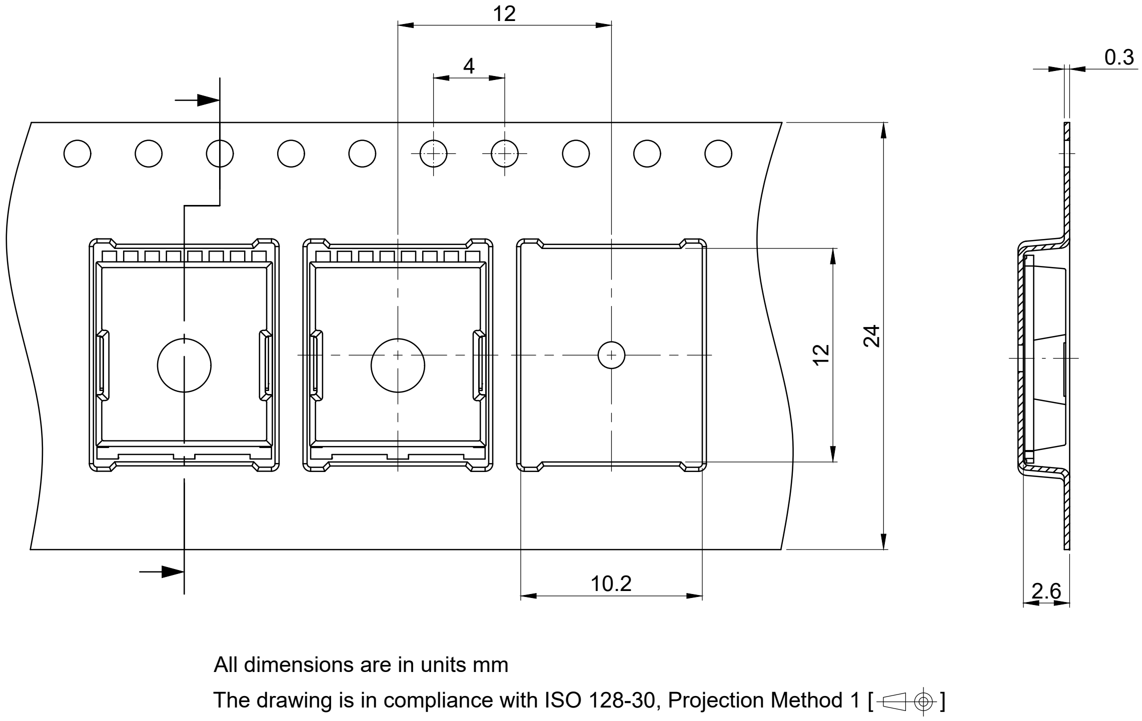


Figure 3 Packaging variant PG-HSOF-8, dimensions in mm

7 Appendix A

Table 11 Related links

- IFX CoolMOS™ G7 Webpage
- IFX CoolMOS™ G7 application note
- IFX CoolMOS™ G7 simulation model
- IFX Design tools

Revision history

IPT60R125G7

Revision 2025-02-03, Rev. 2.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2016-12-15	Release of final version
2.1	2020-10-28	Content update diagram 2,3,4,7,8 and format update
2.2	2025-02-03	Implementation of standardized Infineon Umbrella-Templates for package drawings. H1 Extension from 6.75 to 6.95 MAX

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