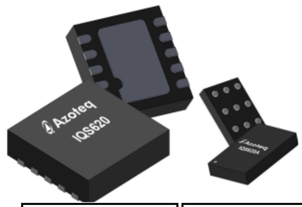
IQS620 / IQS620A Datasheet

Combination sensor with dual channel capacitive proximity/touch, Hall-effect sensor and inductive sensing

The IQS620(A) ProxFusion® IC is a multifunctional capacitive, Hall-effect & inductive sensor designed for applications where any or all of the technologies may be required. The IQS620(A) is an ultra-low power solution designed for short or long term activations through any of the sensing channels. The IQS620(A) is fully I²C compatible and can be configured to output main trigger events on GPIOs.

Features

- **Unique combination of sensing technologies:**
  - Capacitive sensing
  - Hall-effect sensing
  - Inductive sensing
- **Capacitive sensing**
  - Full auto-tuning with adjustable sensitivity
  - 2pF to 200pF external capacitive load capability
  - Enhanced temperature stability
- **Hall-effect sensing**
  - On-chip Hall-effect measurement plates
  - Dual direction Hall switch sensor UI
  - 2 level detection (widely variable)
  - Detection range 10mT – 200mT
- **Inductive sensing**
  - 2 level detection and hysteresis for inductive sensing
  - External sense coil required (PCB trace)
- **Multiple integrated UI** options based on years of experience in sensing on fixed and mobile platforms:
  - Proximity wake-up; Touch; SAR; Hysteresis
- **A**utomatic **T**uning **I**mplementation (**ATI**) – performance enhancement (10bit)
- Minimal external components
- Standard **I²C** interface
- Optional **RDY indication** for event mode operation
- **Low power consumption:**
  - 130uA (100Hz response, 1ch inductive)
  - 105uA (100Hz response, 2ch Hall)
  - 90uA (100Hz response, 3ch capacitive)
  - 75uA (100Hz response, 1ch cap. SAR)
  - 46uA (20Hz response, 1ch inductive)
  - 38uA (20Hz response, 2ch Hall)
  - 32uA (20Hz response, 3ch capacitive)
  - 27uA (20Hz response, 1ch cap. SAR)
  - 2.5uA (4Hz response, 1ch cap. wake-up)
- **Supply voltage:**
  - IQS620: 2.0V to 3.3V
  - IQS620A: 1.8V to 3.3V
- **Low profile packages:**
  - DFN(3x3) – 10 pin package
  - WLCSP – 9 pin package



DFN(3x3)-10 | WLCSP-9

Representations only, not actual marking

Applications

- Mobile electronics (phones/tablets)
- SAR safety requirements for laptops, tablets and phones
- Wearable devices
- White goods and appliances
- Human Interface Devices
- Proximity activated backlighting
- Applications with long-term activation
- Aftermarket automotive[1]

Available Packages			
T_A	DFN(3x3)-10		WLCSP-9
-20°C to +85°C	IQS620	IQS620A	IQS620A

[1] The part is not automotive qualified.

Table of Contents

List of abbreviations

AC	– Alternating Current
ACK	– I^2C Acknowledge condition
ATI	– Automatic Tuning Implementation
BOD	– Brown Out Detection
CS	– Sampling Capacitor
DSP	– Digital Signal Processing
ESD	– Electrostatic Discharge
FOSC	– Main Clock Frequency Oscillator
GND	– Ground
GPIO	– General Purpose Input Output
I^2C	– Inter-Integrated Circuit
IC	– Integrated Circuit
LP	– Low Power
LPOSC	– Low Power Oscillator
LTA	– Long Term Average
LTX	– Inductive Transmitting electrode
MCU	– Microcontroller unit
MSL	– Moisture Sensitive Level
MOV	– Movement
MOQ	– Minimum Order Quantity
NACK	– I^2C Not Acknowledge condition
NC	– Not Connect
NP	– Normal Power
OTP	– One Time Programmable
PMU	– Power Management Unit
POR	– Power On Reset
PWM	– Pulse Width Modulation
QRD	– Quick Release Detection
RDY	– Ready Interrupt Signal
RX	– Receiving electrode
SAR	– Specific Absorption Rate
SCL	– I^2C Clock
SDA	– I^2C Data
SR	– I^2C Slew rate
THR	– Threshold
UI	– User Interface
ULP	– Ultra Low Power

1 Introduction

1.1 ProxFusion®

The ProxFusion® sensor series provides all of the proven ProxSense® engine capabilities with additional sensors types. A combined sensor solution is available within a single platform.

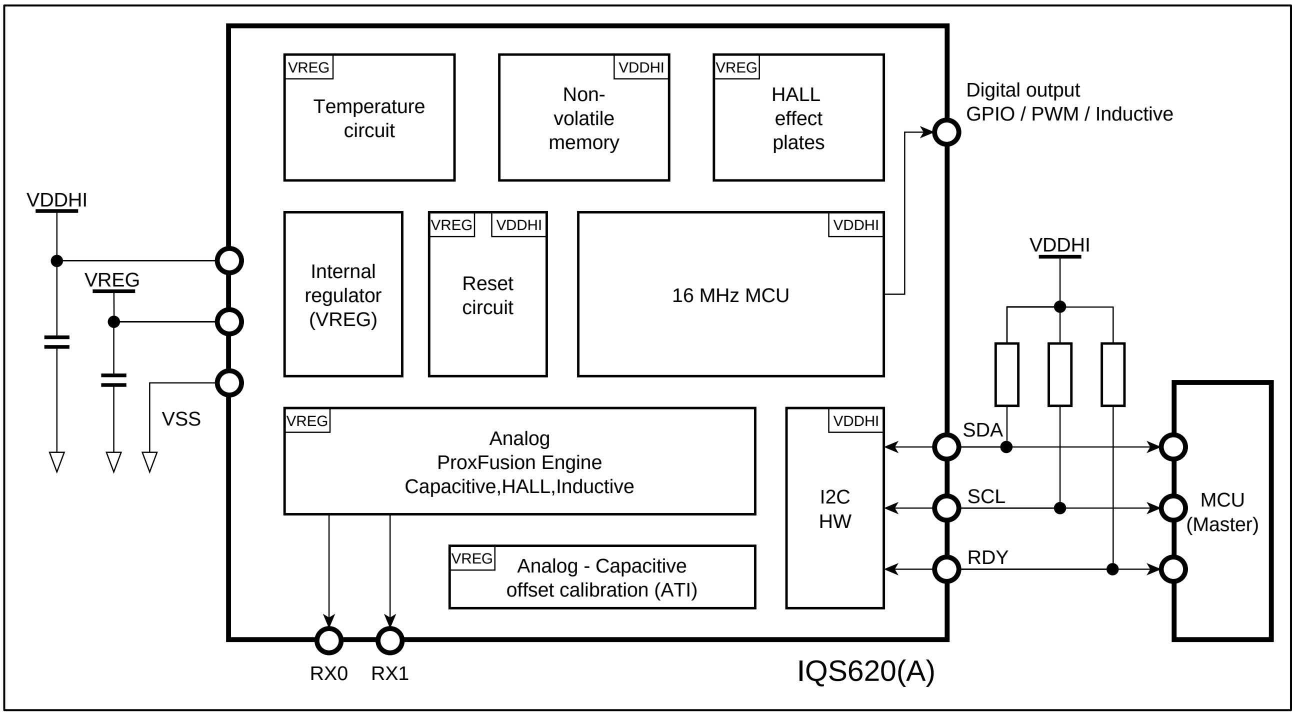


Figure 1.1 IQS620(A) functional block diagram

1.2 Packaging and Pin-Out

12.1.1 DFN(3x3)-10

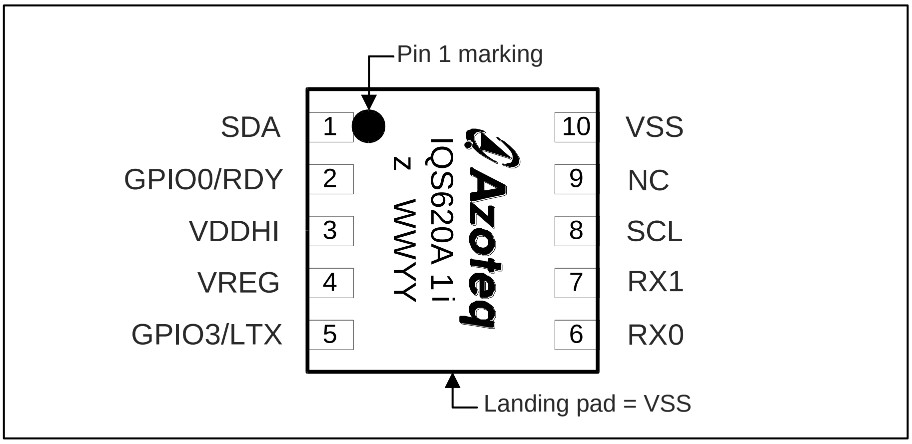


Figure 1.2 IQS620(A) pin-out (DFN(3x3)-10 package top view; markings may differ)

Table 1.1 DFN(3x3)-10 pin-out description

IQS620(A) in DFN(3x3)-10			
Pin	**Name**	**Type**	**Function**
1	SDA	Digital input / output	**SDA** (I^2C Data signal)
2	GPIO0 / RDY	Digital output Open drain active low logic	SAR activation output (higher priority) **RDY** (I^2C Ready interrupt signal; lower priority)
3	VDDHI	Supply input	Supply: IQS620: 2.0V – 3.3V IQS620A: 1.8V – 3.3V
4	VREG	Voltage regulator output	Regulates the system's internal voltage Requires external capacitors to ground
5	GPIO3 / LTX	Digital output / Analogue transmitter electrode	PWM signal output (higher priority) / Connect to inductive sensor's transmitting coil (lower priority)
6	RX0	Analogue receiving electrode	Connect to conductive area intended for sensor receiving
7	RX1	Analogue receiving electrode	Connect to conductive area intended for sensor receiving
8	SCL	Digital input / output	**SCL** (I^2C Clock signal)
9	NC	Not connect	Not connect
10	VSS	Supply input	Common ground reference

12.1.2 WLCSP-9

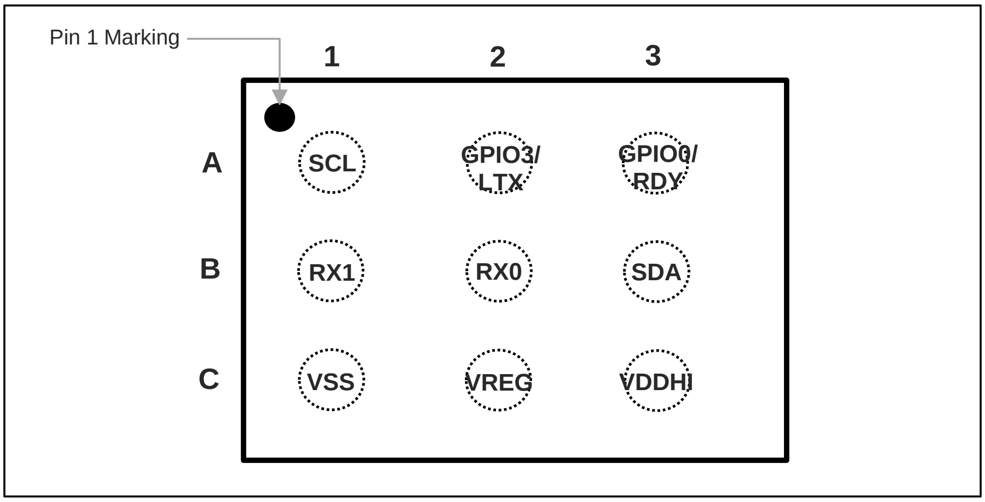


Figure 1.3 IQS620A pin-out (WLCSP-9 package top view; markings may differ)

Table 1.2 WLCSP-9 pin-out description

IQS620A in WLCSP-9			
Pin	**Name**	**Type**	**Function**
A1	SCL	Digital input / output	**SCL** (I^2C Clock signal)
A2	GPIO3 / LTX	Digital output / Analogue transmitter electrode	PWM signal output (higher priority) / Connect to inductive sensor's transmitting coil (lower priority)
A3	GPIO0 / RDY	Digital output Open drain active low logic	SAR activation output (higher priority) **RDY** (I^2C Ready interrupt signal; lower priority)
B1	RX1	Analogue receiving electrode	Connect to conductive area intended for sensor receiving
B2	RX0	Analogue receiving electrode	Connect to conductive area intended for sensor receiving
B3	SDA	Digital input / output	**SDA** (I^2C Data signal)
C1	VSS	Supply input	Common ground reference
C2	VREG	Voltage regulator output	Regulates the system's internal voltage Requires external capacitors to ground
C3	VDDHI	Supply input	Supply: IQS620A: 1.8V – 3.3V

1.3 Reference schematic

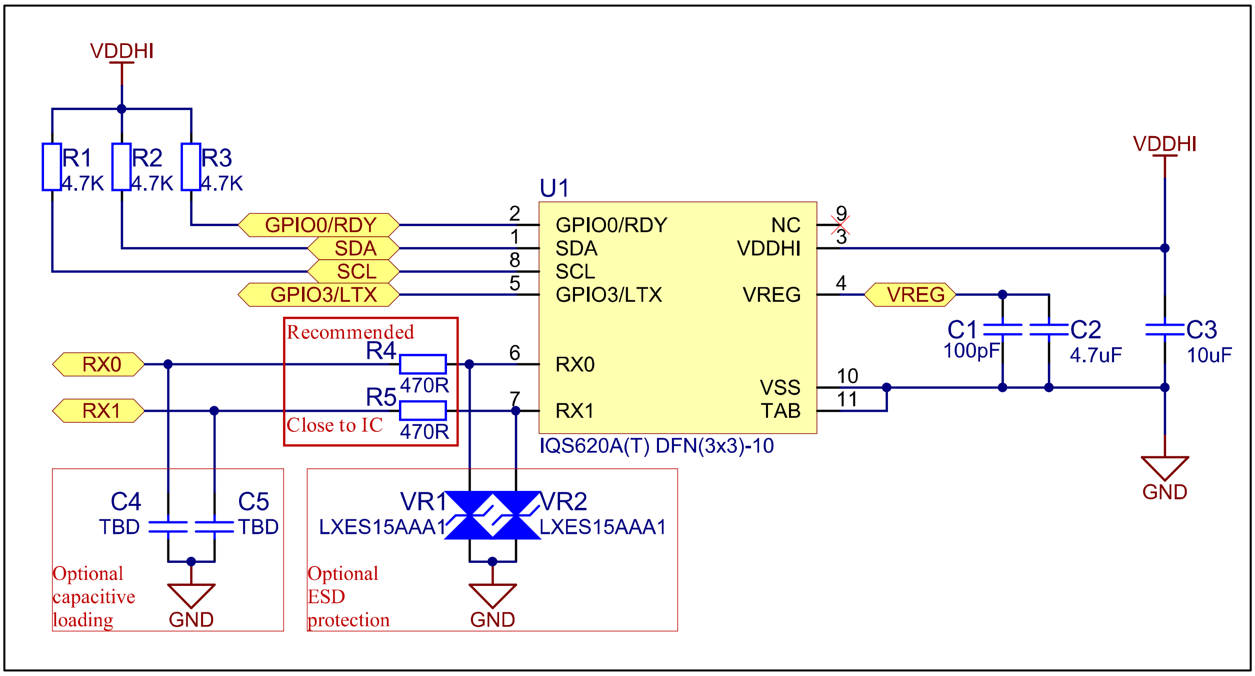


Figure 1.4 IQS620A DFN(3x3)-10 reference schematic

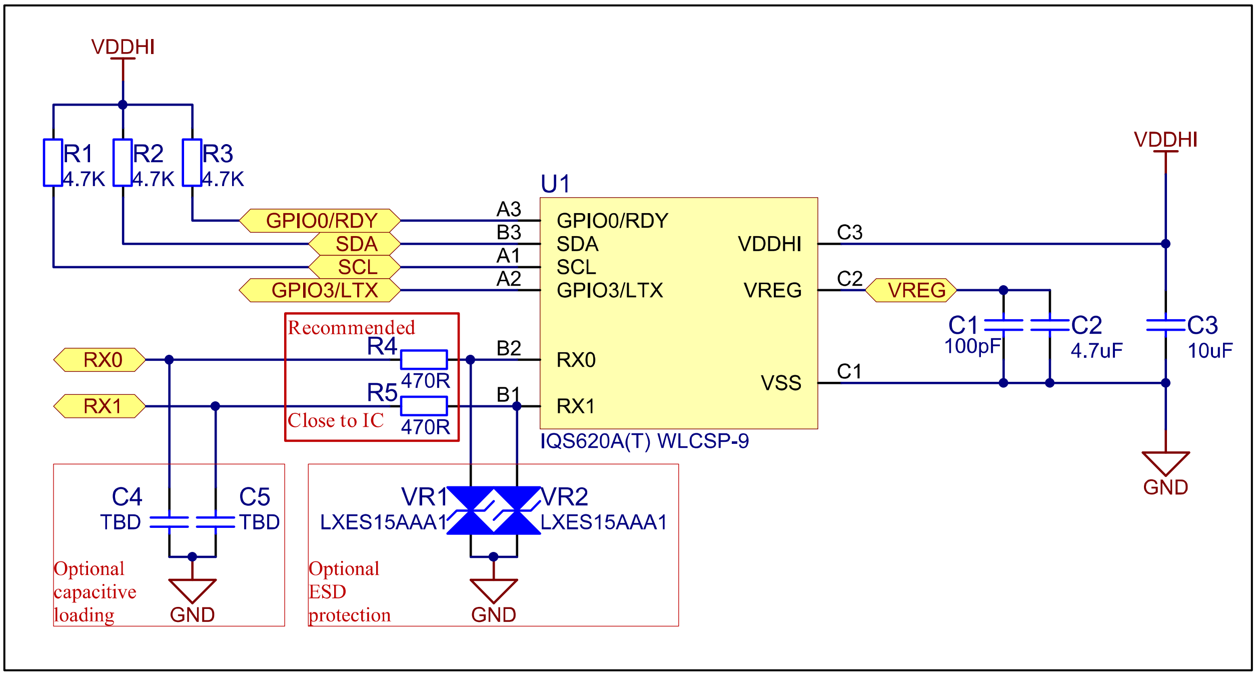


Figure 1.5 IQS620A WLCSP-9 reference schematic

Please note:

- C1, C2 and C3 should be placed as close as possible to the IQS620A package and should terminate using the shortest possible path to the IQS GND connection pin.
- R4 & R5 are recommend 0603 ESD protection diodes but also aid in sensor RF immunity. The values can be increased up to 4kΩ for severe RF noise environments.
- C4 & C5 are optional loading capacitors and should only be used if intended to de-sensitize sensors or match one sensor’s capacitive load with another electrode implementation.
- VR1 & VR2 are optional TVS diode for ESD clamping and noise suppression. Ensure the correct layout principles are followed when placed and routed.

1.4 Sensor channel combinations

The table below summarizes the IQS620(A)'s sensor and channel associations.

Table 1.3 Sensor - channel allocation

	Sensor / UI type	CH0	CH1	CH2	CH3	CH4	CH5
Capacitive	Self capacitive	○	○	○			
	SAR UI 1CH self (2 level + movement)	● Main	● Movement				
	SAR UI 2CH self (3 level)	●	●	●			
	Hysteresis UI			●			
Hall-effect	Hall-effect switch UI					● Positive	● Negative
Inductive	Mutual inductive	○	○	○			
	Hysteresis UI			●			
Temperature	Temperature monitoring				●		

Key:

○ - Optional implementation

● - Fixed use for UI

1.5 ProxFusion® Sensitivity

The measurement circuitry uses a temperature stable internal sample capacitor (C_S) and internal regulated voltage (V_{REG}). Internal regulation provides for more accurate measurements.

The Automatic Tuning Implementation (ATI) is a sophisticated technology implemented on the ProxFusion® device series. It allows for optimal performance of the devices for a wide range of sense electrode capacitances, without modification or addition of external components. The ATI functionality ensures that sensor sensitivity is not affected by external influences such as temperate, parasitic capacitance and ground reference changes.

The ATI process adjusts three values (Coarse multiplier, Fine multiplier, Compensation) using two parameters (ATI base and ATI target) as inputs. A 10-bit compensation value ensures that an accurate target is reached. The base value influences the overall sensitivity of the channel and establishes a base count for the ATI algorithm. A rough estimation of sensitivity can be approximated using the relation:

$$Sensitivity \propto \frac{Target}{Base}$$

As seen from this equation, the sensitivity can be increased by either increasing the Target value or decreasing the Base value. A lower base value will typically result in lower multipliers and more compensation would be required. It should, however, be noted that a higher sensitivity will yield a higher noise susceptibility. Refer to Appendix B for more information regarding Hall-effect ATI.

2 Capacitive sensing

2.1 Introduction to ProxSense®

Building on the previous successes from the ProxSense® range of capacitive sensors, the same fundamental sensor engine has been implemented in the ProxFusion® series.

The capacitive sensing capabilities of the IQS620(A) include:

- Self-capacitive sensing.
- Maximum of 3 capacitive channels to be individually configured.
  - Individual sensitivity setups
  - Alternative ATI modes
- Discreet button UI:
  - Fully configurable 2 level threshold setups for prox & touch activation levels.
  - Customizable filter halt time
- Single channel SAR UI:
  - For passing the SAR qualification
  - Movement sensing to distinguish between stationary in-contact objects and human interference
  - Quick release detection feature (fully configurable)
  - GPIO output of SAR activation (on GPIO0) for driving e.g. WWAN module directly
  - Up to three triggers levels (proximity, touch and deep touch) for dynamic power reduction
  - All triggers offer never time-out capability
- Two Channel SAR UI:
  - For passing the SAR qualification latest requirements (EN50566)
  - Up to three dedicated triggers levels per sensor for dynamic power reduction
  - All triggers offer never time-out capability
- Hysteresis UI:
  - 4 Optional prox and touch activation hysteresis selections.
  - Fully configurable 2 level threshold setups for prox & touch activation levels.
  - Customizable filter halt time

2.2 Channel specifications

The IQS620(A) provides a maximum of 3 channels available to be configured for capacitive sensing. Each channel can be setup separately according to the channel's associated settings registers.

There are three distinct capacitive user interfaces available to be used.

a) Self capacitive proximity/touch UI

b) SAR UIs

c) Hysteresis UI

When the single channel SAR UI is activated (ProxFusion Settings4: bit7-6):

- Channel 0 is used for the main capacitive sensing channel for SAR detection and release detection.
- Channel 1 is used for capacitive movement detection.

When the two channel SAR UI is active (ProxFusion Settings4: bit7-6):

- Channel 0 & 1 is used for the first or main SAR antenna sensor (Rx0)
- Channel 2 is used for a second SAR antenna sensor (Rx1)

Table 2.1 Capacitive sensing - channel allocation

Mode	CH0	CH1	CH2	CH3	CH4	CH5
Self capacitive	o	o	o			
Single SAR UI self	• Main	• Movement				
Two channel SAR UI self	•	•	•			
Hysteresis UI			•			

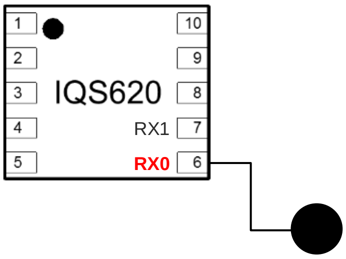
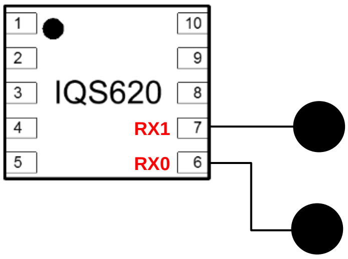
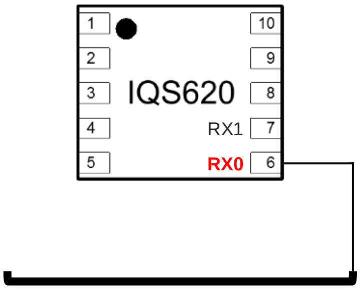
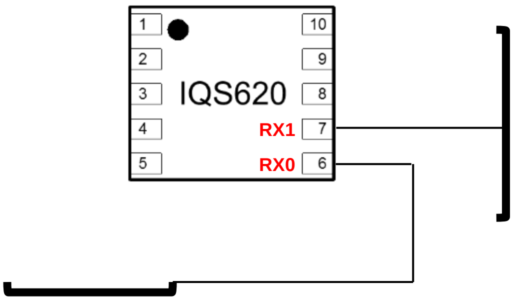
Key:

○ - Optional implementation
• - Fixed use for UI

2.3 Hardware configuration

In the table below are multiple options of configuring sensing (Rx) electrodes to realize different implementations (combinations not shown).

Table 2.2 Capacitive sensing - hardware description

	Self capacitive configuration
1 button	
2 buttons	
Single SAR antenna	
Two SAR antenna	

2.4 Software configuration

12.1.1 Registers to configure for capacitive sensing:

Table 2.3 Capacitive sensing settings registers

Address	Name	Description	Recommended setting
0x40 0x41 0x42	ProxFusion Settings 0	Sensor mode and configuration of each channel.	Sensor mode should be set to capacitive mode An appropriate RX should be chosen
0x43 0x44 0x45	ProxFusion Settings 1	Channel settings for the ProxSense sensors	Full ATI is recommended for fully automated sensor tuning.
0x46 0x47 0x48	ProxFusion Settings 2	ATI settings for ProxSense sensors	ATI target should be more than ATI base to achieve an ATI
0x49 0x4A 0x4B	ProxFusion Settings 3	Additional Global settings for ProxSense sensors	None
0x50	ProxFusion Settings 4	UI enable command and filter settings	Choose Normal 2 Channel, Single SAR or 3 level dual SAR UI
0x51	ProxFusion Settings 5	Advance sensor settings	None

12.1.2 Registers to configure for the standard UI (proximity / touch):

Please note: If the standard UI (proximity / touch) is used then the single SAR UI (proximity / touch / movement) cannot be used and the special SAR registers should not be configured or used. Initializing inactive UI registers can corrupt other active UI's.

Table 2.4 standard UI settings registers

Address	Name	Description
0x60 0x62 0x64	Proximity threshold	Proximity Thresholds for all capacitive channels (except for single channel SAR active on channel 0)
0x61 0x63 0x65	Touch threshold	Touch Thresholds for all capacitive channels
0x66	ProxFusion standard UI halt time	Halt timeout setting for all capacitive channels

12.1.3 Registers to configure for the two channel SAR UI (proximity / touch / deep touch):

Please note: If the two channel SAR UI is used then the special SAR UI registers (proximity, movement, release detection) cannot be used and the settings registers should be used as shown in the table below. Initializing inactive UI registers can corrupt other active UI's.

Table 2.5 Two channel SAR UI settings registers

Address	Name	Description
0x50	ProxFusion settings 4	Two channel SAR UI enable command (bit7-6).
0x80	Hysteresis settings	Disable Hysteresis for proximity and touch thresholds
0x60	CH0 Proximity threshold	SAR Antenna 1 proximity threshold
0x61	CH0 Touch threshold	SAR Antenna 1 touch threshold
0x63	CH1 Touch threshold	SAR Antenna 1 deep touch threshold
0x81	CH2 filter halt threshold	SAR Antenna 2 proximity threshold
0x82	CH2 proximity threshold	SAR Antenna 2 touch threshold
0x83	CH2 touch threshold	SAR Antenna 2 deep touch threshold
0x66	ProxFusion standard UI halt time	Halt timeout setting for all capacitive channels. Set to 0xFF for no time-out as required by SAR applications

12.1.4 Registers to configure for the single channel SAR UI:

Please note: If the single SAR UI is used then the discreet button UI cannot be used and the ProxFusion discrete UI settings registers should not be configured or used. Initializing inactive UI registers can corrupt other active UI's.

Table 2.6 Single channel SAR UI settings registers

Address	Name	Description
0x50	ProxFusion settings 4	Single channel SAR UI (prox / touch / movement) enable command (bit7-6).
0x70	SAR UI Settings 0	Filter settings for movement and QRD, SAR activation output to GPIO0 (RDY signal disabled)
0x71	SAR UI Settings 0	LTA halt timeout and movement threshold settings
0x72	Quick release threshold Ch0	Threshold setting to trigger a quick release based on the Quick release count values in register 0xF2 & 0xF3.
0x73	Filter halt threshold Ch0	Threshold value for channel 0 LTA filter halt
0x74	SAR Proximity threshold Ch0	Proximity threshold used for SAR activations on channel 0
0x75	Quick release halt time	Halt timeout setting for channel 0 LTA after a quick release trigger with zero movement

12.1.5 Registers to configure for the Hysteresis UI:

Please note: Only channel 2 can be used with the Hysteresis UI. Please setup channel 2 accordingly if required. The Hysteresis UI can be used simultaneously with the discrete button UI or SAR UI.

Table 2.7 Hysteresis UI settings registers

Address	Name	Description
0x50	ProxFusion settings 4	Hysteresis UI enable command (bit6).
0x80	Hysteresis UI settings	Hysteresis selection options for prox and touch activations
0x81	Hysteresis UI filter halt threshold	UI filter halt threshold value to halt the LTA value from following
0x82	Hysteresis UI prox threshold	Threshold setting to trigger a prox activation on channel 2 data.
0x83	Hysteresis UI touch threshold	Threshold value to trigger a touch activation on channel 2 data.

12.1.6 Example code:

Example code for an Arduino Uno can be downloaded at:

www.azoteq.com//images/stories/software/IQS62x_Demo.zip

2.5 Sensor data output and flags

The following registers should be monitored by the master to detect capacitive sensor output and SAR activations.

a) The **Global events register (0x11)** will show the IQS620(A)'s main events. Bit0 is dedicated to the ProxSense activations and two other bits (bit7 & bit1) is provided to show the state of the single channel SAR UI. SINGLE_SAR_ACTIVE (bit7) will be constantly active during SAR detection. SAR event (bit1) will toggle upon each SAR qualified event or change of SAR status. Bit3 is dedicated to the Hysteresis UI activations (for ch2 data only).

Global Events (0x11)								
Bit Number	**7**	6	5	4	**3**	2	**1**	**0**
Data Access	**R**	R	R	R	**R**	R	**R**	**R**
Name	**SINGLE SAR ACTIVE**	PMU EVENT	SYS EVENT	TEMP EVENT	**HYSTE-RESIS UI EVENT**	HALL EVENT	**SINGLE SAR EVENT**	**PROX SENSE EVENT**

b) The **ProxFusion UI flags (0x12)** and **SAR UI flags (0x13)** provide more detail regarding the outputs. A prox and touch output bit for each channel 0 to 3 is provided in the ProxFusion UI flags register.

c) The **SAR UI Flags (0x13)** register will show detail regarding the state of the SAR output as well as Quick release toggles, movement activations and the state of the filter (halted or not). The SAR UI can also be used with the inductive sensing capabilities and is explained in section 4. Inductive sensing.

ProxFusion UI flags (0x12)								
Bit Number	7	**6**	**5**	**4**	3	**2**	**1**	**0**
Data Access	-	**R**	**R**	**R**	-	**R**	**R**	**R**
Name	-	**CH2_T**	**CH1_T**	**CH0_T**	-	**CH2_P**	**CH1_P**	**CH0_P**
SAR UI flags (0x13)								
Bit Number	7	6	5	**4**	3	**2**	**1**	**0**
Data Access	-	-	-	**R**	-	**R**	**R**	**R**
Name	-	-	-	**SAR ACTIVE**	-	**QUICK RELEASE**	**MOVE-MENT**	**FHALT**
Hysteresis UI flags (0x13)								
Bit Number	**7**	**6**	**5**	4	3	2	1	0
Data Access	**R**	**R**	**R**	-	-	-	-	-
Name	**Signed output**	**TOUCH**	**PROX**	-	-	-	-	-

d) When the "Two channel SAR UI" is chosen for proximity, touch and deep touch on two channels, the ProxFusion UI flags and Hysteresis UI flags are defined as shown below:

Two channel SAR UI flags (0x12)								
Bit Number	7	6	**5**	**4**	3	**2**	1	**0**
Data Access	-	R	**R**	**R**	-	**R**	R	**R**
Name	-	-	**ANT 1 DEEP TOUCH**	**ANT 1 TOUCH**	-	**ANT 2 PROX**	-	**ANT 1 PROX**
Two channel SAR UI flags 2 (0x13)								
Bit Number	7	**6**	**5**	4	3	2	1	0
Data Access	R	**R**	**R**	R	-	R	R	R
Name	-	**ANT 2 DEEP TOUCH**	**ANT 2 TOUCH**	-	-	-	-	-

3 Hall-effect sensing

3.1 Introduction to Hall-effect sensing

The IQS620(A) has an internal Hall-effect sensing plate (on chip). No external sensing hardware is required for Hall-effect sensing.

The Hall-effect sensor measures the generated voltage difference across the plate, which can be modelled as a Wheatstone bridge. The voltage difference is converted to a current using an operational amplifier in order to be measured by the same ProxSense® sensor engine.

Advanced digital signal processing is performed to provide sensible output data.

- Two threshold levels are provided (prox & touch).
- Hall-effect output can be linearized through a selectable inverse calculator option.
- North/South field direction indication provided.
- Differential Hall-Effect sensing:
  - Removes common mode disturbances
  - North-South field indication

3.2 Channel specifications

Channels 4 and 5 are dedicated to Hall-effect sensing. Channel 4 performs the positive direction measurements and channel 5 will handle all measurements in the negative direction. These two channels are used in conjunction to acquire differential Hall-effect data and will always be used as input data to the Hall-effect UI's.

There are two distinct Hall-effect user interfaces available:

a) General Hall-effect sensing

b) Hall-effect switch UI

Table 3.1 Hall-effect sensor – channel allocation

<table>
<tr><th>Mode</th><th>CH0</th><th>CH1</th><th>CH2</th><th>CH3</th><th>CH4</th><th>CH5</th></tr>
<tr><td>Hall-effect switch UI</td><td></td><td></td><td></td><td></td><td rowspan="3">●
Positive</td><td rowspan="3">●
Negative</td></tr>
<tr><td>Smart cover</td><td></td><td></td><td></td><td></td></tr>
<tr><td>Slide switch</td><td></td><td></td><td></td><td></td></tr>
</table>

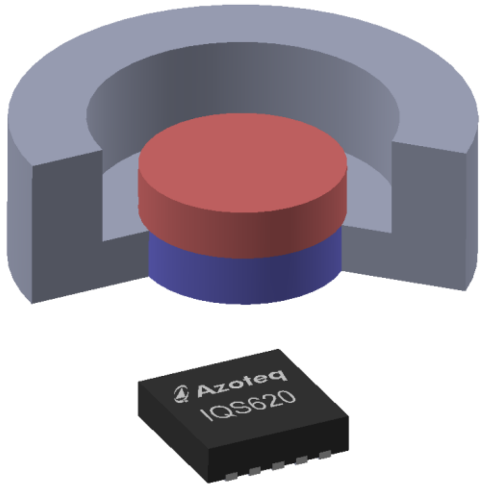
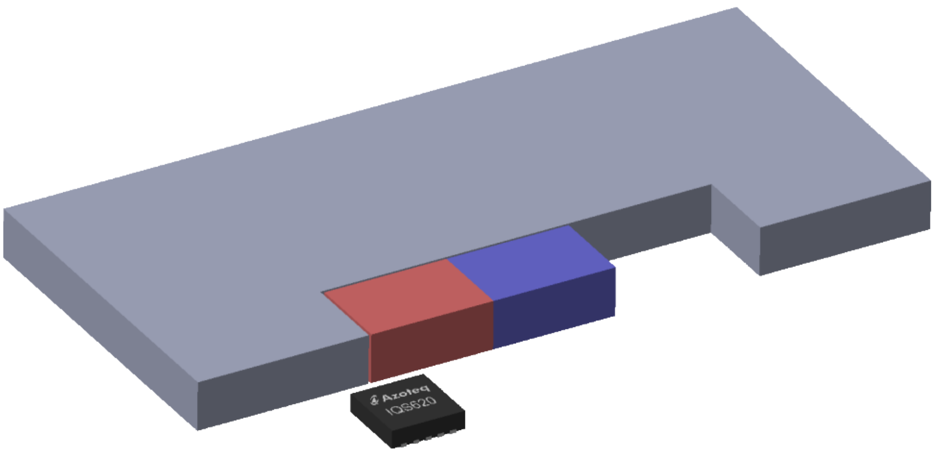
Key:

○ - Optional implementation

● - Fixed use for UI

3.3 Hardware configuration

Rudimentary hardware configurations

	Axially polarized magnet (linear movement or magnet presence detection)
Hall-effect push switch	
Smart cover	
	Bar magnet (linear movement and magnet field detection)
Slide switch	

3.4 Software configuration

12.1.1 Registers to configure for Hall-effect sensing:

Table 3.2 Hall-effect sensing settings registers

Address	Name	Description	Recommended setting
0x90	Hall-effect settings 0	Charge frequency divider and ATI mode settings	Charge frequency adjusts the conversion rate of the Hall-effect channels. Faster conversions consume less current. Full ATI is recommended for fully automated sensor tuning.
0x91	Hall-effect settings 1	ATI base and target selections	ATI target should be more than ATI base to achieve an ATI
0xA0	Hall-effect switch UI settings	Various settings for the Hall-effect switch UI	None
0xA1	Hall-effect switch UI proximity threshold	Proximity Threshold for UI	Less than touch threshold
0xA2	Hall-effect switch UI touch threshold	Touch Threshold for UI	None

12.1.2 Example code:

Example code for an Arduino Uno can be downloaded at:

www.azoteq.com//images/stories/software/IQS62x_Demo.zip

3.5 Sensor data output and flags

The following registers can be monitored by the master to detect Hall-effect related events.

a) One bit in the **Global events (0x11)** register is dedicated to the Hall-effect output. Bit2 **HALL_EVENT** will be toggled for any Hall-effect UI detections.

Global events (0x11)								
Bit Number	7	6	5	4	3	**2**	1	0
Data Access	R	R	R	R	R	**R**	R	R
Name	SAR ACTIVE	PMU EVENT	SYS EVENT	TEMP EVENT	HYSTE-RESIS UI EVENT	**HALL EVENT**	SAR EVENT	PROX SENSE EVENT

b) The **Hall-effect UI flags (0x16)** register provides the standard two-level activation output (prox = **HALL_POUT** & touch = **HALL_TOUT**) as well as a **HALL_N/S** bit to indicate the magnet polarity orientation.

Hall-effect UI flags (0x16)								
Bit Number	7	6	5	4	3	**2**	**1**	**0**
Data Access	-	-	-	-	-	**R**	**R**	**R**
Name	-	-	-	-	-	**HALL TOUT**	**HALL POUT**	**HALL N/S**

c) The **Hall-effect UI output (0x17 & 0x18)** registers provide a 16-bit value of the Hall-effect amplitude detected by the sensor.

Hall-effect UI Output (0x17 - 0x18)								
Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data Access	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
Name	**Hall-effect UI output low byte**							
Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Data Access	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
Name	**Hall-effect UI output high byte**							

4 Inductive sensing

4.1 Introduction to inductive sensing

The IQS620(A) provides inductive sensing capabilities in order to detect the presence of metal/metal-type objects. Prox and touch thresholds are widely adjustable and individual hysteresis settings are definable for each using the Hysteresis UI.

4.2 Channel specifications

The IQS620(A) requires both Rx sensing pins as well as the Tx pin for mutual inductive sensing.

Channels 0, 1 and/or 2 can be setup for inductive sensing although only channel 2 can be used for the Hysteresis UI which is attractive as an inductive data processing UI.

The Hysteresis UI provides superior options for prox and touch activation with filter halt and hysteresis settings.

a) Hysteresis UI (Dedicated to CH2)

Table 4.1 Inductive sensor – channel allocation

Mode	CH0	CH1	CH2	CH3	CH4	CH5
Mutual inductive	o	o	o			
Hysteresis UI			•			

Key:

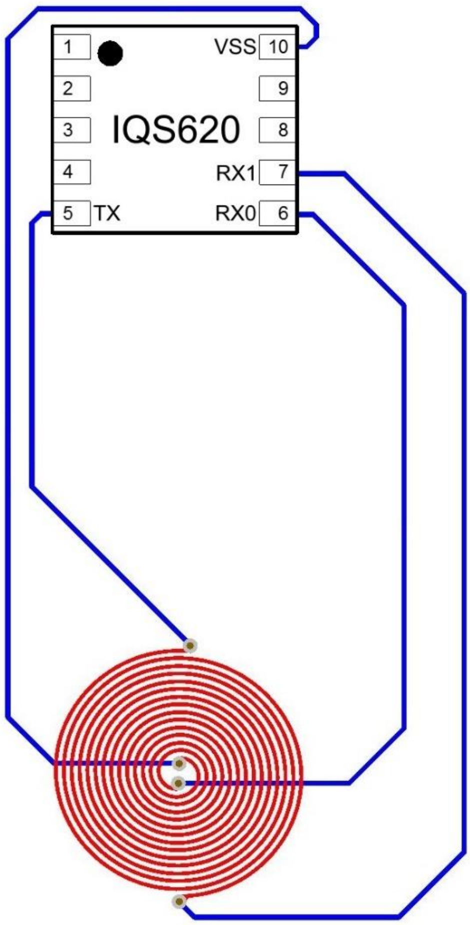
○ - Optional implementation

● - Fixed use for UI

4.3 Hardware configuration

Rudimentary hardware configuration. Please refer to application note for design details.

Table 4.2 Inductive hardware description

Mutual inductive


4.4 Software configuration

12.1.1 Registers to configure for inductive sensing:

Please note: If the discreet button UI is used then the SAR UI cannot be used, and the SAR registers should not be configured or used. Initializing inactive UI registers can corrupt other active UI's.

Table 4.3 Inductive sensing settings registers

Address	Name	Description	Recommended setting
0x42	ProxFusion Settings 0	Sensor mode and configuration of channel 2.	Sensor mode should be set to inductive mode Both RX0 and RX1 should be active on channel 2
0x45	ProxFusion Settings 1	Channel 2 settings for the inductive sensor	Full ATI is recommended for fully automated sensor tuning.
0x48	ProxFusion Settings 2	ATI settings for the inductive sensor	ATI target should be more than ATI base to achieve an ATI
0x4B	ProxFusion Settings 3	Additional settings for the inductive sensor	None
0x50	ProxFusion Settings 4	UI enable command and filter settings	Enable the Hysteresis UI filter according to application

12.1.2 Registers to configure for the Hysteresis UI:

Please note: Only channel 2 can be used with the Hysteresis UI. Please setup channel 2 accordingly if required. The Hysteresis UI can be used simultaneously with the discrete button UI or SAR UI.

Table 4.4 Hysteresis UI settings registers

Address	Name	Description
0x50	ProxFusion settings 4	Hysteresis UI enable command
0x80	Hysteresis UI Settings	Hysteresis settings for the Hysteresis UI prox and touch output
0x81	Hysteresis UI filter halt threshold	Threshold setting to trigger a filter halt for sensor data on channel 2
0x82	Hysteresis UI proximity threshold	Proximity threshold used for sensor data on channel 2
0x83	Hysteresis UI touch threshold	Touch threshold used for sensor data on channel 2

4.5 Sensor data output and flags

The following registers can be monitored by the master to detect inductive sensor related events.

a) **Global events (0x11)** to prompt for inductive sensor activation. Bit0 **PROXSENSE_EVENT** will indicate the detection of a metal object on any of the channels 0, 1 or 2 using the discreet mutual inductive sensing UI permitted that the specific channel is setup for inductive sensing.

b) Bit3 denoted as **HYSTERESIS_UI_EVENT** will indicate the detection of a metal object using the hysteresis UI on an inductive sensing channel permitted that the hysteresis UI is activated.

Global events (0x11)								
Bit Number	7	6	5	4	**3**	2	**1**	**0**
Data Access	R	R	R	R	**R**	R	**R**	**R**
Name	SAR ACTIVE	PMU EVENT	SYS EVENT	TEMP EVENT	**HYSTE-RESIS UI EVENT**	HALL EVENT	**SAR EVENT**	**PROX SENSE EVENT**

c) The **Hysteresis UI flags (0x13)** register provides the classic prox/touch two level activation outputs as well as a bit to distinguish whether the current counts are above or below the LTA.

Hysteresis UI flags (0x13)								
Bit Number	**7**	**6**	**5**	4	3	2	1	0
Data Access	**R**	**R**	**R**	-	-	-	-	-
Name	**Signed output**	**TOUCH**	**PROX**	-	-	-	-	-

d) **Hysteresis UI output (0x14 & 0x15)** registers will provide a combined 16-bit value to acquire the magnitude of the inductive sensed object.

Hysteresis UI output (0x14 - 0x15)								
Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data Access	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
Name	**Hysteresis UI output low byte**							
Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Data Access	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
Name	**Hysteresis UI output high byte**							

5 Temperature monitoring

5.1 Introduction to temperature monitoring

The IQS620(A) provides temperature monitoring capabilities which can be used for temperature change detection in order to ensure the integrity of other sensing technology. The use of the temperature sensor is primarily to reseed other sensor channels to account for sudden changes in environmental conditions.

The IQS620(A) uses a linearly proportional to absolute temperature sensor for temperature data. The temperature output data is given by,

$$T = \frac{a.2^{19}}{b.CH_3} + c$$

Where a, b and c are constants that can be determined to provide a required output data as a function of device temperature. Additionally, the channel setup must be calculated during a testing process.

The IQS620AT/P part(s) have been calibrated during production and will use OTP stored values calculated for that specific part for parameters a, b and c as well as a 4-bit value used for the fine multiplier setup of channel 3 (default always uses the lowest course multiplier).

Table 5.1 Temperature calibration setting registers and ranges

Parameter		IQS620			IQS620A	
Name	**Description**	**Register**		**Range**	**Register**	**Range**
a	$Multiplier$	0xC2	Higher nibble	1 – 16	0xC2	1 – 256
b	$Divider$		Lower nibble	1 – 16	0xC3	1 – 256
c	$Offset$	0xC3		0 – 255	0xC4	0 – 255

5.2 Channel specifications

The IQS620(A) requires only external passive components to do temperature monitoring (no additional circuitry/components required). The temperature UI will be executed using data from channel 3.

Table 5.2 Temperature sensor – channel allocation

Mode	CH0	CH1	CH2	CH3	CH4	CH5
Temperature monitoring				●		

Key:

○ - Optional implementation

● - Fixed use for UI

Please note that channels 4 and 5, for Hall-effect sensing, needs to be active in order for the temperature monitoring UI to execute correctly on version 0 and 1 software versions.

For version 2 software devices Hall-effect channels 4 & 5 may be disabled regardless.

5.3 Hardware configuration

No additional hardware required. Temperature monitoring is realized on-chip.

5.4 Software configuration

12.1.1 Registers to configure for temperature monitoring

For IQS620 only:

Table 5.3 Temperature monitoring settings registers

Address	Name	Description	Recommended setting
0xC0	Temperature UI settings	Channel reseed settings	Reseed enable should be set
0xC1	Multipliers channel 3	Temperature sensor channel multiplier selection	Dependent on calibration step
0xC2	Temperature calibration data 0	4-bit Multiplier (a+1) and 4-bit divider (b+1) calibration values	Requires sample calibration
0xC3	Temperature calibration data 1	8-bit Offset (c) calibration value	Requires sample calibration

For IQS620AX:

Table 5.4 Temperature monitoring settings registers

Address	Name	Description	Recommended setting
0xC0	Temperature UI settings	Channel reseed settings	Reseed enable should be set
0xC1	Multipliers channel 3	Temperature sensor channel multiplier selection	Dependent on calibration step Defined during fabrication for IQS620AT/P samples
0xC2	Temperature UI calibration multiplier	8-bit Multiplier (a+1) calibration value	Requires sample calibration Defined during fabrication for IQS620AT/P samples
0xC3	Temperature calibration UI divider	8-bit Divider (b+1) calibration value	Requires sample calibration Defined during fabrication for IQS620AT/P samples
0xC4	Temperature UI offset	8-bit Offset (c) calibration value	Requires sample calibration Defined during fabrication for IQS620AT/P samples

5.5 Sensor data output and flags

The following registers can be monitored by the master to detect temperature sensor related events.

e) **Global events (0x11)** to prompt for temperature trip activation. Bit4 denoted as TEMP_EVENT will indicate the detection of a temperature event.

Global events (0x11)								
Bit Number	7	6	5	**4**	3	2	1	0
Data Access	R	R	R	**R**	R	R	R	R
Name	SAR ACTIVE	PMU EVENT	SYS EVENT	**TEMP EVENT**	HYSTE-RESIS UI EVENT	HALL EVENT	SAR EVENT	PROX SENSE EVENT

f) The **Temperature UI flags (0x19)** register provides a temperature trip activation output bit if the condition of a temperature reseed threshold is tripped.

Temperature UI flags (0x19)								
Bit Number	**7**	**6**	**5**	4	3	2	1	0
Data Access	**R**	-	-	-	-	-	-	-
Name	**Temp trip**	-	-	-	-	-	-	-

g) **Temperature UI output (0x1A & 0x1B)** registers will provide a combined 16-bit output value for the measured internal IC temperature.
Please note: For the IQS620A**T/P** part(s) the calibration was done so that the UI output is offset by a decimal value of +100 in order to be able to calculate and represent absolute temperatures below 0°C in the controller arithmetic and temperature UI capabilities.
Example: Temperature UI output = 120'D → 20°C or 90'D → -10°C

Temperature UI output (0x1A – 0x1B)								
Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data Access	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
Name	**Temperature output low byte**							
Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Data Access	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
Name	**Temperature output high byte**							

6 Device clock, power management and mode operation

6.1 Device main oscillator

The IQS620(A) has a **16MHz** main oscillator (default enabled) to clock all system functionality.

An option exists to reduce the main oscillator to 4MHz. This will result in charge transfer frequencies to be one-quarter of the default implementations. System timers are adjusted so that timeouts and report rates remain the same if possible.

To set this option this:

- As a software setting – Set the System_Settings: bit4 = 1, via an I^2C command.
- As a permanent setting – Set the OTP option in OTP Bank 0: bit2 = 1, using IQS620A PC software.

6.2 Device modes

The IQS620(A) supports the following modes of operation;

- **Normal mode** (Fixed report rate)
- **Low power mode** (Reduced report rate)
- **Ultra-low power mode** (Only channel 0 is sensed for a prox)
- **Halt mode** (Suspended/disabled)
  Note: Auto modes must be disabled to enter or exit halt mode.

The device will automatically switch between the different operating modes by default. However, this Auto mode feature may be disabled by setting the DSBL_AUTO_MODE bit (Power_mode_settings 0xD2: bit5) to confine device operation to a specific power mode. The POWER_MODE bits (Power_mode_settings 0xD2: bit4-3) can then be used to specify the desired mode of operation.

12.1.1 Normal mode

Normal mode is the fully active sensing mode to function at a fixed report rate specified in the Normal mode report rate (0xD3) register. This 8-bit value is adjustable from 0ms – 255ms in intervals of 1ms.

Note: The device's low power oscillator has an accuracy of 4ms.

12.1.2 Low power mode

Low power mode is a reduced sensing mode where all channels are sensed but at a reduced oscillator speed. The sample rate can be specified in the Low Power mode report rate (0xD4) register. The 8-bit value is adjustable from 0ms – 255ms in intervals of 1ms. Reduced report rates also reduce the current consumed by the sensor.

Note: The device's low power oscillator has an accuracy of 4ms.

12.1.3 Ultra-low power mode

Ultra-low power mode is a reduced sensing mode where only channel 0 is sensed at the ultra low power report rate. Channels 1 to 5 are only updated (sensed and processed according to each channels setup) during a normal power update cycle. This NP update cycle rate can be set as a fraction of the configured ULP mode report rate. There are 8 NP segment fraction options available (Power_mode_settings: bit2-0) ranging from the fastest, ½ ULP rate to the slowest rate of 1/256 of the ULP rate. This ensures that channels 1 to 3's LTA values track any slow changes in sensor counts (typically seen over a long period for varying environmental conditions).

To enable use of the ultra-low power mode set the EN_ULP_MODE bit (Power_mode_settings: bit6). The sample rate can be specified in the Ultra-Low Power mode report rate (0xD5) register. The 8-bit value is adjustable from 0ms – 4sec in increments of 16ms for each decimal integer.

IQS620(A) wake up (return to normal mode) will occur on prox detection of channel 0.

12.1.4 Halt mode

Halt mode will suspend all sensing and will place the device in a dormant or sleep state. The device requires an I^2C command from a master to explicitly change the power mode out of the halt state before any sensor functionality can continue.

12.1.5 Mode time

The mode time defines the time period in normal or low power modes before automatically moving to a slower mode (or finally ULP mode if applicable) if no activations are registered in this time. This time is set in the Auto Mode Timer (0xD6) register. The 8-bit value is adjustable from 0ms – 2 min in intervals of 500ms.

6.3 System reset

The IQS620(A) device monitor’s system resets and events.

a) Every device power-on and reset event will set the Show Reset bit (System flags 0x10: bit7) and the master should explicitly clear this bit by setting the ACK_RESET (bit6) in System Settings.

b) The system events will also be indicated with the Global events register’s SYS_EVENT bit (Global events 0x11: bit5) if any system event occur such as a reset. This event will continuously trigger until the reset has been acknowledged.

7 Communication

7.1 I²C module specification

The device supports a standard two wire I²C interface with the addition of an RDY (ready interrupt) line. The communications interface of the IQS620(A) supports the following:

- *Fast-mode (Fm)* standard I²C up to 400kHz.
- Streaming data as well as event mode.
- The master may address the device at any time. If the IQS620(A) is not in a communication window, the device will return an ACK after which clock stretching may be induced until a communication window is entered. Additional communication checks are included in the main loop in order to reduce the average clock stretching time.
- The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

7.2 I²C Read

To read from the device a *current address read* can be performed. This assumes that the address-command is already setup as desired.

Current Address Read

Start	Control byte		Data n		Data n+1		Stop
S	Addr + READ	ACK		ACK		NACK	S

Figure 7.1 Current Address Read

If the address-command must first be specified, then a *random read* must be performed. In this case, a WRITE is initially performed to setup the address-command, and then a repeated start is used to initiate the READ section.

Random Read

Start	Control byte		Address-command		Start	Control byte		Data n		Stop
S	Addr + WRITE	ACK		ACK	S	Addr + READ	ACK		NACK	S

Figure 7.2 Random Read

7.3 I²C Write

To write settings to the device a *Data Write* is performed. Here the Address-Command is always required, followed by the relevant data bytes to write to the device.

Data Write

Start	Control byte		Address-Command		Data n		Data n+1		Stop
S	Addr + WRITE	ACK		ACK		ACK		ACK	S

Figure 7.3 I²C Data Write

7.4 Stop-bit disable option

The IQS620A parts offer:

- an additional I²C settings register (0xDA) specifically added for stop-bit disable functionality,
- as well as a RDY timeout period register (0xD9) in order to set the required timeout period for termination of any communication windows (RDY = Low) if no I²C activity is present on SDA and SCL pins.

Customers using an MCU with a binary serial-encoder peripheral which is not fully I²C compatible (but provide some crude serial communication functions) can use this option to configure the IQS620A so that any auto generated stop command from the serial peripheral can be ignored by the IQS620A I²C hardware. This will restrict the IQS620A from immediately exiting a communication window until all required communication has been completed and a stop command can correctly be transmitted. Please refer to the figures below for serial data transmission examples.

Please note:

1. Stop-bit disable and enable must be performed at the beginning and end of a communication window. The first and last I²C register to be written to ensure no unwanted communication window termination.
2. Leaving the Stop-bit disabled will result in successful reading of registers but will not execute any commands written over I2C in a communication window being terminated after an RDY timeout and with no IQS recognised stop command.
3. The default RDY timeout period for IQS620A is purposefully long (10.24ms) for slow responding MCU hardware architectures. Please set this register according to your requirements/preference.
4. These options are only available on IQS620A parts and not for IQS620.

Stop-bit Disable

Communication window open	Start	Control byte		Address-Command		Disable stop-bit		Ignored stop	Continue with reads / writes
RDY = ↓LOW	**S**	**Addr + WRITE**	**ACK**	**0xDA**	**ACK**	**0x81**	**ACK**	**S**	**…**

Figure 7.4 I²C Stop-bit Disable

Stop-bit Enable

Reads / Writes Finished	Start	Control byte		Address-Command		Enable stop-bit		Stop	Communication window closed
…	**S**	**Addr + WRITE**	**ACK**	**0xDA**	**ACK**	**0x01**	**ACK**	**S**	**RDY = ↑HIGH**

Figure 7.5 I²C Stop-bit Enable

7.5 Device address and sub-addresses

The default device address is **0x44 = DEFAULT_ADDR**.

Alternative sub-address options are definable in the following one-time programmable bits: **OTP Bank0 (bit3; 0; bit1; bit0) = SUB_ADDR_0** to **SUB_ADDR_7**

a) Default address: **0x44** = DEFAULT_ADDR (**0x44**) **OR** SUB_ADDR_0 (**0000b**)
b) Sub-address: **0x45** = DEFAULT_ADDR (**0x44**) **OR** SUB_ADDR_1 (**0001b**)
c) Sub-address: **0x46** = DEFAULT_ADDR (**0x44**) **OR** SUB_ADDR_2 (**0010b**)
d) Sub-address: **0x47** = DEFAULT_ADDR (**0x44**) **OR** SUB_ADDR_3 (**0011b**)
e) Sub-address: **0x4C** = DEFAULT_ADDR (**0x44**) **OR** SUB_ADDR_4 (**1000b**)
f) Sub-address: **0x4D** = DEFAULT_ADDR (**0x44**) **OR** SUB_ADDR_5 (**1001b**)
g) Sub-address: **0x4E** = DEFAULT_ADDR (**0x44**) **OR** SUB_ADDR_6 (**1010b**)
h) Sub-address: **0x4F** = DEFAULT_ADDR (**0x44**) **OR** SUB_ADDR_7 (**1011b**)

7.6 Additional OTP options

12.1.1 Firmware version 0 (Device software number 0x04 = D'04)

All one-time-programmable device options are located in OTP bank0.

OTP bank0								
Bit Number	7	6	5	4	3	2	1	0
Name	Internal use	COMMS ATI	Internal use	Internal use	SUB ADDRESS (bit3)	4MHz	SUB ADDRESS (bit1-0)	

Bit definitions:

- Bit 7: Internal use
  - Do not set. Leave bit cleared.
- Bit 6: Communication mode during ATI
  - 0: No streaming events are generated during ATI
  - 1: Communication continue as setup regardless of ATI state.
- Bit 5,4: Internal use
  - Do not configure
- Bit 2: Main Clock frequency selection
  - 0: Run FOSC at 16MHz
  - 1: Run FOSC at 4MHz
- Bit 3,1,0: I²C sub-address
  - I²C address = 0x44 OR SUB_ADDR

12.1.2 Firmware version 1 (Device software number 0x08 = D'08)

All one-time-programmable device options are located in OTP bank0.

OTP bank0								
Bit Number	7	6	5	4	3	2	1	0
Name	Internal use	COMMS ATI	Internal use	Internal use	SUB ADDRESS (bit3)	4MHz	SUB ADDRESS (bit1-0)	

Bit definitions:

- Bit 7: Internal use
  - Do not set. Leave bit cleared.
- Bit 6: Communication mode during ATI
  - 0: No streaming events are generated during ATI
  - 1: Communication continue as setup regardless of ATI state.
- Bit 5,4: Internal use
  - Do not configure
- Bit 2: Main Clock frequency selection
  - 0: Run FOSC at 16MHz
  - 1: Run FOSC at 4MHz
- Bit 3,1,0: I^2C sub-address
  - I^2C address = 0x44 OR SUB_ADDR

12.1.3 Firmware version 2 (Device software number 0x0D = D'13)

All one-time-programmable device options are located in OTP bank0.

OTP bank0								
Bit Number	7	6	5	4	3	2	1	0
Name	Disable Hall	COMMS ATI	Internal use	Internal use	SUB ADDRESS (bit3)	4MHz	SUB ADDRESS (bit1-0)	

Bit definitions:

- Bit 7: Disable Hall
  - 0: All sensors are active.
  - 1: Hall-effect is disabled permanently, use this option for low voltage applications.
- Bit 6: Communication mode during ATI
  - 0: No streaming events are generated during ATI
  - 1: Communication continue as setup regardless of ATI state.
- Bit 5,4: Internal use
  - Do not configure
- Bit 2: Main Clock frequency selection
  - 0: Run FOSC at 16MHz
  - 1: Run FOSC at 4MHz
- Bit 3,1,0: I^2C sub-address
  - I^2C address = 0x44 OR SUB_ADDR

7.7 Recommended communication and runtime flow diagram

The following is a basic master program flow diagram to communicate and handle the device. It addresses possible device events such as output events, ATI and system events (resets).

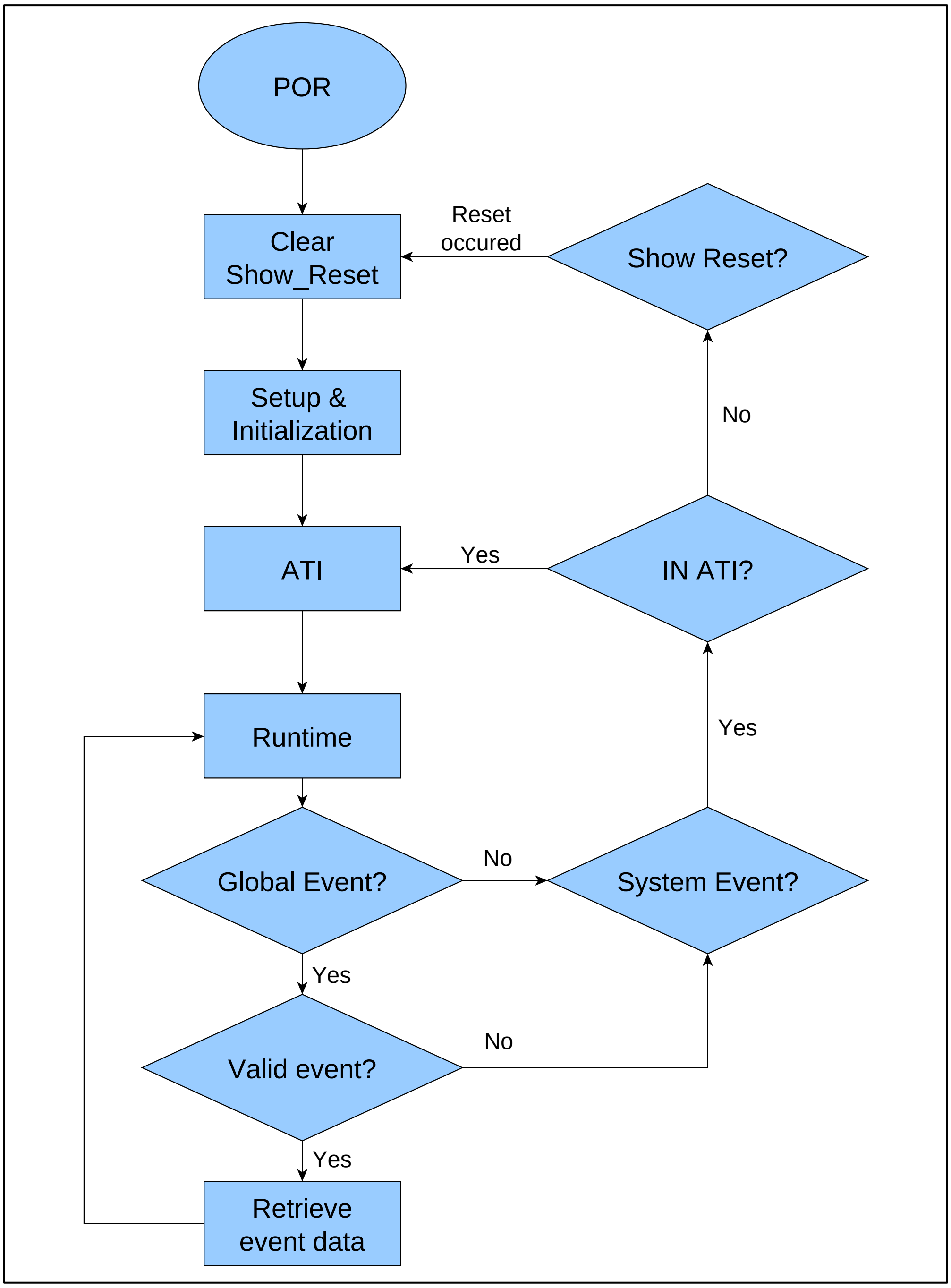


Figure 7.6 Master command structure and runtime event handling flow diagram

It is recommended that the master verifies the status of the System_Flags0 bits to identify events and resets. Detecting either one of these should prompt the master to the next steps of handling the IQS620(A).

Streaming mode communication is used for detail sensor evaluation during prototyping and/or development phases.

Event mode communication is recommended for runtime use of the IQS620(A). This reduces the communication on the I²C bus and report only triggered events.

8 Memory map

The full memory map is summarized below. Registers are explained later in this section.

Table 8.1 IQS620(A) Memory map index

Full Address	Group Name	Item Name	Data Access
0x00	Device information data	Product number	Read-Only
0x01		Software number	Read-Only
0x02		Hardware number	Read-Only
0x10	Flags and user interface data	System flags	Read-Only
0x11		Global events	Read-Only
0x12		ProxFusion UI flags	Read-Only
0x13		SAR and Hysteresis UI flags	Read-Only
0x14		Hysteresis UI output 0	Read-Only
0x15		Hysteresis UI output 1	Read-Only
0x16		Hall-effect UI flags	Read-Only
0x17		Hall-effect UI output 0	Read-Only
0x18		Hall-effect UI output 1	Read-Only
0x19		Temperature UI flags	Read-Only
0x1A		Temperature UI output 0	Read-Only
0x1B		Temperature UI output 1	Read-Only
0x20	Channel counts (raw data)	Channel 0 counts low	Read-Only
0x21		Channel 0 counts high	Read-Only
0x22		Channel 1 counts low	Read-Only
0x23		Channel 1 counts high	Read-Only
0x24		Channel 2 counts low	Read-Only
0x25		Channel 2 counts high	Read-Only
0x26		Channel 3 counts low	Read-Only
0x27		Channel 3 counts high	Read-Only
0x28		Channel 4 counts low	Read-Only
0x29		Channel 4 counts high	Read-Only
0x2A		Channel 5 counts low	Read-Only
0x2B		Channel 5 counts high	Read-Only
0x30	LTA values (filtered data)	Channel 0 LTA low	Read-Write
0x31		Channel 0 LTA high	Read-Write
0x32		Channel 1 LTA low	Read-Write
0x33		Channel 1 LTA high	Read-Write
0x34		Channel 2 LTA low	Read-Write
0x35		Channel 2 LTA high	Read-Write
0x40	ProxFusion sensor settings block 0	ProxFusion settings 0_0	Read-Write
0x41		ProxFusion settings 0_1	Read-Write
0x42		ProxFusion settings 0_2	Read-Write
0x43		ProxFusion settings 1_0	Read-Write
0x44		ProxFusion settings 1_1	Read-Write
0x45		ProxFusion settings 1_2	Read-Write
0x46		ProxFusion settings 2_0	Read-Write
0x47		ProxFusion settings 2_1	Read-Write
0x48		ProxFusion settings 2_2	Read-Write
0x49		ProxFusion settings 3_0	Read-Write
0x4A		ProxFusion settings 3_1	Read-Write
0x4B		ProxFusion settings 3_2	Read-Write

0x50	ProxFusion sensor settings block 1	ProxFusion settings 4	Read-Write
0x51		ProxFusion settings 5	Read-Write
0x52		Compensation Ch0	Read-Write
0x53		Compensation Ch1	Read-Write
0x54		Compensation Ch2	Read-Write
0x55		Multipliers Ch0	Read-Write
0x56		Multipliers Ch1	Read-Write
0x57		Multipliers Ch2	Read-Write
0x60	ProxFusion UI settings	Prox threshold Ch0	Read-Write
0x61		Touch threshold Ch0	Read-Write
0x62		Prox threshold Ch1	Read-Write
0x63		Touch threshold Ch1	Read-Write
0x64		Prox threshold Ch2	Read-Write
0x65		Touch threshold Ch2	Read-Write
0x66		ProxFusion discrete UI halt time	Read-Write
0x70	SAR UI settings	SAR UI settings 0	Read-Write
0x71		SAR UI settings 1	Read-Write
0x72		QRD threshold Ch0	Read-Write
0x73		Filter halt threshold Ch0	Read-Write
0x74		Prox threshold Ch0	Read-Write
0x75		Quick release detection halt time	Read-Write
0x80	Hysteresis UI settings	Hysteresis UI settings	Read-Write
0x81		Hysteresis UI filter halt threshold	Read-Write
0x82		Hysteresis UI prox threshold	Read-Write
0x83		Hysteresis UI touch threshold	Read-Write
0x90	Hall-effect sensor settings	Hall-effect settings 0	Read-Write
0x91		Hall-effect settings 1	Read-Write
0x92		Compensation Ch4 and Ch5	Read-Write
0x93		Multipliers Ch4 and Ch5	Read-Write
0xA0	Hall-effect switch UI settings	Hall-effect switch UI settings	Read-Write
0xA1		Hall-effect switch UI prox threshold	Read-Write
0xA2		Hall-effect switch UI touch threshold	Read-Write
0xC0	Temperature UI settings	Temperature UI settings	Read-Write
0xC1		Multipliers Ch3	Read-Write
0xC2		Temp calibration data0 / Temp calibration multiplier*	Read-Write
0xC3		Temp calibration data1 / Temp calibration divider*	Read-Write
0xC4		Temperature calibration offset*	Read-Write
0xD0	Device and power mode settings	System settings	Read-Write
0xD1		Active channels	Read-Write
0xD2		Power mode settings	Read-Write
0xD3		Normal mode report rate	Read-Write
0xD4		Low power mode report rate	Read-Write
0xD5		Ultra-low power mode report rate	Read-Write
0xD6		Auto mode time	Read-Write
0xD7		Global event mask	Read-Write
0xD8		PWM duty cycle	Read-Write
0xD9		RDY Timeout period*	Read-Write
0xDA		I^2C settings*	Read-Write
0xDB		Channel reseed enable*	Read-Write

* Only available for IQS620A v1 & v2

8.2 Device Information Data

12.1.1 Product number

Product number (0x00)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R	R	R	R	R	R	R	R
Name	Device Product Number							

Bit definitions:

- Bit 7-0: Device Product Number
  - 0x41 = D'65: IQS620 product number
  - 0x41 = D'65: IQS620A product number

12.1.2 Software number

Software number (0x01)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R	R	R	R	R	R	R	R
Name	Device Software Number							

Bit definitions:

- Bit 7-0: Device Software Number
  - 0x04 = D'04: IQS620 version 0 firmware (pre-production)
  - 0x08 = D'08: IQS620A version 1 firmware (production)
  - 0x0D = D'13: IQS620A version 2 firmware (update)

12.1.3 Hardware number

Hardware number (0x02)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R	R	R	R	R	R	R	R
Name	Device Hardware Number							

Bit definitions:

- Bit 7-0: Device Hardware Number
  - 0x82 = D'130: IQS620 hardware number
  - 0x82 = D'130: IQS620A hardware number

8.3 Flags and user interface data

12.1.1 System flags

System flags (0x10)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R	-	-	R	R	R	R	R
Name	SHOW RESET	-	-	POWER MODE		IN ATI	EVENT	NP SEG ACTIVE

Bit definitions:

- Bit 7: Reset Indicator
  - 0: No reset event
  - 1: A device reset has occurred and needs to be acknowledged.
- Bit 4-3: Active power-mode indicator
  - 00: Normal Mode
  - 01: Low Power Mode
  - 10: Ultra-Low Power Mode
  - 11: Halt Mode
- Bit 2: ATI busy indicator
  - 0: No channels are in ATI
  - 1: One or more channels are in ATI
- Bit 1: Global Event Indicator
  - 0: No new event to service
  - 1: An event has occurred and should be serviced
- Bit 0: Normal power segment indicator
  - 0: Not performing a normal power update
  - 1: Busy performing a normal power update

12.1.2 Global events

Global events (0x11)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R	R	R	R	R	R	R	R
Name	SAR ACTIVE	PMU EVENT	SYS EVENT	TEMP EVENT	HYSTE-RESIS UI EVENT	HALL EVENT	SAR EVENT	PROX SENSE EVENT

Bit definitions:

- Bit 7: SAR activation state
  - 0: SAR output inactive
  - 1: SAR output active
- Bit 6: Power management unit event flag
  - 0: No event to report
  - 1: A PMU event occurred
- Bit 5: System event flag
  - 0: No event to report
  - 1: A system event has occurred
- Bit 4: Temperature event flag
  - 0: No event to report
  - 1: A temperature event has occurred and should be handled
- Bit 4: Hysteresis UI event flag
  - 0: No event to report
  - 1: A hysteresis UI event has occurred and should be handled
- Bit 2: Hall-effect event flag

- 0: No event to report
- 1: A Hall-effect event has occurred and should be handled

- Bit 1: Single channel SAR event flag
  - 0: No event to report
  - 1: A single channel SAR event has occurred and should be handled
- Bit 0: ProxSense event flag
  - 0: No event to report
  - 1: A capacitive event has occurred and should be handled

12.1.3 ProxFusion UI flags

ProxFusion UI flags (0x12)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	R	R	R	-	R	R	R
Name	-	CH2_T	CH1_T	CH0_T	-	CH2_P	CH1_P	CH0_P

Bit definitions:

- Bit 6: Ch2 touch indicator
  - 0: Delta below touch threshold
  - 1: Delta above touch threshold
- Bit 5: Ch1 touch indicator
  - 0: Delta below touch threshold
  - 1: Delta above touch threshold
- Bit 4: Ch0 touch indicator
  - 0: Delta below touch threshold
  - 1: Delta above touch threshold
- Bit 2: Ch2 proximity indicator
  - 0: Delta below prox threshold
  - 1: Delta above prox threshold
- Bit 1: Ch1 proximity indicator
  - 0: Delta below prox threshold
  - 1: Delta above prox threshold
- Bit 0: Ch0 proximity indicator
  - 0: Delta below prox threshold
  - 1: Delta above prox threshold

12.1.4 Single channel SAR UI flags

Single channel SAR UI flags (0x13)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	-	-	R	-	R	R	R
Name	-	-	-	SAR ACTIVE	-	QRD	MOVE-MENT	FHALT

Bit definitions:

- Bit 4: SAR Standoff Active
  - 0: Delta below SAR prox THR
  - 1: Delta above SAR prox THR
- Bit 2: Quick Release Detection (QRD) indicator
  - 0: Quick release not detected
  - 1: Quick release detected
- Bit 1: Movement indicator
  - 0: Movement not detected
  - 1: Movement detected
- Bit 0: Filter Halt indicator
  - 0: Delta below filter halt THR
  - 1: Delta above filter halt THR

12.1.5 Hysteresis UI flags

Hysteresis UI flags (0x13)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R	R	R	-	-	-	-	-
Name	Signed output	TOUCH	PROX	-	-	-	-	-

Bit definitions:

- Bit 7: Delta directional signed output
  - 0: Counts < LTA. Delta positive
  - 1: Counts > LTA. Delta negative
- Bit 6: Hysteresis UI touch indicator
  - 0: Delta below touch threshold
  - 1: Delta above touch threshold
- Bit 5: Hysteresis proximity indicator
  - 0: Delta below prox threshold
  - 1: Delta above prox threshold

12.1.6 Hysteresis UI output

Hysteresis UI output (0x14 - 0x15)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R	R	R	R	R	R	R	R
Name	Hysteresis UI Output Low Byte							
Bit Number	15	14	13	12	11	10	9	8
Data Access	R	R	R	R	R	R	R	R
Name	Hysteresis UI Output High Byte							

Bit definitions:

- Bit 15-0: Hysteresis UI output value

12.1.7 Hall-effect UI flags

Hall-effect UI flags (0x16)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	-	-	-	-	R	R	R
Name	-	-	-	-	-	TOUCH	PROX	HALL N/S

Bit definitions:

- Bit 2: Hall-effect touch indicator
  - 0: Count delta below touch threshold
  - 1: Count delta above touch threshold
- Bit 1: Hall-effect proximity indicator
  - 0: Count delta below prox threshold
  - 1: Count delta above prox threshold
- Bit 0: Hall-effect North South Field indication
  - 0: North field direction present
  - 1: South field direction present

*Please note: Only for IQS620AXz**CS**R (CS = WLCSP-9) a flip chip process is used thus:*

- 0: South field direction present
- 1: North field direction present

12.1.8 Hall-effect UI output

Hall-effect UI output (0x17/0x18)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R	R	R	R	R	R	R	R
Name	Hall-effect UI Output Low Byte							
Bit Number	15	14	13	12	11	10	9	8
Data Access	R	R	R	R	R	R	R	R
Name	Hall-effect UI Output High Byte							

Bit definitions:

- Bit 15-0: Hall-effect UI output
  - 0 – 8 000: Hall-effect UI output value

12.1.9 Temperature UI flags

Temperature UI flags (0x19)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R	-	-	-	-	-	-	-
Name	Temp trip	-	-	-	-	-	-	-

Bit definitions:

- Bit 7: Temperature trip indicator
  - 0: No event to report
  - 1: Temperature reseed event occurred

12.1.10 Temperature UI output

Temperature UI output (0x1A – 0x1B)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R	R	R	R	R	R	R	R
Name	Temperature output low byte							
Bit Number	15	14	13	12	11	10	9	8
Data Access	R	R	R	R	R	R	R	R
Name	Temperature output high byte							

Bit definitions:

- Bit 15-0: Temperature UI output
  - IQS620(A): Temperature output value (relative/unitless; uncalibrated)
  - IQS620AT/P: Temperature output value -100 = Device die temperature (°C)

8.4 Channel counts (raw data)

Channel counts Ch0/1/2/3 (0x20/0x21 - 0x26/0x27)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R	R	R	R	R	R	R	R
Name	Channel Data Low Byte							
Bit Number	15	14	13	12	11	10	9	8
Data Access	R	R	R	R	R	R	R	R
Name	Channel Data High Byte							

Bit definitions:

- Bit 15-0: Channel counts
  - AC filtered or raw value counts of ProxFusion sensor channels

Channel counts Ch4/5 (0x28/0x29 - 0x2A/0x2B)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R	R	R	R	R	R	R	R
Name	Channel Data Low Byte							
Bit Number	15	14	13	12	11	10	9	8
Data Access	R	R	R	R	R	R	R	R
Name	Channel Data High Byte							

Bit definitions:

- Bit 15-0: Channel counts
  - AC filtered or raw value counts of Hall-effect sensors channels

8.5 LTA values (filtered data)

LTA Ch0/1/2 (0x30/0x31 - 0x34/0x35)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	LTA Low Byte							
Bit Number	15	14	13	12	11	10	9	8
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	LTA High Byte							

Bit definitions:

- Bit 15-0: LTA filter value output
  - Long term average value of channels

8.6 ProxFusion sensor settings block 0

12.1.1 ProxFusion settings 0

8.6.1.1 Capacitive sensing

ProxFusion settings 0_0/1/2 (0x40-0x42)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	-	-	-	-	R/W	R/W
Name	Capacitive sensor mode		Internal use	Internal use	-		RX Select	
Fixed value	0	0	-	-	-		-	

Bit definitions:

- Bit 7-6: Sensor Mode
  - 00: Capacitive sensing mode
- Bit 1-0: RX Select
  - 00: RX 0 and RX 1 is disabled
  - 01: RX 0 is enabled
  - 10: RX 1 is enabled
  - 11: RX 0 and RX 1 is enabled

8.6.1.2 Inductive sensing

ProxFusion settings 0_0/1/2 (0x40-0x42)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	-	R/W	-	-	R/W	R/W
Name	Inductive sensor mode		Internal use	Multiplier range	-		RX Select	
Fixed value	1	0	-	-	-		1	1

Bit definitions:

- Bit 7-6: Sensor Mode
  - 10: Inductive sensor mode
- Bit 4: Multiplier range
  - 0: Large
  - 1: Small
- Bit 1-0: RX Select
  - 11: RX 0 and RX 1 is enabled (Fixed selection for inductive sensing)

12.1.2 ProxFusion settings 1

8.6.2.1 Capacitive sensing

ProxFusion settings 1_0/1/2 (0x43 - 0x45)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	R/W	R/W	R/W	-	-	R/W	R/W
Name	-	CSz	CHARGE FREQ		-		AUTO ATI MODE	
Default	0x67							
	0	1	1	0	0	1	1	1

Bit definitions:

- Bit 6: CS size
  - 0: CS capacitor size is 15 pF
  - 1: CS capacitor size is 60 pF
- Bit 5-4: Charge frequency divider
  - 00: 1/2
  - 01: 1/4
  - 10: 1/8
  - 11: 1/16
- Bit 1-0: Auto ATI Mode
  - 00: ATI disabled
  - 01: Partial ATI (all multipliers are fixed)
  - 10: Semi-Partial ATI (only coarse multipliers are fixed)
  - 11: Full-ATI

8.6.2.2 Inductive sensing

ProxFusion settings 1_0/1/2 (0x43 - 0x45)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	R/W	R/W	R/W	-	-	R/W	R/W
Name	-	CSz	CHARGE FREQ		-		AUTO ATI MODE	
Default	0x67							
	0	1	1	0	0	1	1	1

Bit definitions:

- Bit 6: CS size
  - 0: CS capacitor size is 15 pF
  - 1: CS capacitor size is 60 pF
- Bit 5-4: Charge frequency divider
  - 00: 1/2
  - 01: 1/4
  - 10: 1/8
  - 11: 1/16
- Bit 1-0: Auto ATI Mode
  - 00: ATI disabled
  - 01: Partial ATI (all multipliers are fixed)
  - 10: Semi-Partial ATI (only coarse multipliers are fixed)
  - 11: Full-ATI

12.1.3 ProxFusion settings 2

8.6.3.1 Capacitive sensing

ProxFusion settings 2_0/1/2 (0x46 - 0x48)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ATI_BASE		ATI_TARGET (x32)					
Default	0xD0							
	1	1	0	1	0	0	0	0

Bit definitions:

- Bit 7-6: Auto ATI base value
  - 00: 75
  - 01: 100
  - 10: 150
  - 11: 200
- Bit 5-0: Auto ATI Target
  - ATI Target is 6-bit value x 32

8.6.3.2 Inductive sensing

ProxFusion settings 2_0/1/2 (0x46 - 0x48)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ATI_BASE		ATI_TARGET (x32)					
Default	0xD0							
	1	1	0	1	0	0	0	0

Bit definitions:

- Bit 7-6: Auto ATI base value
  - 00: 75
  - 01: 100
  - 10: 150
  - 11: 200
- Bit 5-0: Auto ATI Target
  - ATI Target is 6-bit value x 32

12.1.4 ProxFusion settings 3

8.6.4.1 Capacitive sensing

ProxFusion settings 3_0/1/2 (0x49 - 0x4B)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	-	R/W	-	-	-
Name	UP_LENGTH		CS DIV	Internal use	UP LEN EN	-	-	-
Default	0x06							
	0	0	0	0	0	1	1	0

Bit definitions:

- Bit 7-6: Up length select (requires **UP_LENGTH_EN = 1** for use)
  - 00: Up length = 0010
  - 01: Up length = 0110
  - 10: Up length = 1010
  - 11: Up length = 1110
- Bit 5: CS divider
  - 0: Normal CS cap size
  - 1: CS cap size 5 times smaller
- Bit 3: Up length select enable
  - 0: Up length select is disabled
  - 1: Up length select is enabled (value in bit 7-6 is used)

8.6.4.2 Inductive sensing

ProxFusion settings 3_0/1/2 (0x49 - 0x4B)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	-	R/W	-	R/W	-	-	-
Name	-		CS DIV	Internal use	-	-	-	-
Default	0x06							
	0	0	0	0	0	1	1	0

Bit definitions:

- Bit 5: CS divider
  - 0: Normal CS cap size
  - 1: CS cap size 5 times smaller

8.7 ProxFusion sensor settings block 1

12.1.1 ProxFusion settings 4

8.7.1.1 Capacitive sensing

ProxFusion settings 4 (0x50)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SAR UIs		TWO SIDED EN	ACF DISABLE	LTA BETA		ACF BETA	
Default	0x00							
	0	0	0	0	0	0	0	0

Bit definitions:

- Bit 7-6: SAR UIs
  - 00: Three channel discreet UI (multi-purpose sensing possibilities).
  - 01: Two channel SAR proximity / touch / deep touch.
  - 10: Single channel SAR (ch0) & Movement (ch1) UI enabled.
  - 11: Same as '10' with hysteresis features on unused channel 2.
- Bit 5: Two-sided detection
  - 0: Bidirectional detection disabled
  - 1: Bidirectional detection enabled
- Bit 4: Disable AC filter
  - 0: AC filter enabled
  - 1: AC filter disabled
- Bit 3-2: Long term average beta value
  - 00: 7
  - 01: 8
  - 10: 9
  - 11: 10
- Bit 1-0: AC filter beta value
  - 00: 1
  - 01: 2
  - 10: 3
  - 11: 4

8.7.1.2 Inductive sensing

ProxFusion settings 4 (0x50)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	UI selection		TWO SIDED EN	ACF DISABLE	LTA BETA		ACF BETA	
Fixed	0x20							
	0	0	1	0	0	0	0	1

Bit definitions:

- Bit 7: UI selection
  - 00: Two channel proximity / touch UI (multi-purpose)
  - 01: Hysteresis options available on dedicated channel
  - 10: Single channel SAR proximity / touch / movement UI is enabled
  - 11: Single channel SAR with hysteresis on dedicated channel.
- Bit 5: Two-sided detection
  - 0: Bidirectional detection disabled
  - 1: Bidirectional detection enabled

- Bit 4: Disable AC filter
  - 0: AC filter enabled
  - 1: AC filter disabled
- Bit 3-2: Long term average beta value
  - 00: 7
  - 01: 8
  - 10: 9
  - 11: 10
- Bit 1-0: AC filter beta value
  - 00: 1
  - 01: 2
  - 10: 3
  - 11: 4

12.1.2 ProxFusion settings 5

IQS620A software number 0x08 = D'08 (Firmware version 1):

ProxFusion settings 5 (0x51)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	-	-	-	-	-	-	-
Name	Disable Ch1 auto	Internal use						
Default	0x01							
	0	0	0	0	0	0	0	1

Bit definitions:

- Bit7: Disable Ch1 auto
  - 0: Ch1 is automatically enabled and disabled when SAR UI is active
  - 1: Ch1 is manually enabled or disabled when SAR UI is active
- Bit 6-0: Internal use

IQS620A software number 0x0D = D'13 (Firmware version 2):

ProxFusion settings 5 (0x51)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	-	-	-	-	-	-	-
Name	Disable Ch1 auto	Internal use	Disable fast debounce	Internal use				
Default	0x01							
	0	0	0	0	0	0	0	1

Bit definitions:

- Bit7: Disable Ch1 auto
  - 0: Ch1 is automatically enabled and disabled when SAR UI is active
  - 1: Ch1 is manually enabled or disabled when SAR UI is active
- Bit 6: Internal use
- Bit 5: Disable fast debounce
  - 0: Fast debounce active in NP & LP modes
  - 1: Fast debounce inactive in NP & LP modes
- Bit 4-0: Internal use

12.1.3 Compensation

Compensation Ch0/1/2 (0x52 - 0x54)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Compensation (7-0)							

Bit definitions:

- Bit 7-0: Compensation (7-0)
  - Lower 8-bits of the Compensation value.

12.1.4 Multipliers

Multipliers Ch0/1/2 (0x55-0x57)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Compensation (9-8)		Multiplier coarse		Multiplier fine			

Bit definitions:

- Bit 7-6: Compensation (9-8)
  - Upper 2-bits of the Compensation value.
- Bit 5-4: Multiplier coarse
  - 0-3: Coarse multiplier selection
- Bit 3-0: Multiplier fine
  - 0-15: Fine multiplier selection

8.8 ProxFusion UI settings

12.1.1 Prox threshold Ch0/1/2

Prox threshold Ch0/1/2 (0x60/0x62/0x64)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Prox threshold value							
Default	0x16 = D'22							
	0	0	0	1	0	1	1	0

Bit definitions:

- Bit 7-0: Prox threshold = Prox threshold value
  - 0-255: Prox threshold
  - Ch0 Prox threshold ignored when SAR UI is active. Use SAR prox threshold 0x74

12.1.2 Touch threshold Ch0/1/2

Touch threshold Ch0/1/2 (0x61/0x63/0x65)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Touch threshold value							
Default	0x25 = D'37							
	0	0	1	0	0	1	0	1

Bit definitions:

- Bit 7-0: Touch threshold = Touch threshold value * LTA/ 256
  - 0-255*LTA/256: Touch threshold

12.1.3 ProxFusion discrete UI halt time

ProxFusion discrete UI halt time (0x66)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ProxFusion discrete UI halt time							
Default	0x28 = D'40 = 20sec							
	0	0	1	0	1	0	0	0

Bit definitions:

- Bit 7-0: Halt time in 500ms increments (decimal value x 500ms)
  - 0-127sec: ProxFusion discrete UI halt time
  - 0xFF = 255: Never halt

8.9 Single channel SAR UI settings

12.1.1 Single channel SAR UI settings 0

SAR UI settings 0 (0x70)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Fast mov beta	QRD Beta			SAR to GPIO0	Slow mov beta		
Default	0x16							
	0	0	0	1	0	1	1	0

Bit definitions:

- Bit 7: Fast movement detection filter beta
  - 0: beta = 0
  - 1: beta = 3
- Bit 6-4: Quick Release Detection Beta
  - 0-7: Quick Release Detection filter beta value
- Bit 3: SAR Standoff State to GPIO0
  - 0: SAR standoff state to GPIO0 not active. RDY on GPIO0
  - 1: SAR standoff state to GPIO0 active. No RDY signal. For IQS620 use recommended schematic as shown in Figure 8.2 or contact Azoteq for more information.
- Bit 2-0: Slow movement detection filter beta
  - 0-7: Slow movement filter beta value relative to fast beta

For use with IQS620 (pre-production version):

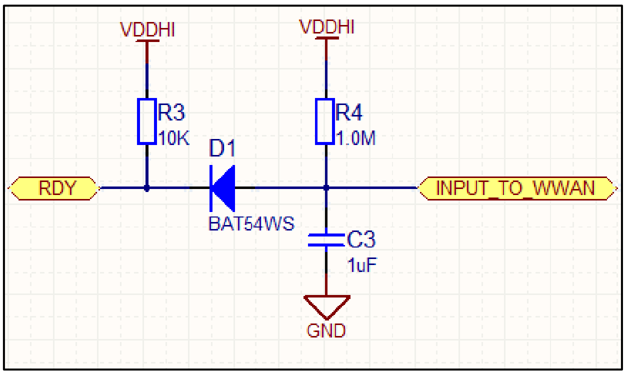


Figure 8.1 Recommended analog circuit when using GPIO0 output to drive a digital input (only required for IQS620). R4 and C3 Component values should be "select on test".

For use with IQS620A (production firmware version 1 & 2):

There is no need for any additional analog circuitry for the IQS620A part except for the standard pull-up resistor as indicated in the schematic reference design. GPIO0/RDY pin is configured as an open drain active low logic I/O.

12.1.2 Single channel SAR UI settings 1

SAR UI settings 1 (0x71)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	LTA halt timeout in no prox				Movement detection threshold			
Default	0x25							
	1sec				D’5			
	0	0	1	0	0	1	0	1

Bit definitions:

- Bit 7-4: LTA halt timeout in no prox
  - 0-15: LTA halt timeout in no prox in 500ms increments (decimal value * 500ms)
- Bit 3-0: Movement Detection Threshold
  - 0-15: Movement threshold = Movement threshold Value

12.1.3 Quick release detection threshold

Quick release detection threshold (0x72)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	QRD Threshold value							
Default	0x05							
	0	0	0	0	0	1	0	1

Bit definitions:

- Bit 7-0: 0-255: QRD threshold = QRD threshold value
  - With ProxFusion settings 5 (0x51): bit 7 = 0: QRD threshold of 0 will prevent the system from entering movement detection timeout mode
  - With ProxFusion settings 5 (0x51): bit 7 = 1: QRD threshold of 0 will immediately on SAR proximity enter movement detection timeout mode.

12.1.4 Single channel SAR filter halt threshold

SAR filter halt threshold (0x73)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SAR filter halt threshold value							
Default	0x16 = D'22							
	0	0	0	1	0	1	1	0

Bit definitions:

- Bit 7-0: SAR filter halt threshold = SAR filter halt threshold value
  - 0: Always halt
  - 1-255: SAR filter halt threshold

12.1.5 Single channel SAR prox threshold

SAR prox threshold Ch0 (0x74)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SAR prox threshold value							
Default	0x25 = D'37							
	0	0	1	0	0	1	0	1

Bit definitions:

- Bit 7-0: SAR prox threshold Ch0 = SAR prox threshold value
  - 0-255: SAR prox threshold Ch0

12.1.6 Quick release detection halt time

Quick release detection halt time (0x75)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	LTA halt timeout after a QRD (decimal value x 500ms)							
Default	0x28 = D'40 = 20sec							
	0	0	1	0	1	0	0	0

Bit definitions:

- Bit 7-0: LTA halt timeout after a Quick release detection with no movement afterwards (decimal value x 500ms)
  - 0x00 - 0xFE = 0 - 127 seconds: QRD halt timeout
  - 0xFF = 255 = Never time-out

8.10 Hysteresis UI settings

12.1.1 Hysteresis UI settings

Hysteresis UI settings (0x80)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	-	R/W	R/W	-	-	R/W	R/W
Name	-	-	Hysteresis T		-	-	Hysteresis P	
Default	0xA2							
	1	0	1	0	0	0	1	0

Bit definitions:

- Bit 5-4: Touch hysteresis
  - 00: Disabled
  - 01: 1/4 of threshold
  - 10: 1/8 of threshold
  - 11: 1/16 of threshold
- Bit 1-0: Prox hysteresis
  - 00: Disabled
  - 01: 1/4 of threshold
  - 10: 1/8 of threshold
  - 11: 1/16 of threshold

12.1.2 Hysteresis UI filter halt threshold

Hysteresis UI filter halt threshold (0x81)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Hysteresis UI filter halt threshold value							
Default	0x0A = D’10							
	0	0	0	0	1	0	1	0

Bit definitions:

- Bit 7-0: Hysteresis UI filter halt threshold.
  - 0: Always halt
  - 1-254: Hysteresis UI filter halt threshold

12.1.3 Hysteresis UI prox threshold

Hysteresis UI prox threshold (0x82)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Hysteresis UI prox threshold value							
Default	0x16 = D’22							
	0	0	0	1	0	1	1	0

Bit definitions:

- Bit 7-0: Hysteresis UI prox threshold
  - 0-255: Hysteresis UI prox threshold

12.1.4 Hysteresis UI touch threshold

Hysteresis UI touch threshold (0x83)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Hysteresis UI touch threshold value							
Default	0x25 = D'37 * 4 = 148							
	0	0	1	0	0	1	0	1

Bit definitions:

- Bit 7-0: Hysteresis UI touch threshold = Hysteresis UI touch threshold value * 4
  - 0-1020: Hysteresis UI touch threshold

8.11 Two channel SAR proximity / touch / deep touch UI settings

When implementing multiple threshold trigger thresholds, be sure.

12.1.1 2 Channel SAR UI settings

Hysteresis UI settings (0x80)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	-	R/W	R/W	-	-	R/W	R/W
Name	-	-	Hysteresis T		-	-	Hysteresis P	
Fixed Value	-	-	00		-	-	00	

Bit definitions:

- Bit 5-4: Touch hysteresis
  - 00: Disabled
- Bit 1-0: Prox hysteresis
  - 00: Disabled

12.1.2 SAR Antenna 1 (pin Cx0) proximity threshold

SAR Antenna 1 proximity threshold (0x60)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SAR antenna 1 proximity threshold value							

Bit definitions:

- Bit 7-0: SAR antenna 1 proximity threshold
  - 0-255: SAR antenna 1 proximity threshold

12.1.3 SAR Antenna 1 (pin Cx0) touch threshold

SAR Antenna 1 touch threshold (0x61)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SAR antenna 1 touch threshold value							

Bit definitions:

- Bit 7-0: Touch threshold = Touch threshold value * LTA/ 256
  - 0-255*LTA/256: SAR antenna 1 touch threshold

12.1.4 SAR Antenna 1 (pin Cx0) deep touch threshold

SAR Antenna 1 deep touch threshold (0x63)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SAR antenna 1 deep touch threshold value							

Bit definitions:

- Bit 7-0: Deep touch threshold = Deep touch threshold value * LTA/ 256
  - 0-255*LTA/256: SAR antenna 1 deep touch threshold

12.1.5 SAR antenna 2 (pin Cx1) proximity threshold

SAR antenna 2 proximity threshold (0x81)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SAR antenna 2 proximity threshold value							

Bit definitions:

- Bit 7-0: SAR antenna 2 proximity threshold.
  - 0-255: SAR antenna 2 proximity threshold

12.1.6 SAR antenna 2 (pin Cx1) touch threshold

SAR antenna 2 touch threshold (0x82)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SAR antenna 2 touch threshold value							

Bit definitions:

- Bit 7-0 SAR antenna 2 touch threshold
  - 0-255: SAR antenna 2 touch threshold

12.1.7 SAR antenna 2 (pin Cx1) deep touch threshold

SAR antenna 2 deep touch threshold (0x83)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SAR antenna 2 deep touch threshold value							

Bit definitions:

- Bit 7-0: SAR antenna 2 touch threshold = SAR antenna 2 deep touch threshold value * 4
  - 0-1020: SAR antenna 2 deep touch threshold

8.12 Hall-effect sensor settings

12.1.1 Hall-effect settings 0

Hall-effect settings 0 (0x90)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	-	R/W	R/W	-	-	R/W	R/W
Name	-	-	CHARGE FREQ		reserved		AUTO ATI MODE	
Default	0x03							
	0	0	0	0	0	0	1	1

Bit definitions:

- Bit 5-4: Charge frequency divider
  - 00: 1/2
  - 01: 1/4
  - 10: 1/8
  - 11: 1/16
- Bit 1-0: Auto ATI Mode
  - 00: ATI disabled
  - 01: Partial ATI (all multipliers are fixed)
  - 10: Semi-Partial ATI (only coarse multipliers are fixed)
  - 11: Full-ATI

12.1.2 Hall-effect settings 1

Hall-effect settings 1 (0x91)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ATI_BASE		ATI_TARGET (x32)					
Default	0x50							
	0	1	0	1	0	0	0	0

Bit definitions:

- Bit 7-6: Auto ATI base value
  - 00: 75
  - 01: 100
  - 10: 150
  - 11: 200
- Bit 5-0: Auto ATI Target
  - ATI Target is 6-bit value x 32

12.1.3 Compensation Ch4 & 5

Compensation Ch4 & 5 (0x92)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Compensation (7-0)							

Bit definitions:

- Bit 7-0: Compensation (7-0)
  - 7-0: Lower 8-bits of the Compensation value.

12.1.4 Multipliers Ch4 & 5

Multipliers Ch4 & 5 (0x93)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Compensation (9-8)		Multipliers coarse		Multipliers fine			

Bit definitions:

- Bit 7-6: Compensation (9-8)
  - 0-3: Upper 2-bits of the Compensation value.
- Bit 5-4: Multipliers coarse
  - 0-3: Coarse multiplier selection
- Bit 3-0: Multipliers fine
  - 0-15: Fine multiplier selection

8.13 Hall-effect switch UI settings

12.1.1 Hall-effect switch UI settings

Hall-effect switch UI settings (0xA0)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	-	Lin Mode	Hysteresis T		-	Swap Dir	Hysteresis P	
Default	0x00							
	0	0	0	0	0	0	0	0

Bit definitions:

- Bit 6: Linearize Output
  - 0: Disabled
  - 1: Enabled
- Bit 5-4: Touch Hysteresis
  - 00: Disabled
  - 01: 1/4 of threshold
  - 10: 1/8 of threshold
  - 11: 1/16 of threshold
- Bit 2: Swap field direction indication
  - 0: Disabled
  - 1: Enabled
- Bit 1-0: Proximity Hysteresis
  - 00: Disabled
  - 01: 1/4 of threshold
  - 10: 1/8 of threshold
  - 11: 1/16 of threshold

12.1.2 Hall-effect switch UI prox threshold

Hall-effect switch UI prox threshold (0xA1)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Prox threshold value							
Default	0x19 = D'25							
	0	0	0	1	1	0	0	1

Bit definitions:

- Bit 7-0: Hall-effect switch UI prox threshold = Prox threshold value
  - 0 – 255: Hall-effect switch UI prox threshold

12.1.3 Hall-effect switch UI touch threshold

Hall-effect switch UI touch threshold (0xA2)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Touch threshold value							
Default	0x19 =D'25							
	0	0	0	0	0	0	0	0

Bit definitions:

- Bit 7-0: Hall-effect switch UI touch threshold = Touch threshold value * 4
  - 0 – 1020: Hall-effect switch UI touch Threshold

8.14 Temperature UI settings

Please note for IQS620A: The temperature calibration multiplier and divider values have been increased to 8-bit and thus uses individual full byte registers located at addresses 0xC2 & 0xC3. The Temperature calibration offset have resultantly moved to address 0xC4.

12.1.1 Temperature UI settings

Temperature UI settings (0xC0)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	-	Reseed in prox	Reseed enable	Reseed threshold value				
Default	0x00							
	0	0	0	0	0	0	0	0

Bit definitions:

- Bit 6: Reseed in prox
  - 0: Reseed cannot occur during a prox
  - 1: Reseed can occur during a prox
- Bit 5: Reseed enable
  - 0: Disabled
  - 1: Enabled
- Bit 4-0: Reseed threshold
  - 0 - 32: Reseed threshold = Reseed threshold value

12.1.2 Multipliers Ch3

Multipliers Ch3 (0xC1)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	-	-	Multiplier coarse		Multiplier fine			
Default	0x00							
	0	0	0	0	0	0	0	0

Bit definitions:

- Bit 5-4: Multiplier coarse
  - 0-3: Coarse multiplier selection
- Bit 3-0: Multiplier fine
  - 0-15: Fine multiplier selection

For IQS620 only:

12.1.3 Temperature calibration data0

Temperature calibration data0 (0xC2)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W				R/W			
Name	Temperature multiplier value				Temperature divider value			
Default	0x00							
	0	0	0	0	0	0	0	0

Bit definitions:

- Bit 7-4: Temperature multiplier value +1
  - 1 – 16: Temperature multiplier
- Bit 3-0: Temperature divider value + 1
  - 1 – 16: Temperature divider

Please note: Do not use the value 0xFF (0xF? or 0x?F) as this will result in overflow(s).

12.1.4 Temperature calibration data1

Temperature calibration data1 (0xC3)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Temperature offset value							
Default	0x00							
	0	0	0	0	0	0	0	0

Bit definitions:

- Bit 7-0: Temperature offset constant = Temperature offset value
  - 0 – 255: Temperature offset constant

For IQS620A:

12.1.5 Temperature calibration multiplier

Temperature calibration multiplier (0xC2)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Temperature multiplier value							
Default	0x00							
	0	0	0	0	0	0	0	0

Bit definitions:

- Bit 7-0: Temperature calibration multiplier = Temperature multiplier value + 1
  - 1 – 256: Temperature calibration multiplier

Please note: Do not use the value 0xFF (D'255) as this will result in an overflow (255 + 1 = 256)

12.1.6 Temperature calibration divider

Temperature calibration divider (0xC3)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Temperature divider value							
Default	0x00							
	0	0	0	0	0	0	0	0

Bit definitions:

- Bit 7-0: Temperature calibration divider = Temperature divider value + 1
  - 1 – 256: Temperature calibration divider

Please note: Do not use the value 0xFF (D'255) as this will result in an overflow (255 + 1 = 256)

12.1.7 Temperature calibration offset

Temperature calibration offset (0xC4)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Temperature offset value							
Default	0x00							
	0	0	0	0	0	0	0	0

Bit definitions:

- Bit 7-0: Temperature offset constant = Temperature offset value
  - 0 – 255: Temperature offset constant

8.15 Device and power mode settings

12.1.1 System settings

System settings (0xD0)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	W=1	W=1	R/W	R/W	R/W	R/W	W=1	W=1
Name	SOFT RESET	ACK RESET	EVENT MODE	4MHz	COMMS ATI	ATI BAND	REDO ATI	RESEED
Default	0x08							
	0	0	0	0	1	0	0	0

Bit definitions:

- Bit 7: Software Reset (***Set only, will clear when done***)
  - 1: Causes the device to perform a WDT reset
- Bit 6: ACK Reset (***Set only, will clear when done***)
  - 1: Acknowledge that a reset has occurred. This event will trigger until acknowledged.
- Bit 5: Event mode enable
  - 0: Event mode disabled. Default streaming mode communication.
  - 1: Event mode communication enabled.
- Bit 4: Main Clock frequency selection
  - 0: Run FOSC at 16MHz
  - 1: Run FOSC at 4MHz
- Bit 3: Communications during ATI
  - 0: No communications are generated during ATI
  - 1: Communication continue as setup regardless of ATI state.
- Bit 2: Re-ATI Band selection
  - 0: Re-ATI when outside 1/8 of ATI target
  - 1: Re-ATI when outside 1/16 of ATI target
- Bit 1: Redo ATI on all channels (***Set only, will clear when done***)
  - 1: Redo the ATI on all channels
- Bit 0: Reseed all Long-term filters (***Set only, will clear when done***)
  - 1: Reseed all channels (irrespective of the channel reseed enable byte (0xDB) for IQS620A)

12.1.2 Active channels

Active channels (0xD1)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	-	-	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0
Default	0x3F							
	0	0	1	1	1	1	1	1

Bit definitions:

- Bit 5: Ch5 (***note: Ch4 & 5 must both be enabled for Hall-effect UI to be functional***)
  - 0: Channel is disabled
  - 1: Channel is enabled
- Bit 4: Ch4 (***note: Ch4 & 5 must both be enabled for Hall-effect UI to be functional***)
  - 0: Channel is disabled
  - 1: Channel is enabled
- Bit 3: Ch3 (***note: Ch3 must be enabled for temperature UI to be functional***

- 0: Channel is disabled
- 1: Channel is enabled

- Bit 2: Ch2 (***note: Ch2 must be enabled for Hysteresis UI to be functional***)
  - 0: Channel is disabled
  - 1: Channel is enabled
- Bit 1: Ch1 (***note: Ch0 and Ch1 must both be enabled for SAR UI to be functional***)
  - 0: Channel is disabled
  - 1: Channel is enabled
- Bit 0: Ch0 (***note: Ch0 and Ch1 must both be enabled for SAR UI to be functional***)
  - 0: Channel is disabled
  - 1: Channel is enabled

12.1.3 Power mode settings

Power mode settings (0xD2)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM OUT	EN ULP MODE	DSBL AUTO MODE	POWER MODE		NP SEG RATE		
Default	0x03							
	0	0	0	0	0	0	1	1

Bit definitions:

- Bit 7: PWM output activation
  - 0: PWM output inactive on GPIO3 (LTX available for use)
  - 1: PWM output active on GPIO3 (LTX disabled; no inductive sensing possible)
    - Please note: IQS620(A) will stay in normal power mode when the PWM output is active.
- Bit 6: Allow auto ultra-low power mode switching
  - 0: ULP is disabled during auto-mode switching
  - 1: ULP is enabled during auto-mode switching
- Bit 5: Disable auto mode switching
  - 0: Auto mode switching is enabled
  - 1: Auto mode switching is disabled
- Bit 4-3: Manually select power mode (***note: bit 5 must be set for static power modes***)
  - 00: Normal Power mode. The device runs at the normal power rate, all enabled channels and UIs will execute.
  - 01: Low Power mode. The device runs at the low power rate, all enabled channels and UIs will execute.
  - 10: Ultra-Low Power mode. The device runs at the ultra-low power rate, Ch0 is run as wake-up channel. The other channels execute at the NP-segment rate.
  - 11: Halt Mode. No conversions are performed; the device must be removed from this mode using an I^{2}C command.
- Bit 2-0: Normal power update rate
  - 000: ½ ULP rate
  - 001: ¼ ULP rate
  - 010: 1/8 ULP rate
  - 011: 1/16 ULP rate
  - 100: 1/32 ULP rate
  - 101: 1/64 ULP rate
  - 110: 1/128 ULP rate
  - 111: 1/256 ULP rate

12.1.4 Normal power mode report rate

Normal power mode report rate (0xD3)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Normal power mode report rate in ms							
Default	0x10 = D'16 = 16ms							
	0	0	0	1	0	0	0	0

Bit definitions:

- Bit 7-0: Normal mode report rate in ms (***note: LPOSC timer has +- 4ms accuracy***)
  - 0-255ms: Normal mode report rate

Please note: Report rates faster than 4ms can be delayed due to channel setup and comm speed.

12.1.5 Low power mode report rate

Low power mode report rate (0xD4)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Low power mode report rate in ms							
Default	0x30 = D'48 = 48ms							
	0	0	1	1	0	0	0	0

Bit definitions:

- Bit 7-0: Low-power mode report rate in ms (***note: LPOSC timer has +- 4ms accuracy***)
  - 0-255ms: Low-power mode report rate

12.1.6 Ultra-low power mode report rate

Ultra-low power mode report rate (0xD5)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Ultra-low power mode report rate value * 16ms							
Default	0x08 = D'08 * 16 = 128ms							
	0	0	0	0	1	0	0	0

Bit definitions:

- Bit 7-0: Ultra-low power mode report rate = Ultra-low power mode report rate value *16ms
  - 0-4080ms: Ultra-low power mode report rate

12.1.7 Auto mode timer

Auto mode timer (0xD6)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Auto mode timer value * 500ms							
Default	0x14 = D'20 * 500 = 10sec							
	0	0	0	1	0	1	0	0

Bit definitions:

- Bit 7-0: Auto modes switching time = Auto mode timer value * 500ms
  - 0-127.5s: Auto mode switching time

12.1.8 Global event mask

Global event mask (0xD7)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SAR ACTIVE	PMU EVENT	SYS EVENT	TEMP EVENT	HYSTE-RESIS UI EVENT	HALL EVENT	SAR EVENT	PROX SENSE EVENT
Default	0x00							
	0	0	0	0	0	0	0	0

Bit definitions:

- Bit 7: SAR activation state mask
  - 0: Event is allowed
  - 1: Event is masked
- Bit 6: Power management unit event mask
  - 0: Event is allowed
  - 1: Event is masked
- Bit 5: System event mask
  - 0: Event is allowed
  - 1: Event is masked
- Bit 4: Temperature event mask
  - 0: Event is allowed
  - 1: Event is masked
- Bit 4: Hysteresis UI event mask
  - 0: Event is allowed
  - 1: Event is masked
- Bit 2: Hall-effect event mask
  - 0: Event is allowed
  - 1: Event is masked
- Bit 1: SAR event mask
  - 0: Event is allowed
  - 1: Event is masked
- Bit 0: ProxSense event mask
  - 0: Event is allowed
  - 1: Event is masked

12.1.9 PWM duty cycle

PWM duty cycle (0xD8)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM duty cycle value							
Default	0x00							
	0	0	0	0	0	0	0	0

Bit definitions:

- Bit 7-0: PWM duty cycle (%) = (PWM duty cycle value + 1) / 256 * 100
  - 0.4 – 100%: PWM duty cycle of the fixed 1kHz PWM output available on GPIO3
  - Requires the activation of PWM OUT bit in Power mode settings 0xD2: bit7

For the IQS620A only:

12.1.10 RDY timeout period

RDY timeout period (0xD9)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RDY timeout period value							
Default	0x20 = D'32 * 0.32ms = 10.24ms							
	0	0	1	0	0	0	0	0

Bit definitions:

- Bit 7-0: RDY timeout period = RDY timeout period value * 0.32ms
  - 0 – 81.6ms: RDY timeout period

12.1.11 I²C settings

I²C settings (0xDA)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	R/W	-	-	-	-	-	-	R/W
Name	STOP DISABLE	Reserved						1
Default	0x01							
	0	0	0	0	0	0	0	1

Bit definitions:

- Bit 7: Stop disable
  - 0: Stop enabled: Stop bit will exit the communication window.
  - 1: Stop disabled: Stop bit will not exit the communication window. No start within the RDY timeout period (0xD9) will exit the communication window.
- Bit 6 – 1: Reserved
  - Do not configure, leave cleared.
- Bit 0: Reserved
  - Must always be set (bit 0 = 1).

12.1.12 Channel reseed enable

Channel reseed enable (0xDB)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	-	-	-	-	-	R/W	R/W	R/W
Name	-	-	-	-	-	Ch2	Ch1	Ch0
Default	0x07							
	0	0	0	0	0	1	1	1

Bit definitions:

- Bit 2-0: Channel reseed enable bit
  - 0: Channel reseed disabled
  - 1: Channel reseed enabled
  - Please note: This byte enables/disables only auto reseed commands upon either:
    - ProxFusion discrete UI halt timeout (0x66)
    - Quick release detection halt timeout (0x75)

9 Electrical characteristics

9.1 Absolute Maximum Specifications

The following absolute maximum parameters are specified for the device:
Exceeding these maximum specifications may cause damage to the device.

Table 9.1 Absolute maximum specification

Parameter	Absolute maximum
Operating temperature	-20°C to 85°C
Supply Voltage (VDDHI – GND)	3.6V
Maximum pin voltage	VDDHI + 0.5V (may not exceed VDDHI max)
Maximum continuous current (for specific Pins)	10mA
Minimum pin voltage	GND - 0.5V
Minimum power-on slope	100V/s
ESD protection	±8kV (Human body model)

9.2 Voltage regulation specifications

Table 9.2 Internal voltage regulator operating conditions

<table>
<tr><th>DESCRIPTION</th><th>CHIPSET</th><th>SYMBOL</th><th>MIN</th><th>TYPICAL</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>Supply voltage</td><td rowspan="2">IQS620</td><td>V_{DDHI}</td><td>2.0</td><td>-</td><td>3.3</td><td rowspan="4">V</td></tr>
<tr><td>Internal voltage regulator</td><td>V_{REG}</td><td>1.63</td><td>1.66</td><td>1.69</td></tr>
<tr><td>Supply voltage</td><td rowspan="2">IQS620A</td><td>V_{DDHI}</td><td>1.8</td><td>-</td><td>3.3</td></tr>
<tr><td>Internal voltage regulator</td><td>V_{REG}</td><td>1.63</td><td>1.66</td><td>1.69</td></tr>
</table>

9.3 Reset conditions

Table 9.3 Device reset specifications

DESCRIPTION	Conditions	PARAMETER	MIN	MAX	UNIT
Power On Reset	V_{DDHI} Slope ≥ 100V/s[1]	POR_{VDDHI}	0.3[2]	1.7	V
VDDHI Brown Out Detect	V_{DDHI} Slope ≥ 100V/s[1]	BOD_{VDDHI}	N/A	1.7	V
VREG Brown Out Detect	V_{DDHI} Slope ≥ 100V/s[1]	BOD_{VREG}	N/A	1.58[3]	V

[1]Applicable to full "operating temperature" range

[2]For a power cycle, ensure lowering V_{DDHI} below the minimum POR_{VDDHI} value before ramping V_{DDHI} past the maximum POR_{VDDHI} value

[3]In Figure 1.4 & Figure 1.5 capacitors C2 & C3 should be chosen to comply with this specification

9.4 I²C module specifications

Specified over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted).

Table 9.4 I²C module specifications

PARAMETER		TEST CONDITIONS	V_{DDHI}	MIN	TYP	MAX	UNIT
f_{SYS}	System clock frequency				16		MHz
f_{SCL}	SCL clock frequency		1.8V - 3V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	1.8V - 3V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	1.8V - 3V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		1.8V - 3V	0			ns
$t_{SU,DAT}$	Data setup time		1.8V - 3V	250			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	1.8V - 3V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
t_{SP}	Pulse duration of spikes suppressed by input filter	N/A	1.8V - 3V	No pulse suppression filter			ns
t_{LOW}	Clock low time-out	N/A	1.8V - 3V	TBD			ms

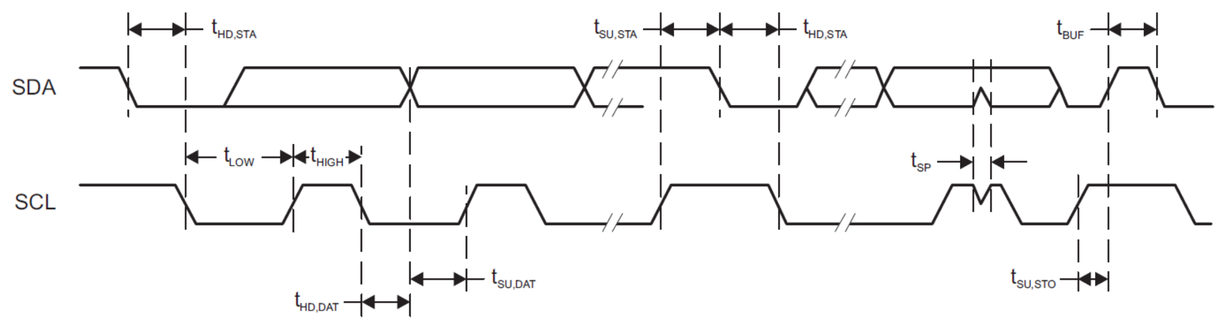


Figure 9.1 I²C mode timing

9.5 I²C module output logic fall time limits

Table 9.5 I²C module output logic fall time specifications

DESCRIPTION	VDDHI (V)	Temp (°C)	Pull-up resistor (Ω)	C_{LOAD} (pF)	SYMBOL	MIN	MAX	UNIT
SDA & SCL minimum fall times	1.8	-20	7000	50	T_{F_min}	11.80		ns
			885	400		28.70		
		+25	7000	50		11.80		
			885	400		30.70		
		+85	7000	50		11.80		
			885	400		33.80		
	3.3	-20	7000	50		7.90		
			885	400		18.60		
		+25	7000	50		11.80		
			885	400		30.70		
		+85	7000	50		11.80		
			885	400		33.80		
SDA & SCL maximum fall times	1.8	-20	420	50	T_{F_max}		42.50	
			420	400			65.10	
		+25	420	50			43.40	
			420	400			69.70	
		+85	420	50			45.30	
			420	400			77.30	
	3.3	-20	770	50			20.20	
			770	400			32.80	
		+25	770	50			19.90	
			885	400			34.30	
		+85	770	50			20.00	
			770	400			36.80	

9.6 I^2C module slew rates

Table 9.6 I^2C module fastest falling slew rates and matching rising slew rates

DESCRIPTION	VDDHI (V)	Conditions	Fall time (ns)	Rise time (ns)	SYMBOL	SR	UNIT
SDA & SCL slew rates for the minimum allowed bus capacitance	1.8	C_{BUS} = 50pF R_{PU} = 7kΩ T_A = -20°C	11.80		SR_{FALL}	61.02	$V/\mu s$
				296.55	SR_{RISE}	2.43	
	3.3	C_{BUS} = 50pF R_{PU} = 7kΩ T_A = -20°C	7.90		SR_{FALL}	167.09	
				296.55	SR_{RISE}	4.45	
SDA & SCL slew rates for the maximum allowed bus capacitance	1.8	C_{BUS} = 400pF R_{PU} = 885Ω T_A = -20°C	28.70		SR_{FALL}	25.09	
				299.94	SR_{RISE}	2.40	
	3.3	C_{BUS} = 400pF R_{PU} = 885Ω T_A = -20°C	18.60		SR_{FALL}	70.97	
				299.94	SR_{RISE}	4.40	

Table 9.7 I^2C module slowest falling slew rates and matching rising slew rates

DESCRIPTION	VDDHI (V)	Conditions	Fall time (ns)	Rise time (ns)	SYMBOL	SR	UNIT
SDA & SCL slew rates for the minimum allowed bus capacitance	1.8	C_{BUS} = 50pF R_{PU} = 420Ω T_A = +85°C	45.30		SR_{FALL}	15.89	$V/\mu s$
				17.79	SR_{RISE}	40.47	
	3.3	C_{BUS} = 50pF R_{PU} = 770Ω T_A = -20°C	20.20		SR_{FALL}	65.35	
				32.62	SR_{RISE}	40.47	
SDA & SCL slew rates for the maximum allowed bus capacitance	1.8	C_{BUS} = 400pF R_{PU} = 420Ω T_A = +85°C	77.30		SR_{FALL}	9.31	
				142.34	SR_{RISE}	5.06	
	3.3	C_{BUS} = 400pF R_{PU} = 770Ω T_A = +85°C	36.80		SR_{FALL}	35.87	
				260.96	SR_{RISE}	5.06	

9.7 I^2C pins (SCL & SDA) input/output logic levels

Table 9.8 I^2C pins (SCL & SDA) input and output logic level boundaries

DESCRIPTION	Conditions	SYMBOL	Temperature	MIN	TYP	MAX	UNIT
Input low level voltage	400kHz I^2C clock frequency	V_{in_LOW}	-20°C	32.12			% of VDDHI
			+25°C		34.84		
			+85°C			39.39	
Input high level voltage		V_{in_HIGH}	-20°C			71.51	
			+25°C		68.18		
			+85°C	66.06			
Output low level voltage		V_{out_LOW}	-20°C – +85°C		0		
Output high level voltage		V_{out_HIGH}	-20°C – +85°C		100		

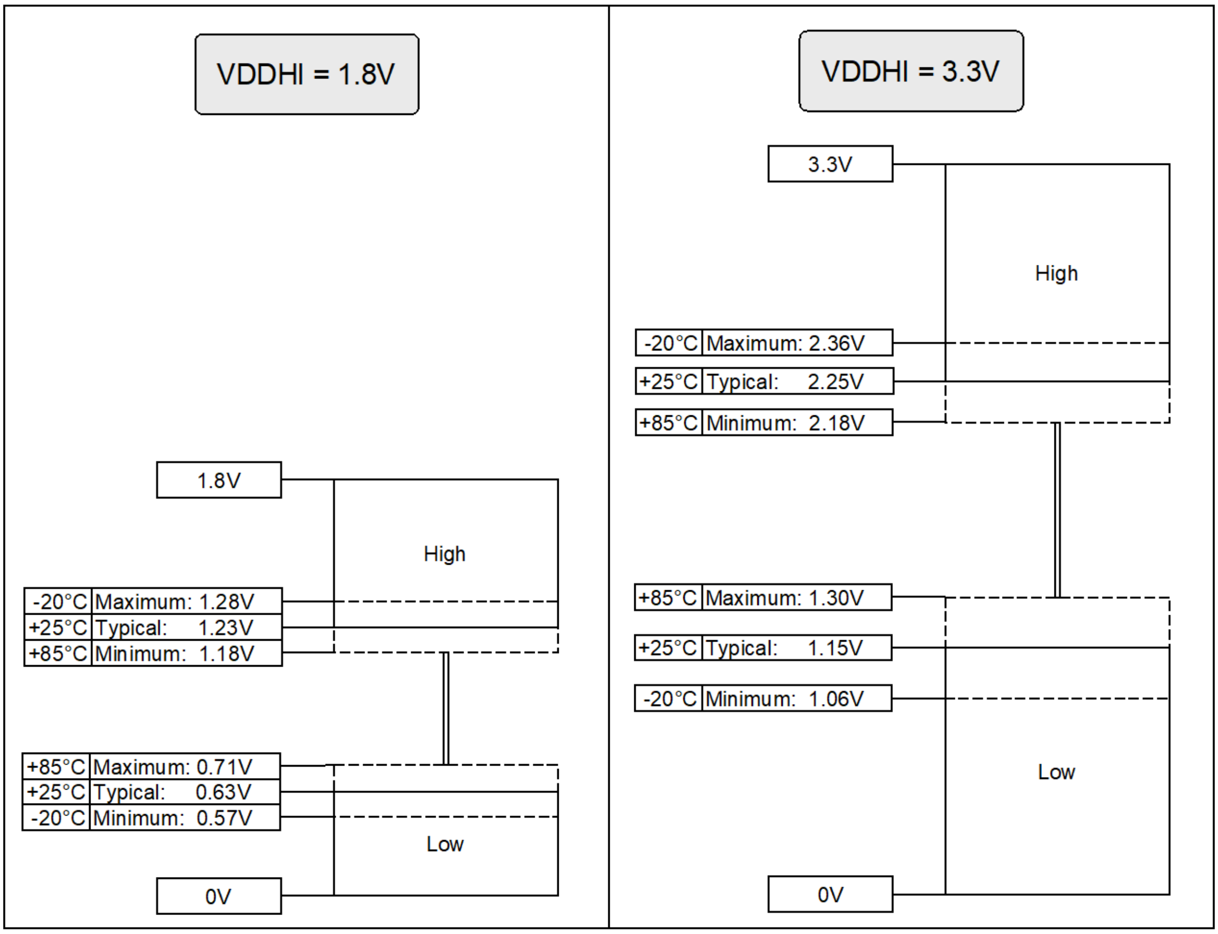


Figure 9.2 Calculated input buffer trigger levels for I^2C pins at 400kHz clock frequency for 1.8V and 3.3V VDDHI power supplies

9.8 General purpose digital output pins (GPIO0 & GPIO3) logic levels

DESCRIPTION	SYMBOL	Temperature	MIN	TYP	MAX	UNIT
Output low level voltage	V_{out_LOW}	-20°C – +85°C		0		% of VDDHI
Output high level voltage	V_{out_HIGH}	-20°C – +85°C		100		

9.9 Current consumptions

12.1.1 IC subsystems

Table 9.9 IC subsystem current consumption

Description	TYPICAL	MAX	UNIT
Core active	339	377	µA
Core sleep	0.63	1	µA

Table 9.10 IC subsystem typical timing

Power mode	Core active	Core sleep	Total	Unit
NP mode	5	5	10	ms
LP mode	5	43	48	ms
ULP mode	1.75	128	129.75	ms

12.1.2 Capacitive sensing alone

Table 9.11 Capacitive sensing current consumption

Power mode	Supply voltage	Report rate	TYPICAL	UNIT
NP mode	VDD = 2.0V	10ms	90.18	µA
	VDD = 3.3V	10ms	91.00	
LP mode	VDD = 2.0V	48ms	32.97	
	VDD = 3.3V	48ms	32.80	
ULP mode	VDD = 2.0V	128ms	11.69	
	VDD = 3.3V	128ms	11.35	

-These measurements where done on the default setup of the IC

Table 9.12 Single capacitive wake-up channel current consumption

Power mode	Supply voltage	Charging frequency	ATI target	Report rate	TYPICAL	UNIT
ULP mode	VDD = 2.0V	2MHz	192	256ms	2.23	µA
	VDD = 3.3V	2MHz	192	256ms	2.57	

-These measurements where done with enhanced settings for minimum current consumption for a single touch channel

12.1.3 Capacitive sensing with SAR UI active

Table 9.13 Capacitive sensing and SAR UI current consumption

Power mode	Supply voltage	Report rate	TYPICAL	UNIT
NP mode	VDD = 2.0V	10ms	75.34	µA
	VDD = 3.3V	10ms	75.43	
LP mode	VDD = 2.0V	48ms	27.76	
	VDD = 3.3V	48ms	27.37	
ULP mode	VDD = 2.0V	128ms	11.72	
	VDD = 3.3V	128ms	11.25	

-These measurements where done on the default setup of the IC

12.1.4 Temperature monitoring alone

Table 9.14 Temperature monitoring current consumption

Power mode	Supply voltage	Report rate	TYPICAL	UNIT
NP mode	VDD = 2.0V	10ms	68.87	µA
	VDD = 3.3V	10ms	69.08	
LP mode	VDD = 2.0V	48ms	24.60	
	VDD = 3.3V	48ms	24.10	
ULP mode	VDD = 2.0V	128ms	22.67	
	VDD = 3.3V	128ms	22.12	

-These measurements where done on the default setup of the IC

12.1.5 Hall-effect sensing alone

Table 9.15 Hall-effect current consumption

Power mode	Supply voltage	Report rate	TYPICAL	UNIT
NP mode	VDD = 2.0V	10ms	104.82	µA
	VDD = 3.3V	10ms	104.42	
LP mode	VDD = 2.0V	48ms	38.11	
	VDD = 3.3V	48ms	37.44	
ULP mode	VDD = 2.0V	128ms	N/A (1)	
	VDD = 3.3V	128ms	N/A (1)	

-These measurements where done on the default setup of the IC

(1) –It is not advised to use the IQS620(A) in ULP without capacitive sensing. This is due to the Hall-effect sensor being disabled in ULP.

12.1.6 Inductive sensing alone

Table 9.16 Inductive sensing current consumption

Power mode	Supply voltage	Report rate	TYPICAL	UNIT
NP mode	VDD = 2.0V	10ms	116.50 (1)	µA
	VDD = 3.3V	10ms	130.10 (1)	
LP mode	VDD = 2.0V	48ms	41.34 (1)	
	VDD = 3.3V	48ms	46.31 (1)	
ULP mode	VDD = 2.0V	128ms	N/A (2)	
	VDD = 3.3V	128ms	N/A (2)	

-These measurements where done on the default setup of the IC

(1) –Measurements where conducted with a recommended inductive coil layout.

(2) –It is not advised to use the IQS620(A) in ULP without capacitive sensing. This is due to the Inductive sensor UI channel being disabled in ULP.

12.1.7 Halt mode

Table 9.17 Halt mode current consumption

Power mode	Conditions	Report rate	TYPICAL	UNIT
Halt mode	VDD = 2.0V	None	1.6	µA
Halt mode	VDD = 3.3V		1.9	

9.10 Start-up timing specifications

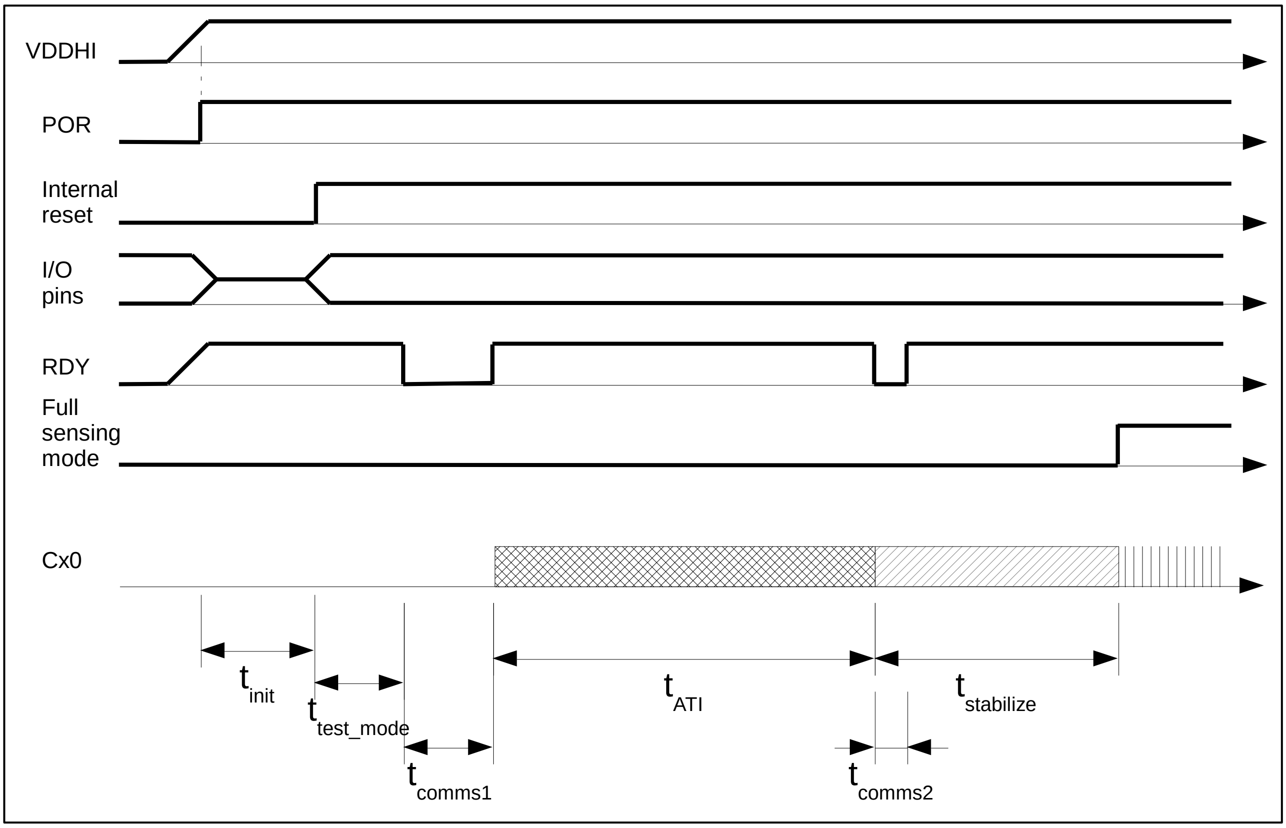


Figure 9.3 IQS620(A) start-up timing diagram

Table 9.18 Timing values for IQS620(A) start-up timing diagram

Timing	Min	Typical	Max
t_{init}		6ms	
t_{test_mode}		5ms	
$t_{comms1\ (16MHz)}$	until I^2C stop bit		10ms (time-out)
$t_{comms1\ (4MHz)}$	until I^2C stop bit		40ms (time-out)
$t_{ATI\ (16MHz)}$		110ms (default settings)	
$t_{ATI\ (4MHz)}$		420ms (default settings)	
t_{comms2} (event mode enabled – system event)	until I^2C stop bit		Time-out value defined in register 0xD9 (x4 for 4MHz mode)
$t_{stabilize\ (16MHz)}$	40ms	70ms (default settings)	
$t_{stabilize\ (4MHz)}$	120ms	140ms (default settings)	
$t_{full\_sensing\_mode\ (16MHz)}$		201ms (from POR)	
$t_{full\_sensing\_mode\ (4MHz)}$		611ms (from POR)	

10 Package information

10.1 DFN(3x3)-10 package and footprint specifications

Table 10.1 DFN(3x3)-10 Package dimensions (bottom)

Dimension	[mm]
A	3 ±0.1
B	0.5
C	0.25
D	n/a
F	3 ±0.1
L	0.4
P	2.4
Q	1.65

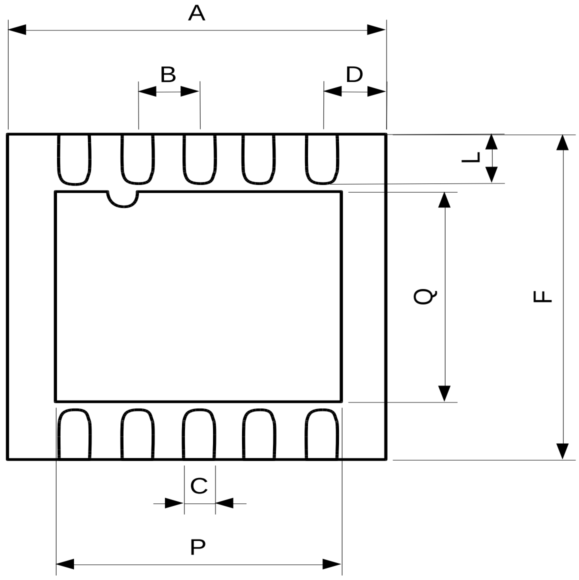


Figure 10.1 DFN(3x3)-10 Package dimensions (bottom view). Note that the saddle needs to be connected to common GND on the PCB.

Table 10.2 DFN(3x3)-10 Package dimensions (side)

Dimension	[mm]
G	0.05
H	0.65
I	0.7-0.8

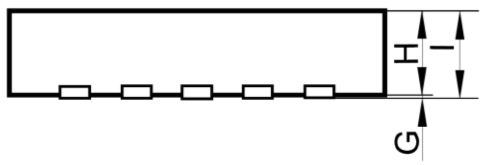


Figure 10.2 DFN(3x3)-10 Package dimensions (side view)

Table 10.3 DFN(3x3)-10 Landing pad dimensions

Dimension	[mm]
A	2.4
B	1.65
C	0.8
D	0.5
E	0.3
F	3.2

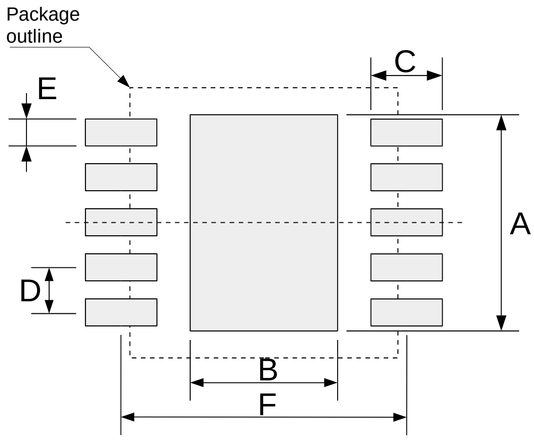
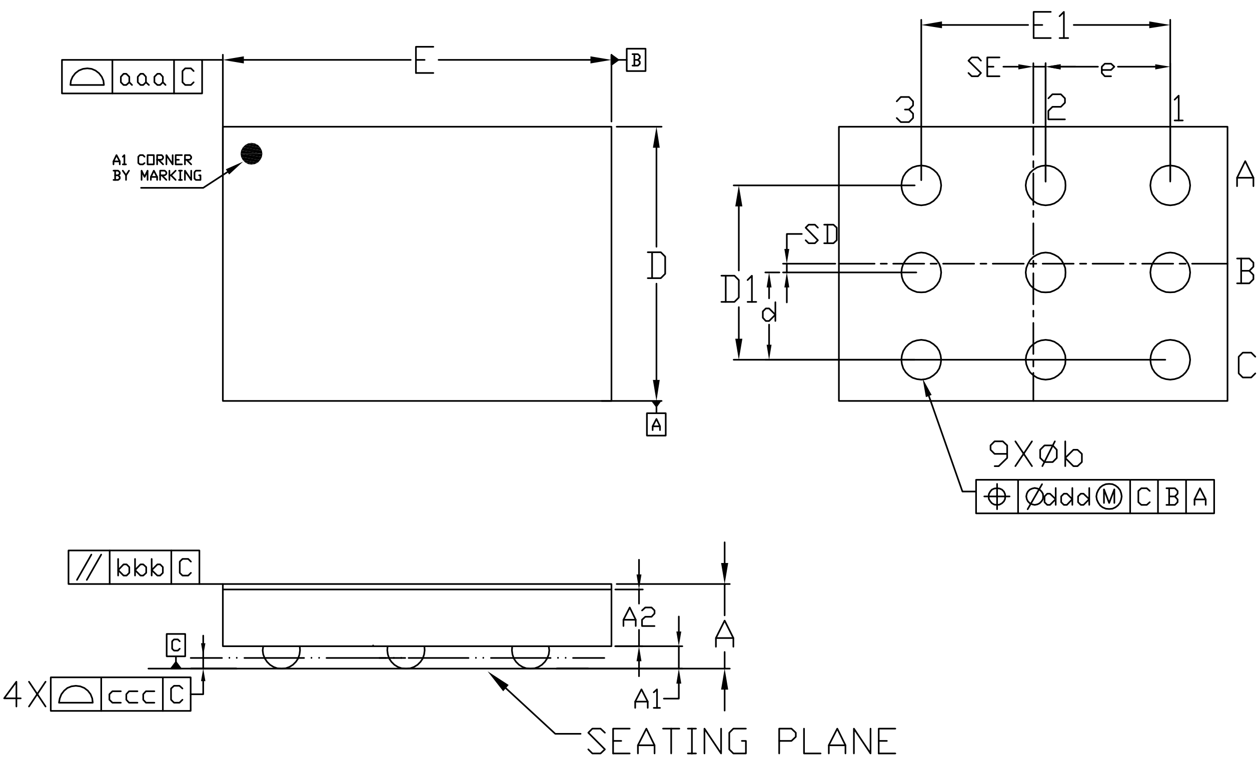


Figure 10.3 DFN(3x3)-10 Landing pad dimensions (top view)

10.2 WLCSP-9 package and footprint specification



Notes

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.300	0.340	0.380
A1	0.075	0.090	0.105
A2	0.205	0.230	0.255
D	1.055	1.070	1.085
E	1.515	1.530	1.545
D1	0.650	0.70	0.750
E1	0.950	1.000	1.050
b	0.135	0.160	0.185
d	0.350 BSC		
e	0.500 BSC		
SD	0.035		
SE	0.050		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Figure 10.4 IQS620A WLCSP-9 package dimensions

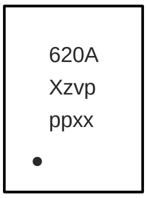
10.3 Device marking and ordering information

12.1.1 Device marking:

The devices can be identified from the top-side marking on the device package as shown below:

<table>
<tr><th colspan="2">DFN(3x3)-10</th></tr>
<tr><td>

Or

</td>
<td>IQS620A = Device name
X = Additional option ('Blank' = Default, T = temperature calibrated)
v = Firmware revision (0 – Pre-production, 1 – Production, 2 – FW update)
i = Industrial temperature range
z = Configuration (I²C address: 0 = 44H, 1 = 45H) [1]
P = Packaging house (1,2…)
WWYY = Date code (week, year)
● = Pin A1 indicator</td></tr>
<tr><th colspan="2">WLCSP-9</th></tr>
<tr><td>
</td>
<td>620A = device name (IQS620A)
X = Additional option (T = temperature calibrated)
z = Configuration (I²C address: 0 = 44H, 1 = 45H) [1]
v = Firmware revision (0 – Pre-production, 1 – Production, 2 – FW update)
ppp = Product code
xx = batch code (AA, AB …. ZZ)
● = Pin A1 indicator</td></tr>
</table>

[1] Other sub-address configurations are available on special request, see section 7.5.

12.1.2 Ordering information:

IQS620A	**X**	**z**	**pp**	**b**	
Device name	Additional option	Configuration (I^2C address)	Package type	Bulk packaging	
IQS620A		0	DN	R	**IQS620A0DNR**
		1			**IQS620A1DNR**
	T	0			**IQS620AT0DNR**
		1			**IQS620AT1DNR**
		0	CS		**IQS620A0CSR**
		1			**IQS620A1CSR**

X – Additional option
- 'Blank': Default device option
- T: Temperature calibrated (only used in order code for temperature calibrated DN parts; Any CS parts are temperature calibrated by default)

z – Configuration (I^2C address)
- 0: 44H default address
- 1: 45H sub-address

pp – Package type
- DN: DFN(3x3)-10
- CS: WLCSP-9

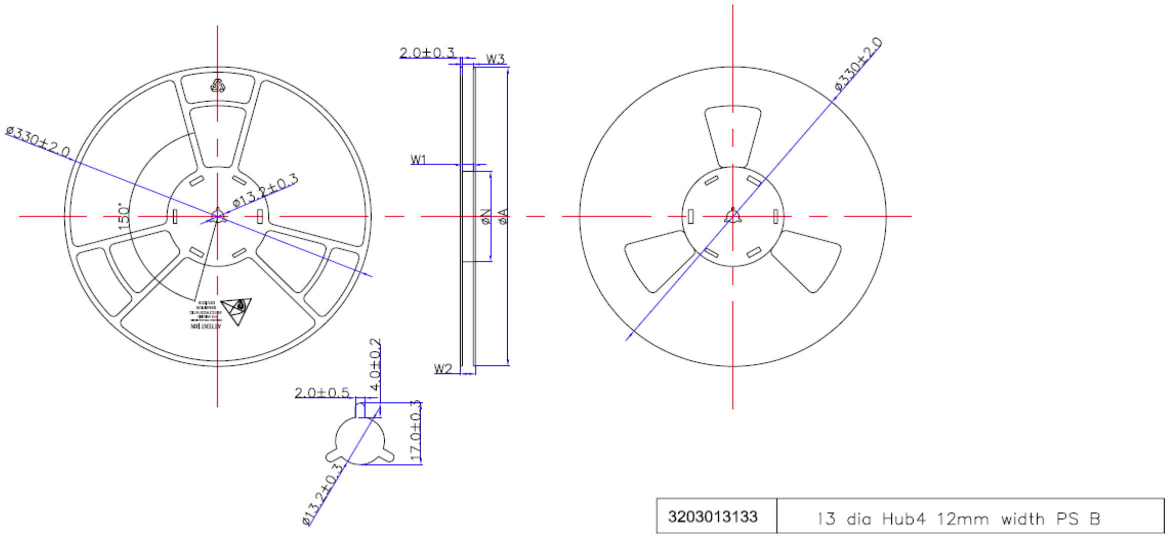
b – Bulk packaging
- R: Reel (3k/reel, MOQ=1 reel)

Example: **IQS620AT0DNR**
- **T** - Temperature calibrated
- **0** - configuration is default (44H default I^2C address)
- **DN** - DFN(3x3)-10 package
- **R** - packaged in reels of 3k (must be ordered in multiples of 3k)

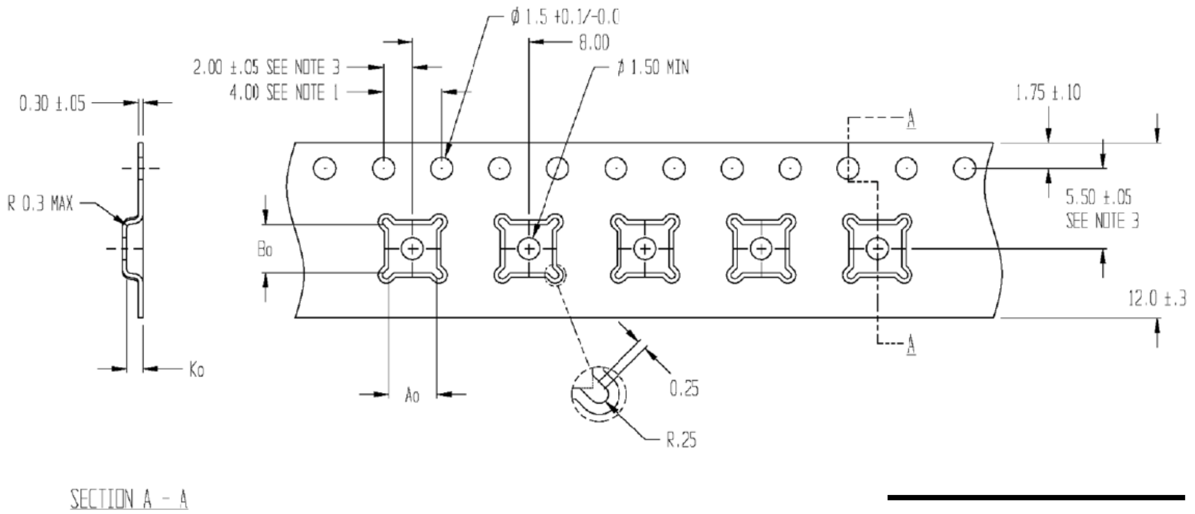
10.4 Tape and reel specification

12.1.1 DFN(3x3)-10

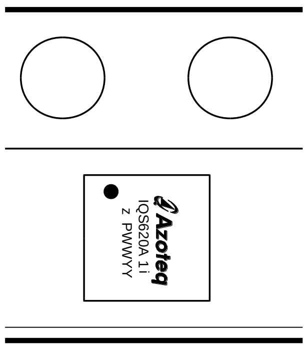
13” diameter reel, W = 12mm (width)



PRODUCT SPECIFICATIONS					
TYPE WIDTH	ØA	ØN	W1(Min)	W2(Max)	W3(Max)
12MM	330±2.0	100±1.0	12.4	18.4	15.4



A0=3.30
B0=3.30
K0=1.10

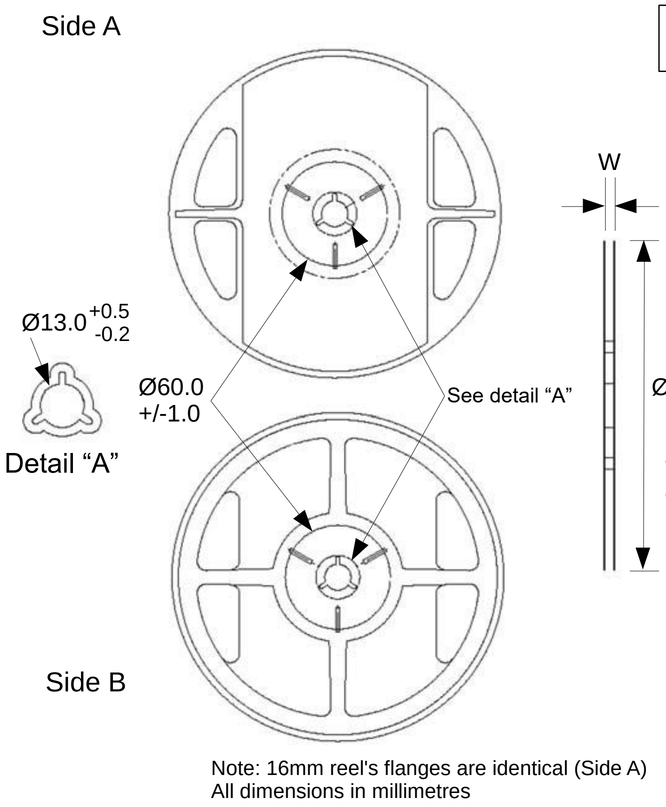


NOTES:
1、10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2、CAMBER IN COMPLIANCE WITH EIA 481
3、POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Figure 10.5 IQS620A DFN(3x3)-10 tape & reel specification

12.1.2 WLCSP-9

7" diameter reel, W = 8mm (width)



Property	Typical value	Test Method/Standard
Tensile strength	> 200 kg/cm²	ASTM D 638
Elongation	>= 30%	ASTM D 638
Flexural modulus	> 1.0 kg/cm²	ASTM D 790
Vicat softening	98° C	ASTM D 1525
Specific gravity	1.05 g/cc	ASTM D 792
Surface resistivity (Antistatic)	<= 10^{11} Ohms/square	ASTM D 257 Static dissipative per EIA541
Surface resistivity (Standard)	<= 10^{12} Ohms/square	ASTM D 257

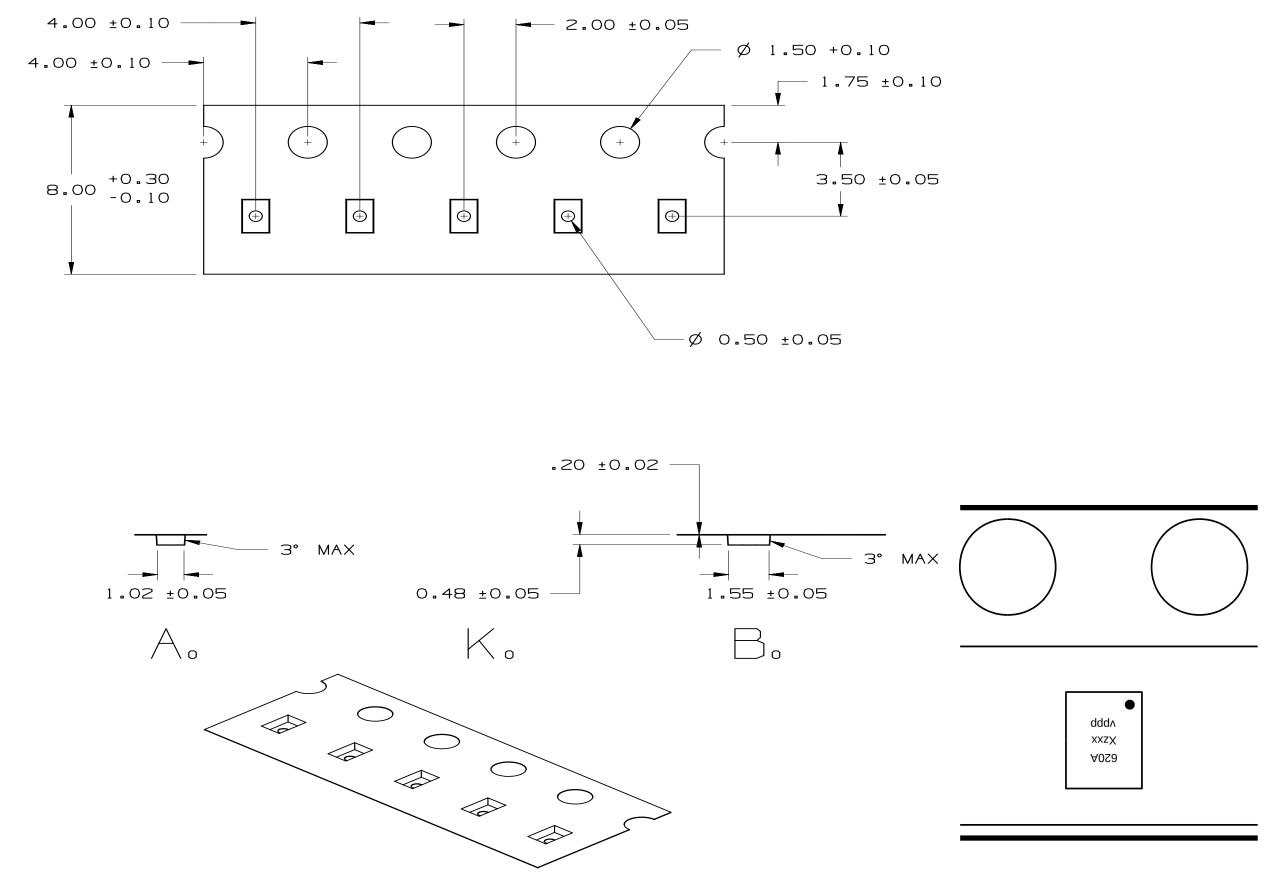


Figure 10.6 IQS620A WLCSP-9 tape & reel specification

10.5 MSL Level

Moisture Sensitivity Level (MSL) relates to the packaging and handling precautions for some semiconductors. The MSL is an electronic standard for the time period in which a moisture sensitive device can be exposed to ambient room conditions (approximately 30°C / 85%RH see J-STD033C for more info) before reflow occur.

Package	Level (duration)
DFN(3x3)-10	MSL 1 (Unlimited at ≤30°C / 85% RH) Reflow profile peak temperature < 260°C for < 25 seconds Number of reflows < 3
WLSCP-9	MSL 1 (Unlimited at ≤30°C / 85% RH) Reflow profile peak temperature < 260°C for < 25 seconds Number of reflows < 3

11 Datasheet revisions

11.1 Revision history

v1.00: – First release version
v1.10: – Datasheet update:
- I²C transaction detail added.
- Document navigational bookmarks added.

v1.11: – Datasheet update:
- IQS620A: 1.8V – 3.3V supply voltage range product addition.
- Device marking and ordering info updated.

v1.12: – Datasheet update:
- Metal detect UI changed to Hysteresis UI.
- Hysteresis UI described for both capacitive and inductive sensing options.
- Temperature sensing changed to Temperature monitoring. UI explanation altered.
- Temperature settings registers updated for IQS620A.
- IQS620A: RDY timeout period and I²C settings registers added (0xD9 & 0xDA).

v1.13: – Datasheet update:
- PWM duty cycle register definition updated.
- IQS620A: Channel reseed enable register (0xDB) added to memory map.

v1.14: – Datasheet update
- Two channel SAR UI option description added
- 3 Trigger level description added

v1.15: – Datasheet update
- Table 5.1 added for calibration value descriptions
- Register 0xC2 and 0xC3 ranges corrected (offset of 1; hex value of 0 = 1 used in equations)

v1.16: – Datasheet update
- Default register values added (hex and binary representation) for all memory map registers.

v1.17: – Datasheet update
- Device package clearance to MSL1. Specifications amended.

v1.18: – Datasheet update
- I²C stop-bit disable functionality explained. Section 7.4 added.

v1.19: – Datasheet update
- WLCSP-9 package detail added.

v1.20: – Datasheet update
- WLCSP-9 pinout-corrected and naming changed to package convention standard.
- Voltage regulation specifications added (Table 9.2).

v1.21: – Datasheet update
- WLCSP-9 package dimensions corrected.
- ProxFusion® updated to registered trademark.

v1.22: – Datasheet update
- Hall-effect sensing operational range confirmed and updated to 10mT – 200mT.
- Section 1.5 ProxFusion® Sensitivity added for ATI algorithm explanation.
- Section 9.4 & 9.6 added: I²C module fall times and slew rates.
- Section 9.7 updated and illustrated in additional Figure 9.2.
- Appendix B. Hall ATI added.

v1.23: – Datasheet update
- Section 9.10 added: Start-up timing specifications.
- Section 9.3 Reset conditions updated
- ESD protection certified to pass ±8kV (Human body model).
- WLCSP-9 tape and reel info added.
- Appendix A. Contact information updated.

v1.24 – Datasheet update
- General language and description improvements.
- General document editing.
- WLCSP-9 flip chip process mentioned for Hall-effect field orientation warning.
- Ultra low power mode description elaborated to include NP segment updates.

v1.25 – Datasheet update
- IQS620AT additional option in both DFN-10 & WLCSP-9 package options.
- Device firmware update version 2 added. Refer to bug fixes and additional features in errata section.
- Updated reference schematic and suggestions to include various ESD and EM noise suppression components.
- Device marking of DFN-10 & WLCSP-9 updated.
- Ordering code section updated to list all options.
- Errata section updated for firmware revisions
- Appendix A. Contact information updated.

11.2 Errata

12.1.1 Firmware version 0 (Device software number [0x01] = 0x04 = D'04)

Pre-production version release

12.1.2 Firmware version 1 (Device software number [0x01] = 0x08 = D'08)

Production version 1 release

12.1.3 Firmware version 2 (Device software number [0x01] = 0x0D = D'13)

Production firmware update version 2

Bug fixes:

- Temperature UI execution between ch4 & 5 changed to execute unconditionally whether channels are active or disabled.
- SAR UI clearing compensation value at maximum resolved.
- Auto mode timer (0xD6) = D'0 (0ms) or D'1 (500ms) immediately entering ULP mode, even if ULP mode is disabled, resolved.
- For halt timeout conditions, touch flag clearing resolved to occur immediately.
- Fast LTA limit calculation corrected.

Device feature additions:

- Fast debounce of channels 1 – 5 by removing report rate sleep time while in debounce. Active by default: Bit option added to ProxSettings5 [0x51] bit4: 0 = Fast debounce active in NP & LP mode; 1 = Fast debounce inactive in NP & LP modes.
- Floating gate option added to disable Hall-effect sensors (Ch4 & 5) permanently. Required for devices that operate at an absolute minimum supply voltage of 1.8V and require a 5% tolerance on the voltage supply source, not to exceed the maximum regulator load when VREG = 1.71V (absolute minimum). Bit option added to OTP bank0: bit7: 0 = Hall-effect sensors active; 1 = Hall-effect sensors disabled.

Appendix A. Contact information

	USA	Asia	South Africa
Physical Address	6507 Jester Blvd Bldg 5, suite 510G Austin TX 78750 USA	Rm1227, Glittery City Shennan Rd Futian District Shenzhen, 518033 China	1 Bergsig Avenue Paarl 7646 South Africa
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Tel	+1 512 538 1995	+86 755 8303 5294 ext 808	+27 21 863 0033
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Email	info@azoteq.com	info@azoteq.com	info@azoteq.com

Please visit www.azoteq.com for a list of distributors and worldwide representation.

Appendix B: Hall ATI

Azoteq's ProxFusion® Hall technology has ATI Functionality; which ensures stable sensor sensitivity. The ATI functionality is similar to the ATI functionality found in ProxSense® technology. The difference is that the Hall ATI requires two channels for a single plate.

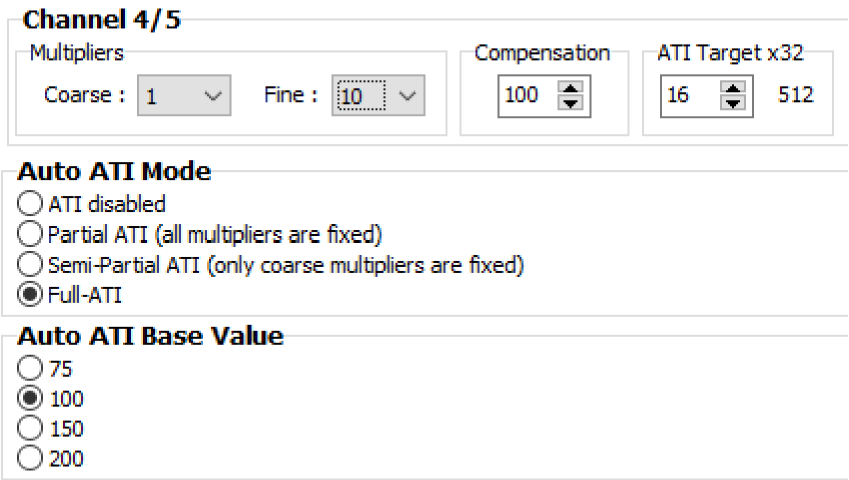
Using two channels ensures that the ATI can still be used in the presence of the magnet. The two channels are the inverse of each other, this means that the one channel will sense North and the other South. The two channels being inverted allows the capability of calculating a reference value which will always be the same regardless of the presence of a magnet.

12.1.4 Hall reference value:

The equation used to calculate the reference value, per plate:

$$Ref_n = \frac{1}{2 \cdot \left(\frac{1}{P_n} + \frac{1}{P_n'}\right)}$$

12.1.5 ATI parameters:



The ATI process adjusts three values (Coarse multiplier, Fine multiplier, Compensation) using two parameters per plate (ATI base and ATI target). The ATI process is used to ensure that the sensor's sensitivity is not severely affected by external influences (Temperature, voltage supply change, etc.).

12.1.6 Coarse and Fine multipliers:

In the ATI process the compensation is set to 0 and the coarse and fine multipliers are adjusted such that the counts of the reference value (Ref) are roughly the same as the ATI Base value. This means that if the base value is increased, the coarse and fine multipliers should also increase and vice versa.

12.1.7 ATI-Compensation:

After the coarse and fine multipliers are adjusted, the compensation is adjusted till the reference value (Ref) reaches the ATI target. A higher target means more compensation and therefore more sensitivity on the sensor.

The ATI process ensures that long term temperature changes, or bulk magnetic interference (e.g. the accidental placement of another magnet too close to the setup), do not affect the sensor's ability to detect the intended magnetic change.