

ISSUE 1; May 2016

Description

- The IQXV-89 is a very high performance VCXO delivering ultra low close-in phase noise for RF/Analog applications and ultra low RMS phase jitter optimised for high speed serial data and digital applications.
- Applications:
 - Communications
 - Ethernet
 - SONET/SDH
 - DSL/ADSL
 - Basestation
 - WiFi
 - WiMAX/WLAN
- Features:
 - Ultra Low Jitter 0.05 to 0.3 ps integrated 12kHz to 20MHz
 - Excellent close-in phase noise performance
 - CMOS, LVPECL, or LVDS Output options
 - Wide frequency range

Frequency Parameters

- Frequency 1.0MHz to 800.0MHz
- Frequency Stability $\pm 10.00\text{ppm}$ to $\pm 20.00\text{ppm}$
- Frequency Stability (including tolerance, temperature range, supply voltage variation, load variation and 15 years ageing at 25°C)

Electrical Parameters

- Supply Voltage Options:
 - 3.3V $\pm 10\%$
 - 2.5V $\pm 5\%$
- Supply Current:
 - CMOS 1 to 40mA max
 - LVPECL 40 to 120mA max
 - LVDS 30 to 80mA max

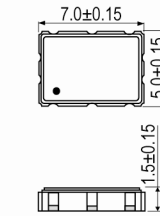
Frequency Adjustment

- Pulling $\pm 50\text{ppm}$ min APR
- Voltage Control:
 - Absolute Pull Range: (APR) $\pm 50\text{ppm}$ min
 - Total Pull Range: (Frequency shift from minimum to maximum control voltage): 100 to 250ppm max
 - Control Voltage (Nominal 1.65V): 0 to 3.3V
 - Linearity (Control voltage 0.3 to 3V): 10% max
 - Slope: Positive only
 - Modulation BW (Control voltage 0.3 to 3V): 15kHz min
 - Input Impedance: 0.1 to 10M Ω min

Operating Temperature Ranges

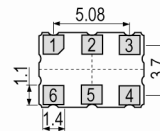
- -40 to 85°C

Outline (mm) 1.5mm package height



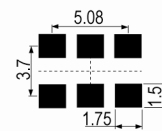
Pad Connections

1. Voltage Control
2. Enable/Disable or NC
3. GND
4. Output (CMOS)
5. Output (LVPECL/LVDS) or E/D or NC
6. +Vs

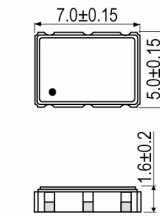


Underside View

Solder Pad Layout

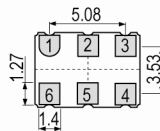


Outline (mm) 1.6mm package height



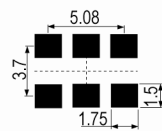
Pad Connections

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3. GND
4. Output (CMOS)
5. Output (LVPECL/LVDS) or E/D or NC
6. +Vs

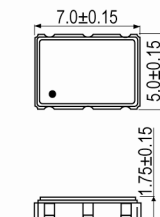


Underside View

Solder Pad Layout

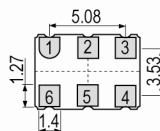


Outline (mm) = 1.75mm package height



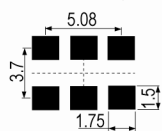
Pad Connections

1. Voltage Control
2. Enable/Disable or NC
3. GND
4. Output (CMOS)
5. Output (LVPECL/LVDS) or E/D or NC
6. +Vs



Underside View

Solder Pad Layout



Sales Office Contact Details:

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Output Details

- Output Compatibility CMOS/LVPECL/LVDS
- Output Characteristics (CMOS up to 200MHz):
Load: 10pF
Output Low (Vol): 10%Vs max
Output High (Voh): 90%Vs min
Duty Cycle @ 50% Vs: 45/55% max
R/F Time (@ 90%/10%): 3ns max
Phase Jitter (12kHz-20MHz): 0.05 to 0.3ps rms max
- Output Characteristics (LVPECL):
Load: 50Ω
Output Low (Vol): Vs-1.6V max
Output High (Voh): Vs-1.03V min
Duty Cycle (@ Vs-1.3V): 45/55% max
R/F Time (@ 80%/20%): 0.6ns max
Phase Jitter (12kHz-20MHz): 0.05 to 0.3ps rms max
- Output Characteristics (LVDS):
Load: 100Ω
Differential Output Voltage: 350mV
Duty Cycle (@ 1.25V): 45/55% max
R/F Time: 0.6ns max
Phase Jitter (12kHz-20MHz): 0.05 to 0.3ps rms max

Output Control

- Enable/Disable:
Logic '1' (70%Vs min) or no connection enables oscillator output
Logic '0' (30%Vs max) disables oscillator output

Noise Parameters

- Phase Noise (typ at 77.76MHz):
-73dBc/Hz @ 10Hz
-100dBc/Hz @ 100Hz
-128dBc/Hz @ 1kHz
-137dBc/Hz @ 10kHz
-148dBc/Hz @ 100kHz
- Phase Noise (typ at 122.88MHz):
-67dBc/Hz @ 10Hz
-98dBc/Hz @ 100Hz
-127dBc/Hz @ 1kHz
-147dBc/Hz @ 10kHz
-150dBc/Hz @ 100kHz

Environmental Parameters

- Shock: MIL-STD-883, Method 2002
- Storage Temperature Range: -55 to 125°C
- Humidity: after 48 hours at 85 °C ±2 °C 85 % relative humidity non-condensing
- Thermal Shock: MIL-STD-883, Method 1011
- Vibration: MIL-STD-883, Method 2007

Manufacturing Details

- Maximum Process Temperature: 260°C (40secs max)

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Ordering Information

- Frequency*
- Model*
- Output Type*
- Pad 2 function*
- Supply Voltage*
- Frequency Stability*
- Operating Temperature Range*
- (*minimum required)

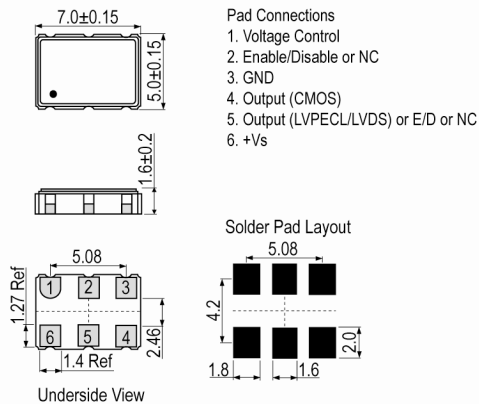
Compliance

- RoHS Status (2011/65/EU) Compliant
- REACH Status Compliant
- MSL Rating (JDEC-STD-033): Not Applicable

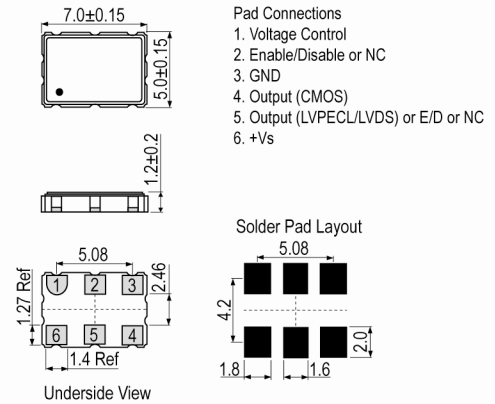
Packaging Details

- Pack Style: Bulk Loose in bulk pack
Pack Size: 1
- Pack Style: Reel Tape & reel in accordance with EIA-481-D
Pack Size: 2,000

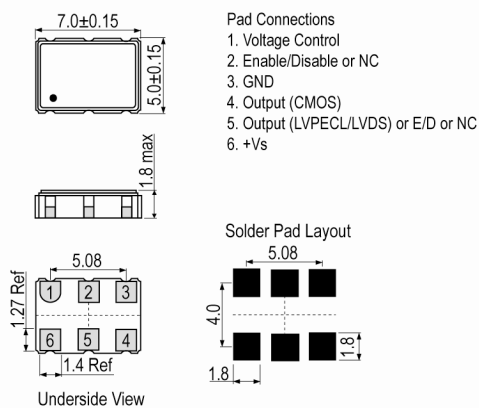
Outline (mm) = 1.6mm package height



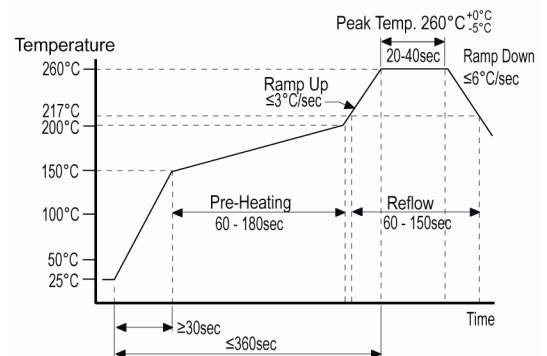
Outline (mm) = 1.2mm package height



Outline (mm) NONE = 1.8mm package height



Pb-Free Reflow



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Electrical Specification - maximum limiting values

Frequency Min	Frequency Max	Temperature Range	Stability (Min)	Current Draw	Rise and Fall Time	Duty Cycle
		°C	ppm	mA	ns	%
1.0MHz	800.0MHz	-40 to 85	-	-	-	-

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