International
IOR Rectifier

Data Sheet No. PD-6.075-G

IR01H(D)214 / IR01H(D)214-P2
IR01H(D)224 / IR01H(D)224-P2
IR01H(D)420 / IR01H(D)420-P2

HIGH VOLTAGE HALF BRIDGE

Features

- Output Power MOSFETs in half-bridge configuration
- 500V rated breakdown voltage
- High side gate drive designed for bootstrap operation
- Matched propagation delay for both channels
- Undervoltage lockout
- 5V Schmitt-triggered input logic
- Half-Bridge output in phase with HIN
- Heatsink version (P2) with improved P_D

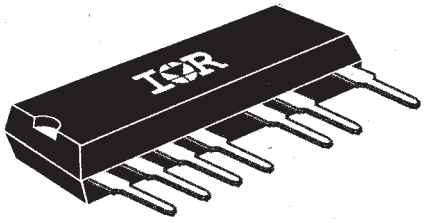
Description

The IR01H(D)xxx is a high voltage, high speed half bridge. Proprietary HVIC and latch immune CMOS technologies, along with the HEXFET power MOSFET technology, enable ruggedized single package construction. The logic inputs are compatible with standard CMOS or LSTTL outputs. The front end features an independent high and low side driver in phase with the logic compatible input signals. The output features two HEXFETs in a half-bridge configuration with a high pulse current buffer stage designed for minimum cross-conduction in the half bridge. Propagation delays for the high and low side power MOSFETs are matched to simplify use.

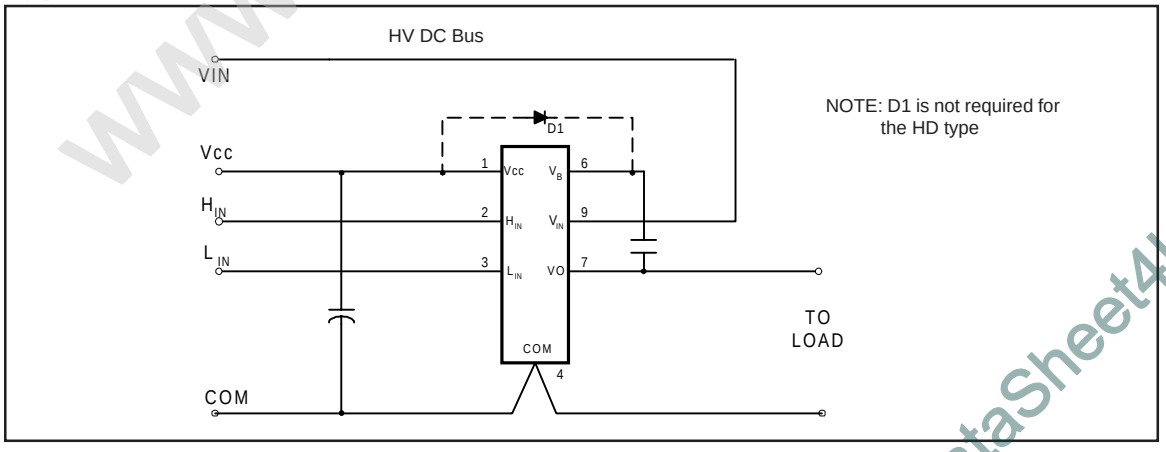
Product Summary

V_{IN} (max)	250V- 214/224 500V - 420
$t_{on/off}$	130 & 90 ns
t_{rr}	260 ns
$R_{DS(on)}$	2.0Ω - H214 1.1Ω - H224 3.0Ω - H420
$P_D(T_A = 25^oC)$	2.0W 4.0W - P2

Packages



Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_{IN}	High Voltage Supply	214/224	-0.3	250	V
		420	-0.3	500	
V_B	High Side Floating Supply Absolute Voltage	214/224	-0.3	275	
		420	-0.3	525	
VO	Half-Bridge Output		-0.3	V_{IN} + 0.3	
V_{IH}/V_{IL}	Logic Input Voltage (HIN & LIN)		- 0.3	V_{cc} + 0.3	
V_{CC}	Low Side and Logic Fixed Supply Voltage		-0.3	25	
dV/dt	Peak Diode Recovery dv/dt		—	3.50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25^oC$		—	2	W
		- P2		4.0	
R_{THJA}	Thermal Resistance, Junction to Ambient		—	60	$^oC/W$
		- P2		30	
R_{THJC}	Thermal Resistance, Junction to Case (heatsink)	- P2	—	20	
T_J	Junction Temperature		-55	150	^oC
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage		V_O + 10	V_O + 20	V
V_{IN}	High Voltage Supply	214/224	—	250	
		420	—	500	
V_O	Half-Bridge Output Voltage	214/224	(note 1)	250	
		420	—	500	
V_{CC}	Low Side and Logic Fixed Supply Voltage		10	20	
V_{IH}/V_{IL}	Logic Input Voltage (HIN & LIN)		0	V_{CC}	
T_A	Ambient Temperature		-40	125	°C
Id	Continuous Drain Current (TA = 25°C)	214	—	0.85	A
		214-P2	—	1.4	
		224	—	1.1	
		224-P2	—	1.9	
		420	—	0.7	
		420-P2	—	1.1	
	(TA = 85°C)	214	—	0.55	
		214-P2	—	0.9	
		224	—	0.7	
		224-P2	—	1.4	
		420	—	0.5	
		420-P2	—	0.8	
	(TC = 25°C)	214-P2	—	1.7	
		224-P2	—	2.3	
		420-P2	—	1.4	

Note 1: Logic operational for VO of -5 to 250V (214/224) and 500V (420).
Logic state held for V0 of -5 to $-V_B$

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. Switching time waveform definitions are shown in figure 2.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay (see note 2)	—	130	200	ns	Vs = 0V
t_{off}	Turn-Off Propagation Delay (see note 2)	—	90	200		Vs = 500V
t_r	Turn-On Rise Time (see note 2)	—	80	120		
t_f	Turn-Off Fall Time (see note 2)	—	40	70		
MT	Delay Matching, HS & LS Turn-On/Off	—	30	—		
t_{rr}	Reverse Recovery Time (MOSFET Body Diode)	—	260	—		I_F = 0.7A
Qrr	Reverse Recovery Charge (MOSFET Body Diode)	—	0.7	—	µC	di/dt = 100 A/us

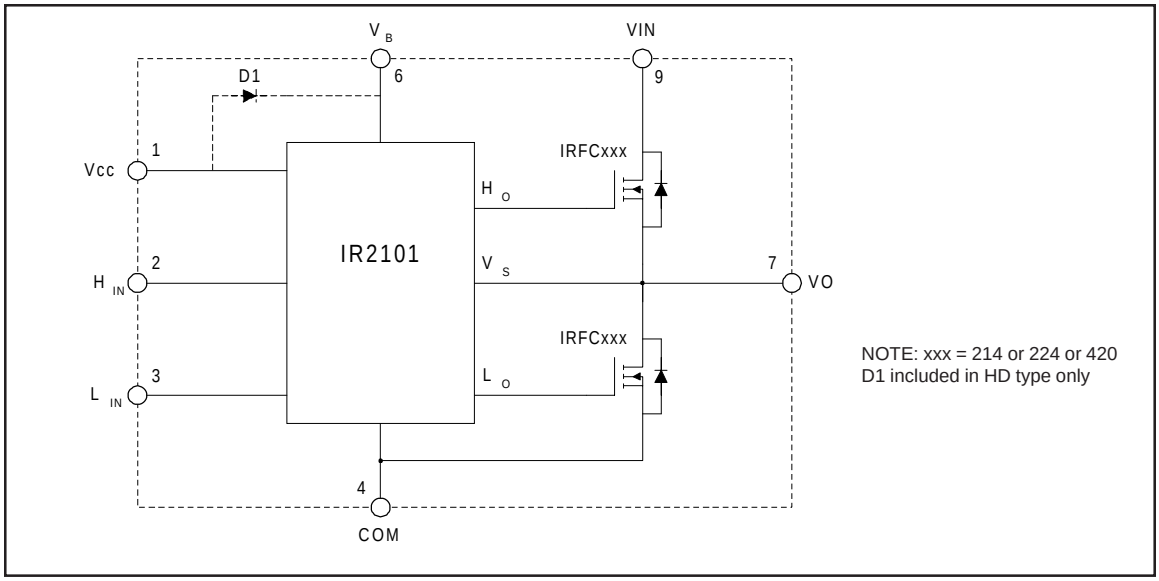
Note 2: Switching times as specified and illustrated in figure 2 are referenced to the MOSFET gate input voltage. This is shown as HO in figure 2.

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_B) = 15V and T_A = 25°C unless otherwise specified. The Input voltage and current levels are referenced to COM.

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold		8.8	9.3	9.8	V	
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold		7.5	8.2	8.6		
I_{QCC}	Quiescent V_{CC} Supply Current		—	140	240	µA	
I_{QBS}	Quiescent V_{BS} Supply Current		—	20	50		
I_{os}	Offset Supply Leakage Current		—	—	50		V_B = V_S = 500V
V_{IH}	Logic “1” Input Voltage		2.7	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” Input Voltage		—	—	0.8		
I_{IN+}	Logic “1” Input Bias Current		—	20	40	µA	
I_{IN-}	Logic “0” Input Bias Current		—	—	1.0		
Rds(on)	Static Drain-to-Source On-Resistance	214	—	2.0	—	Ω	Id=850mA/T_J=150°C
		224	—	1.1	—	Ω	Id=1.1A/T_J=150°C
		420	—	3.0	—	Ω	Id=700mA/T_J=150°C
VSD	Diode Forward Voltage	214/420	—	0.8	—	V	Id=700mA/T_J=150°C
		224	—	0.85	—		Id=1.1A/T_J=150°C

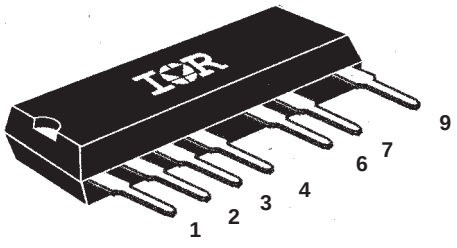
Functional Block Diagram



Lead Definitions

Symbol	Description
V_{CC}	Logic and internal gate drive supply voltage.
HIN	Logic input for high side Half Bridge output, in phase
LIN	Logic input for low side Half Bridge output, in phase
V_B	High side gate drive floating supply
V^+	High voltage supply
VO	Half Bridge output
COM	Logic and low side of Half Bridge return

Lead Assignments



1 V_{CC}
2 HIN
3 LIN
4 COM
6 V_B
7 VO
9 V_{IN}

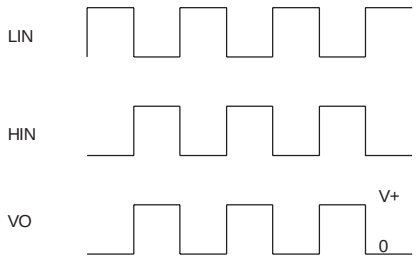


Figure 1. Input/Output Timing Diagram

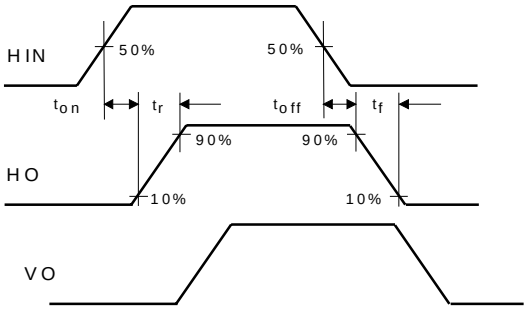


Figure 2. Switching Time Waveform Definitions

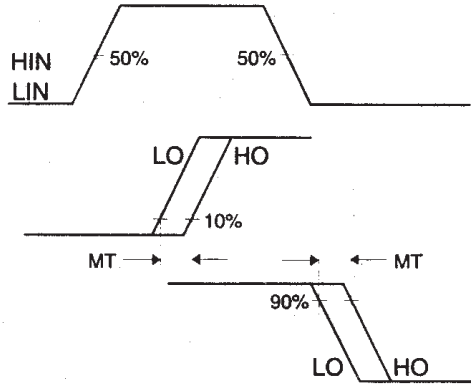


Figure 3. Delay Matching Waveform Definitions

IR01H(D)214 / IR01H(D)214-P2
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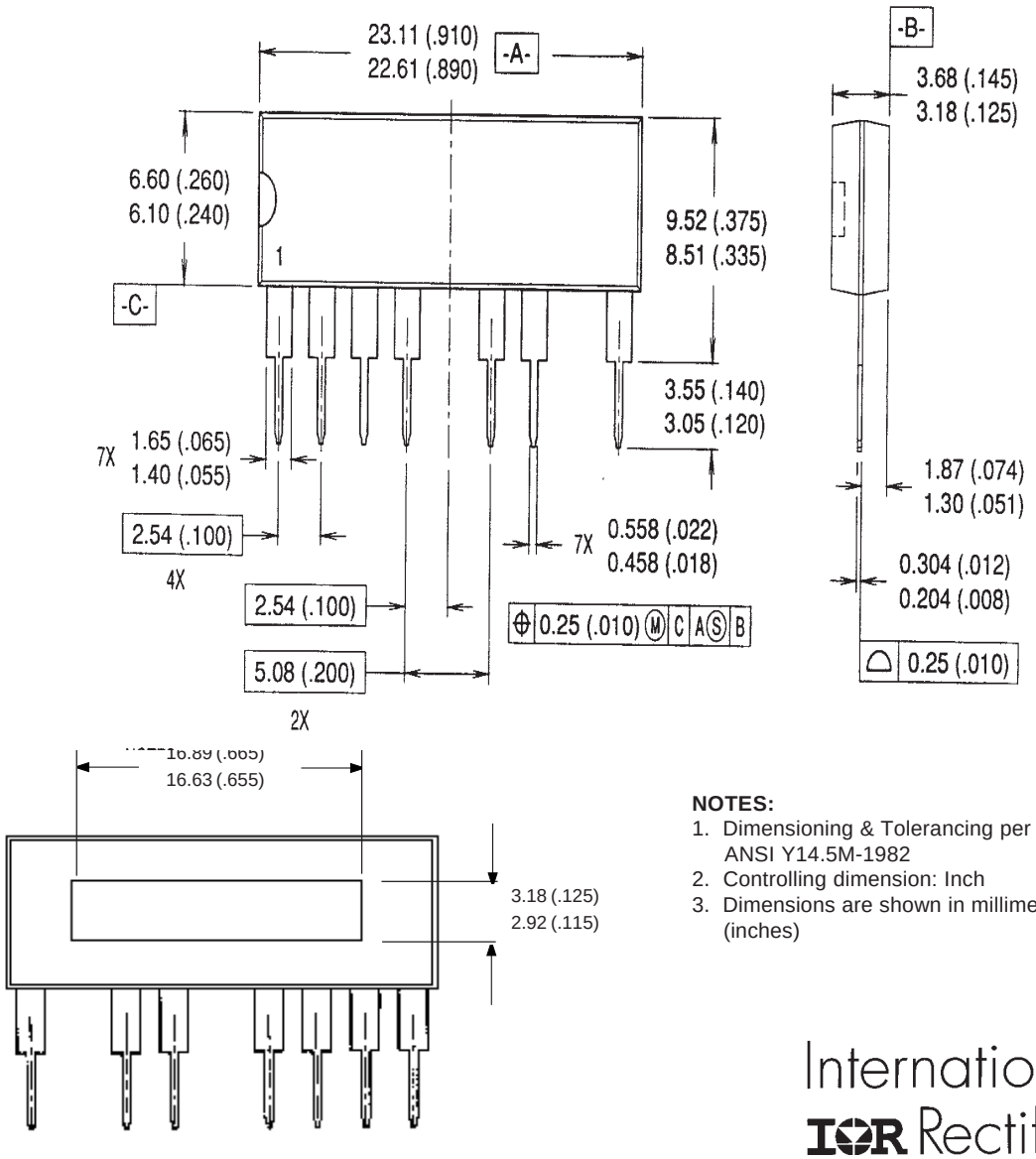
IR01H(D)420 / IR01H(D)420-P2



NOTES:

1. Dimensioning & Tolerancing per ANSI Y14.5M-1982
2. Controlling dimension: Inch
3. Dimensions are shown in millimeters (inches)

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