

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _B	High side floating supply voltage	-0.3	625	V	
V _S	High side floating supply offset voltage	V _B - 25	V _B + 25		
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3		
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3		
I _{OMAX}	Maximum allowable output current (either output) due to external power transistor miller effect	-500	500	mA	
V _{VCO}	Voltage controlled oscillator input voltage	-0.3	6.0	V	
I _{CPH}	CPH current	-5	5	mA	
V _{IPH}	IPH voltage	-0.3	5.5	V	
V _{DIM}	Dimming control pin input voltage	-0.3	5.5		
V _{MAX}	Maximum lamp power setting pin input voltage	-0.3	5.5		
V _{MIN}	Minimum lamp power setting pin input voltage	-0.3	5.5		
V _{CS}	Current sense input voltage	-0.3	5.5		
I _{SD}	Shutdown pin current	-5	5	mA	
I _{CC}	Supply current (note 1)	—	25		
dV/dt	Allowable offset voltage slew rate	-50	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	(16 pin DIP)	—	1.60	W
	P _D = (T _{JMAX} - T _A) / R _{thJA}	(16 pin SOIC)	—	1.25	
R _{thJA}	Thermal resistance, junction to ambient	(16 pin DIP)	—	75	°C/W
		(16 pin SOIC)	—	115	
T _J	Junction temperature	-55	150	°C	
T _S	Storage temperature	-55	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Note 1: This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6V (V_{CLAMP}). Please note that this supply pin should not be driven by a DC, low impedance power source greater than the diode clamp voltage (V_{CLAMP}) as specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V _{BS}	High side floating supply voltage	V _{CC} - 0.7	V _{CLAMP}	V
V _S	Steady state high side floating supply offset voltage	-1	600	
V _{CC}	Supply voltage	V _{CCUV+}	V _{CLAMP} (15.6)	
I _{CC}	Supply current	note 2	10	mA
V _{VCO}	VCO pin voltage	0	5	V
V _{DIM}	DIM pin voltage	0	5	
V _{MAX}	MAX pin current (note 3)	-750	0	μA
V _{MIN}	MIN pin voltage	1	3	V
R _{FMIN}	Minimum frequency setting resistance	10	100	kΩ
I _{SD}	Shutdown pin current	-1	1	mA
I _{CS}	Current sensing pin current	-1	1	
T _J	Junction temperature	-40	125	°C

Note 2: Enough current should be supplied into the VCC lead to keep the internal 15.6V zener clamp diode on this lead regulating its voltage, V_{CLAMP}.

Note 3: The MAX lead is a voltage-controlled current source. For optimum dim interface current mirror performance, this current should be kept between 0 and 750μA.

Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, V_{CS} = 0.5V, V_{SD} = 0.0V, R_{FMIN} = 40k, C_{VCO} = 10 nF, V_{DIM} = 0.0V, R_{MAX} = 33k, R_{MIN} = 56k, V_{C_{PH}} = 0.0V, C_{LO,HO} = 1000pF, T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Supply Characteristics						
V _{CCUV+}	V _{CC} supply undervoltage positive going threshold	12.0	12.5	13.0	V	
V _{CCCHYS}	V _{CC} supply undervoltage lockout hysteresis	1.5	1.6	1.7		
I _{QCCUV}	UVLO mode quiescent current	—	200	—	μA	V _{CC} = 10V SD=5V, CS=2V, or T _J > T _{SD}
I _{QCCFLT}	Fault-mode quiescent current	—	240	—		
I _{QCCFMIN}	V _{CC} supply current @ FMIN (IR2159)	—	5.6	—	mA	V _{VCO} = 0V
I _{QCCFMAX}	V _{CC} supply current @ FMAX (IR2159)	—	6.6	—		V _{VCO} = 5V
I _{QCCFMIN}	V _{CC} supply current @ FMIN (IR21591)	—	5.4	—		V _{VCO} = 0V
I _{QCCFMAX}	V _{CC} supply current @ FMAX (IR21591)	—	6.8	—		V _{VCO} = 5V
V _{CLAMP}	V _{CC} zener shunt clamp voltage	14.5	15.6	16.5	V	I _{CC} = 10mA

IR2159/IR21591 (S)

Electrical Characteristics (cont.)

$V_{CC} = V_{BS} = V_{BIAS} = 14V \pm 0.25V$, $V_{CS} = 0.5V$, $V_{SD} = 0.0V$, $R_{FMIN} = 40k$, $C_{VCO} = 10 \text{ nF}$, $V_{DIM} = 0.0V$, $R_{MAX} = 33k$, $R_{MIN} = 56k$, $V_{TPH} = 0.0V$, $C_{LO,HO} = 1000pF$, $T_A = 25^\circ C$ unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Floating Supply Characteristics						
I_{QBS0}	Quiescent V_{BS} supply current	—	0	—	μA	$V_{HO} = V_S$
I_{QBS1}	Quiescent V_{BS} supply current	—	30	—		$V_{HO} = V_B$
V_{BSMIN}	Minimum required V_{BS} voltage for proper HO functionality	—	4	5	V	
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
Oscillator I/O Characteristics						
f_{VCO}	VCO frequency range (IR2159) (See graph 3)	—	25	—	kHz	$V_{VCO}=0V$, $R_{FMIN}=39K\Omega$
		—	95	—		$V_{VCO}=5V$, $R_{FMIN}=10K\Omega$
f_{VCO}	VCO frequency range (IR21591) (See graph 4)	—	30	—		$V_{VCO}=0V$, $R_{FMIN}=68K\Omega$
		—	230	—		$V_{VCO}=5V$, $R_{FMIN}=10K\Omega$
d	Gate drive outputs duty cycle	—	50	—	%	$V_{VCO} = 0V$
V_{VCOFLT}	Fault-mode VCO pin voltage (UVLO, shutdown, over-current/temp.)	—	5	—	V	
I_{VCOPH}	Preheat mode VCO pin discharge current	—	1.0	—	μA	$V_{CPH} < 5V$
I_{VCODIM}	Dim mode VCO pin discharge current	—	16.0	—		
I_{VCOPK}	Amplitude control VCO pin charging current	—	60.0	—	μA	$V_{CPH} < 5V$, $V_{CS} > V_{IPH}$
t_{DTLO}	LO output deadtime (IR2159)	—	1.8	—	μs	
t_{DTHO}	HO output deadtime (IR2159)	—	1.8	—		
t_{DTLO}	LO output deadtime (IR21591)	—	1.0	—		
t_{DTHO}	HO output deadtime (IR21591)	—	1.0	—		
Gate Driver Output Characteristics						
V_{OL}	Low-level output voltage	—	—	100	mV	
V_{OH}	High-level output voltage	—	—	100		$V_{BIAS} - V_o$
t_r	Turn-on rise time	—	—	150	ns	
t_f	Turn-off fall time	—	—	100		

Electrical Characteristics (cont.)

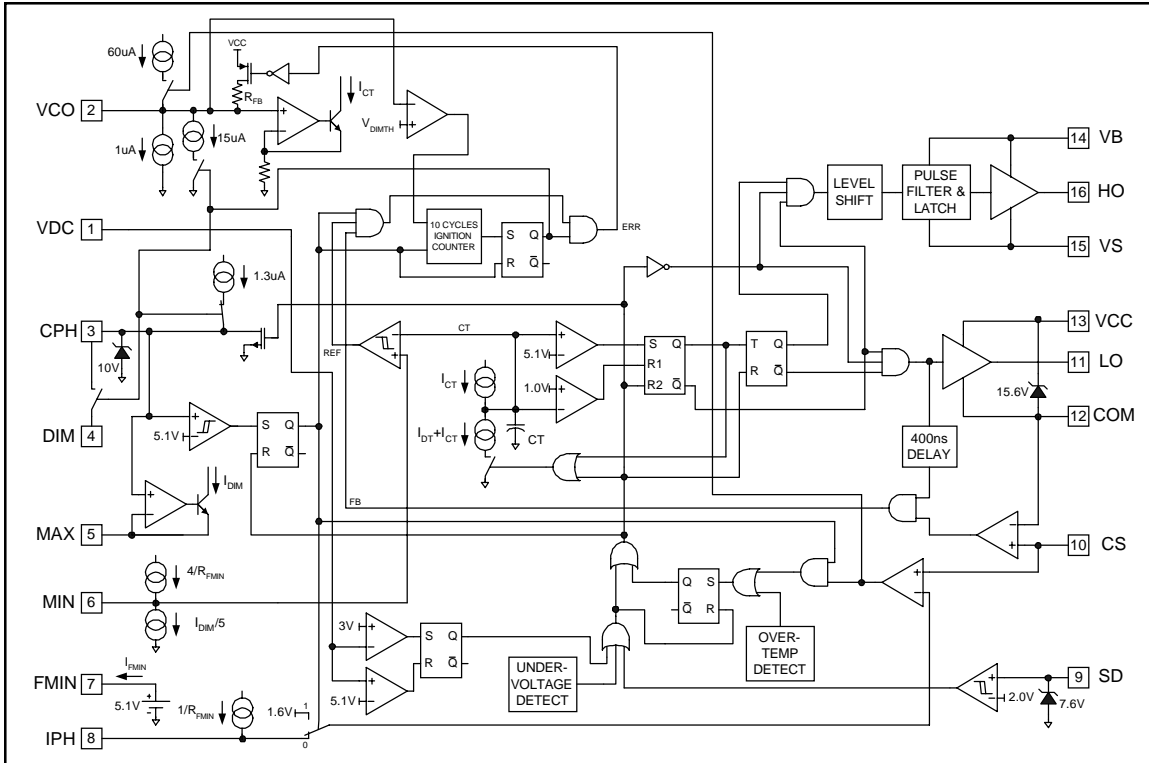
V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, V_{CS} = 0.5V, V_{SD} = 0.0V, R_{FMIN} = 40k, C_{VCO} = 10 nF, V_{DIM} = 0.0V, R_{MAX} = 33k, R_{MIN} = 56k, V_{TPH} = 0.0V, C_{LO,HO} = 1000pF, T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Preheat Characteristics						
ICPH	CPH pin charging current	—	1.3	—	μA	
VCPHIGN	CPH pin ignition mode threshold voltage	—	5.0	—	V	
VCPHCLMP	CPH pin clamp voltage	—	10	—		
IIPH	IPH pin DC source current	—	25.0	—	μA	IIPH = 1/R _{FMIN}
VCSTH	Peak preheat current regulation threshold	—	0.7	—	V	VCSTH = (IIPH) x (RIPH)
VCPHFLT	CPH pin voltage during UVLO or fault	—	0.0	—	V	SD = 5V, or CS = 2V, or T _j > T _{SD}
Ignition Characteristics						
VCSTH	Peak over current threshold	—	1.6	—	V	VCPH < 5V
Protection Characteristics						
VSDTH+	Rising shutdown pin threshold voltage	—	2.0	—	V	
VVDCTH+	Rising VDC pin threshold voltage	—	5.1	—		
VSDHYS	SD threshold hysteresis	—	150	—	mV	
VVDCHYS	VDC threshold hysteresis	—	2.1	—	V	
VSDCLMP	SD pin clamp voltage	—	7.6	—		ISD = 100mA
VCSTH	Peak over-current latch threshold voltage	—	1.6	—		VCPH > 5.1V
T _{SD}	Thermal shutdown junction temperature	—	165	—	°C	
Phase Control						
VCSTHZX	Zero-crossing threshold voltage	—	0.0	—	V	
R _{FB}	Phase control FB resistor (Internal)	—	5.7	—	kΩ	
t _{Blank}	Zero-crossing internal blank time	—	400	—	ns	
Dimming Interface						
VDIMOFF	DIM pin offset voltage	—	0.5	—	V	
VDIM	DIM pin input voltage range	0.0	—	5.0		
V _{MINMIN}	DIM minimum reference voltage (MIN pin)	—	1.0	—		V _{DIM} = 5V
V _{MINMAX}	DIM maximum reference voltage (MIN pin)	—	3.0	—		V _{DIM} = 0V
V _{DIMTH}	DIM mode VCO Threshold (IR2159)	—	0.5	3.0		
V _{DIMTH}	DIM mode VCO Threshold (IR21591)	—	1.1	3.0		
Minimum Frequency Setting						
V _{FMIN}	FMIN pin voltage during normal operation	—	5.1	—	V	
V _{FMINFLT}	FMIN pin voltage during fault mode	—	0.0	—	V	SD = 5V, or CS = 2V, or T _j > T _{SD}

IR2159/IR21591 (S)

International
IR Rectifier

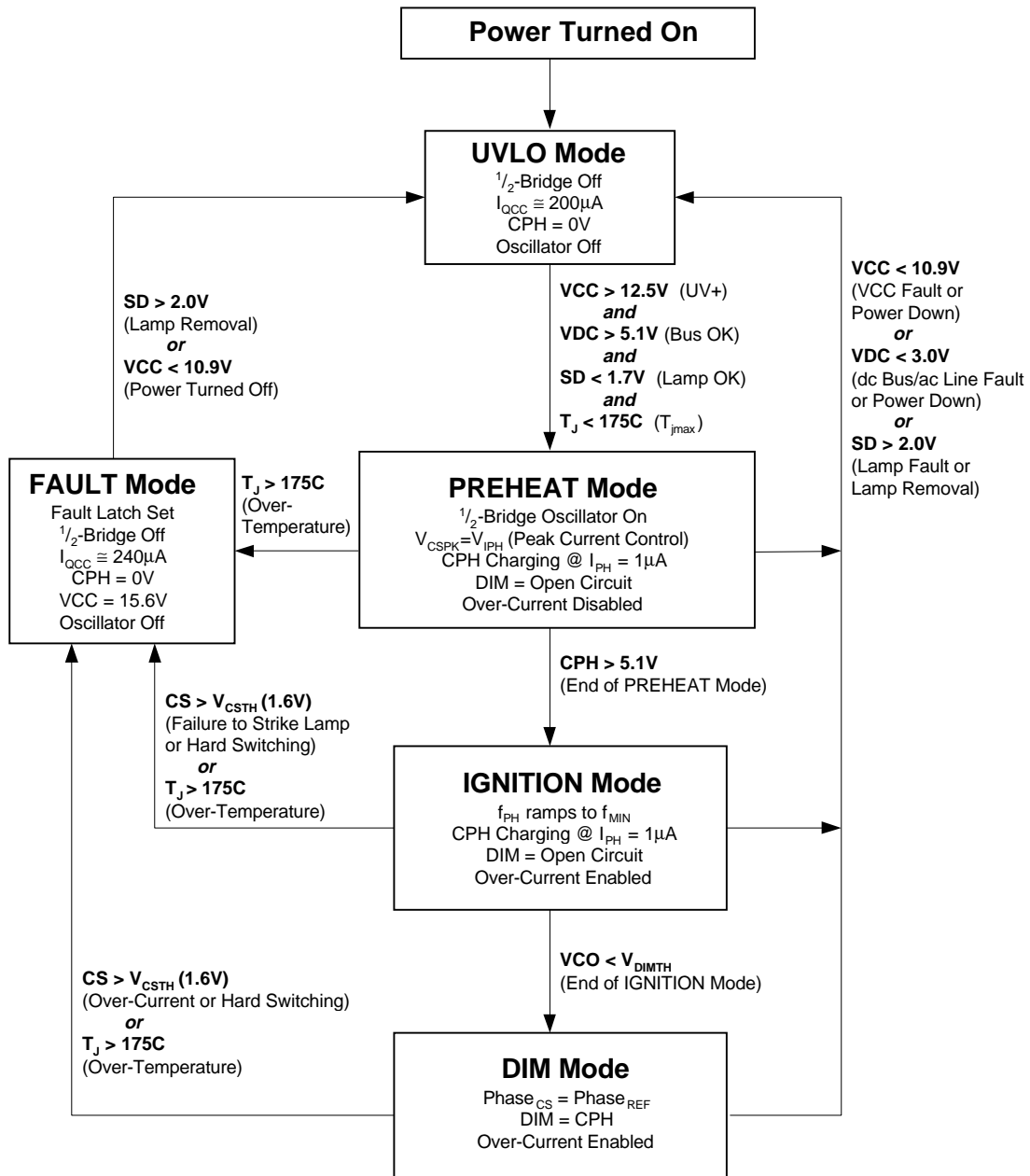
Block Diagram



Lead Assignments & Definitions

Pin Assignments		Pin #	Symbol	Description
VDC	1	16	HO	Line input voltage detection
VCO	2	15	VS	Voltage controlled oscillator Input
CPH	3	14	VB	Preheat timing input
DIM	4	13	VCC	0.5 to 5VDC dimming control input
MAX	5	12	COM	Maximum lamp power setting
MIN	6	11	LO	Minimum lamp power setting
FMIN	7	10	CS	Minimum frequency setting
IPH	8	9	SD	Peak preheat current reference
				Shutdown input
				Current sensing input
				Low-side gate driver output
				IC power & signal ground
				Logic & low-side gate driver supply
				High-side gate driver floating supply
				High voltage floating return
				High-side gate driver output

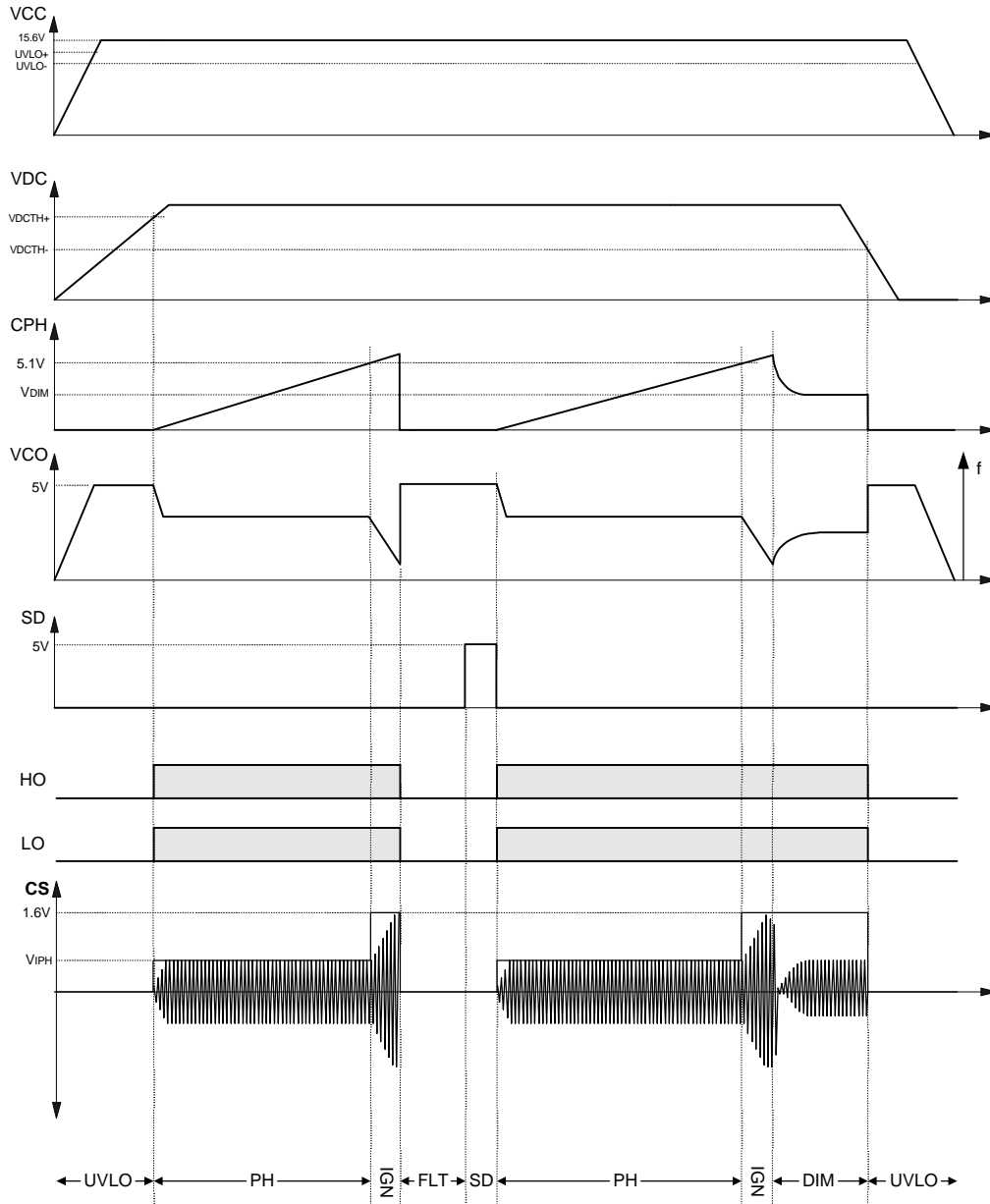
State Diagram



IR2159/IR21591 (S)

Timing Diagram

Non-strike fault condition with lamp exchange



External Components Selection Procedure

(Note:
Please refer to
"Typical Connection"
diagram, page 1)

Set R_{VAC} and R_{VDC} such that the voltage on pin VDC will exceed 5.1 volts at the desired line turn-on voltage.

The minimum operating frequency must be lower than $f_{100\%}$ of f_{IGN} (whichever is lower). R_{FMIN} also programs I_{MIN} and I_{IPH} , so R_{FMIN} must be set first.

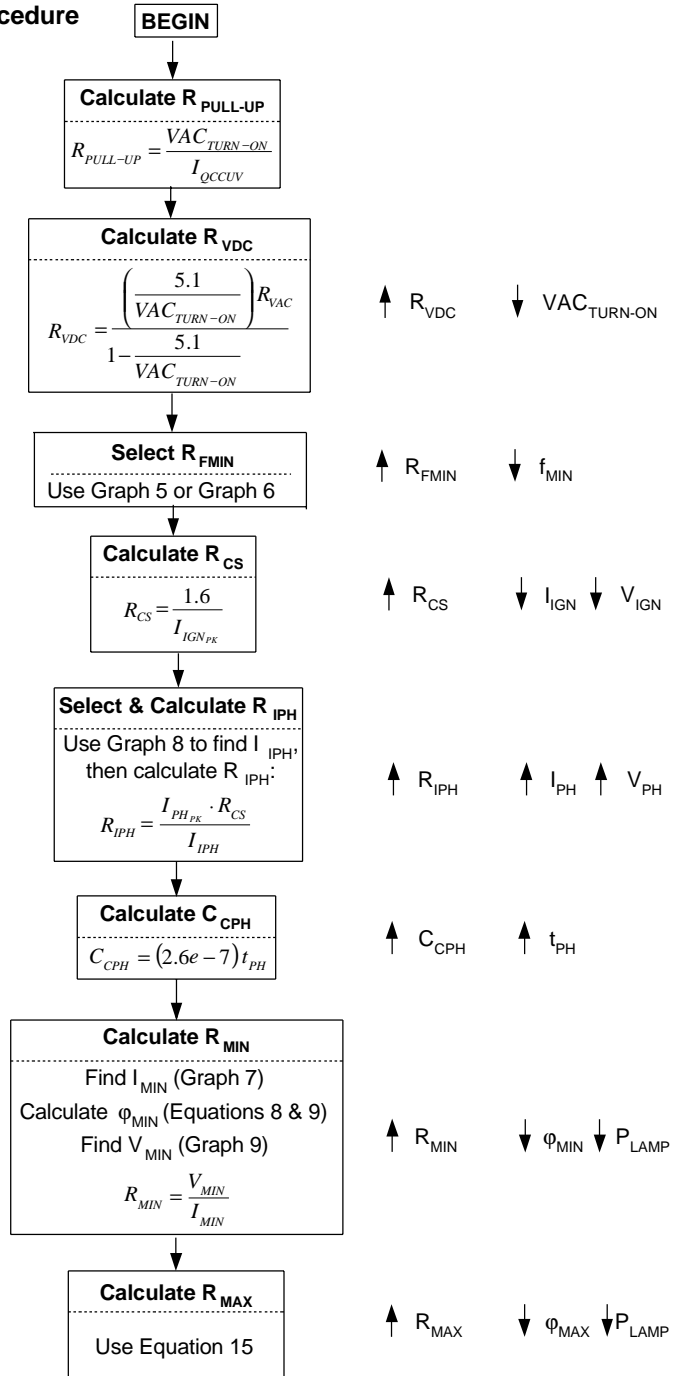
R_{CS} sets the maximum ignition current which corresponds to the maximum ignition voltage across the lamp.

The voltage at pin IPH is the reference for amplitude current control during preheat mode. R_{IPH} must be set after R_{FMIN} .

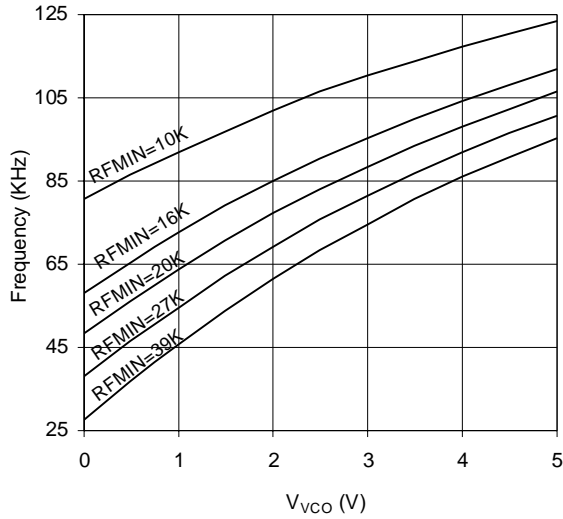
During preheat, an internal $1.3\mu A$ current source at pin CPH charges external capacitor CPH. Preheat mode ends when VCPH exceeds 5.1 volts.

R_{MIN} sets the lower phase boundary corresponding to minimum lamp power when $V_{DIM} = 0$ volts. R_{MIN} must be set after R_{FMIN} .

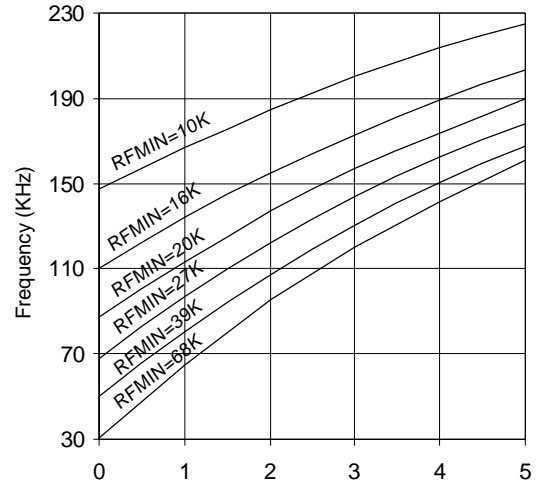
R_{MAX} sets the upper phase boundary corresponding to maximum lamp power when $V_{DIM} = 5$ volts. R_{MAX} must be set after R_{FMIN} and R_{MIN} .



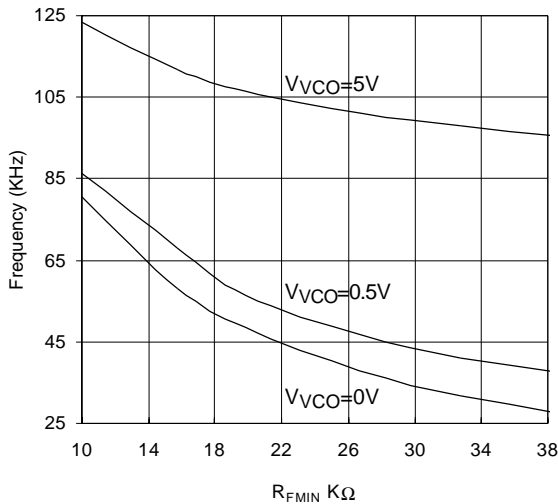
Characteristic Curves



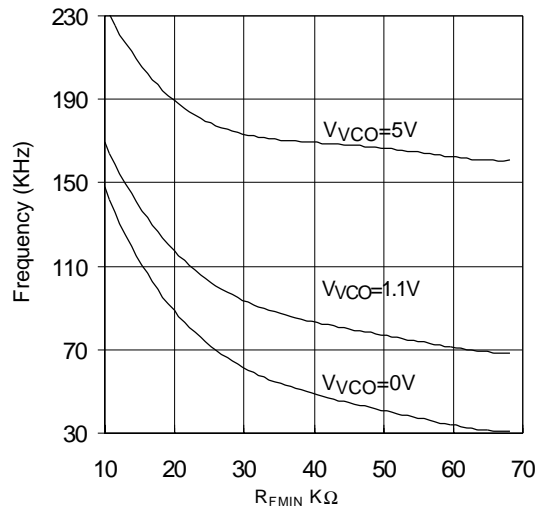
Graph 1. Frequency vs V_{VCO} (IR2159)



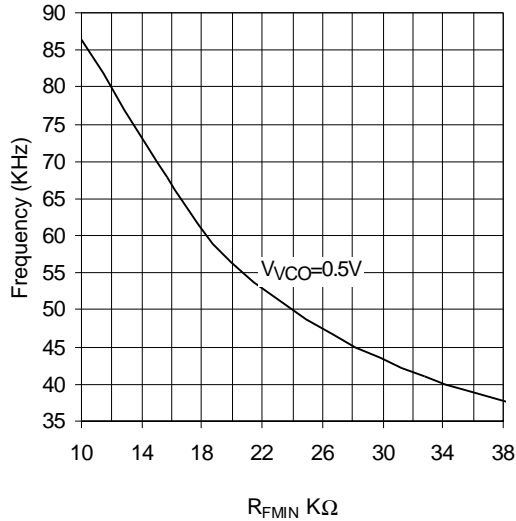
Graph 2. Frequency vs V_{VCO} (IR21591)



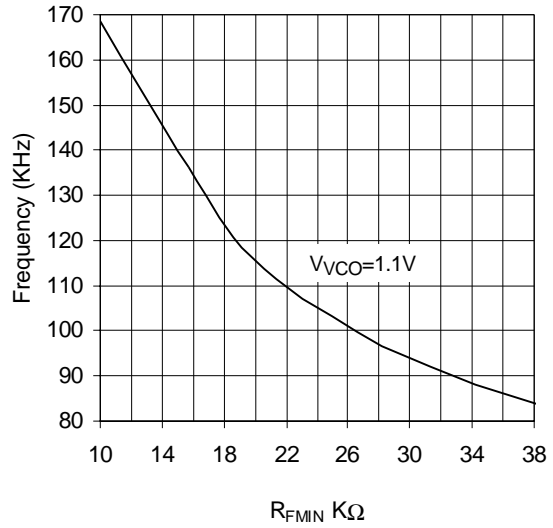
Graph 3. Frequency vs R_{FMIN} (IR2159)



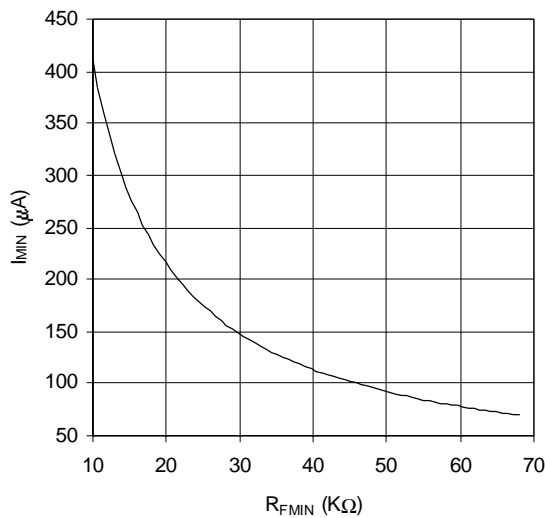
Graph 4. Frequency vs R_{FMIN} (IR21591)



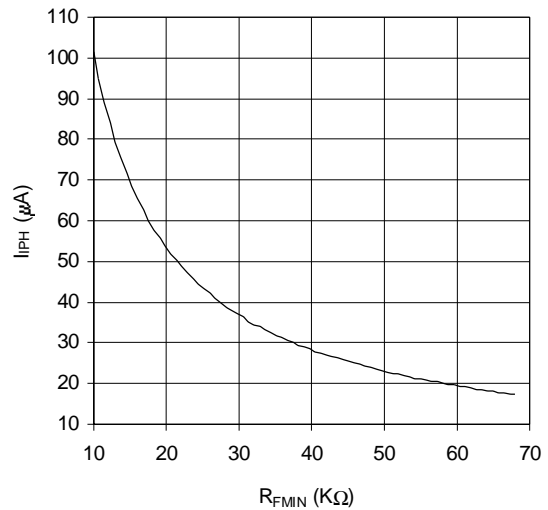
Graph 5. Frequency vs R_{FMIN} (IR2159)



Graph 6. Frequency vs R_{FMIN} (IR21591)

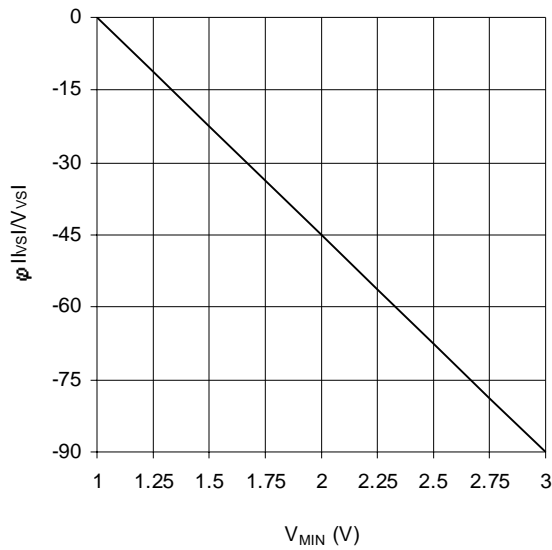


Graph 7. I_{MIN} vs R_{FMIN} (IR2159/IR21591)

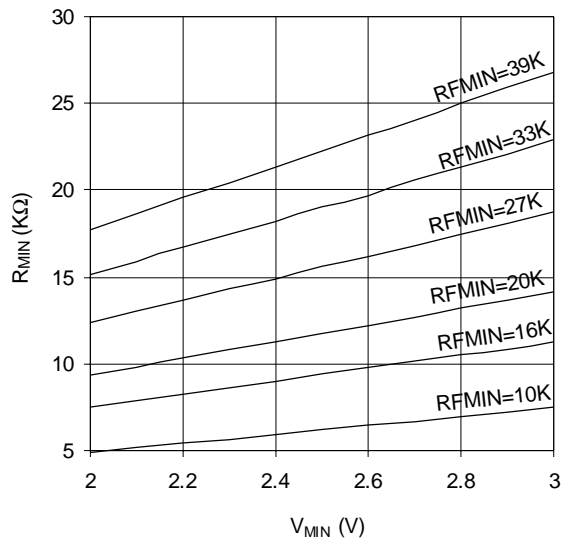


Graph 8. I_{IPH} vs R_{FMIN} (IR2159/IR21591)

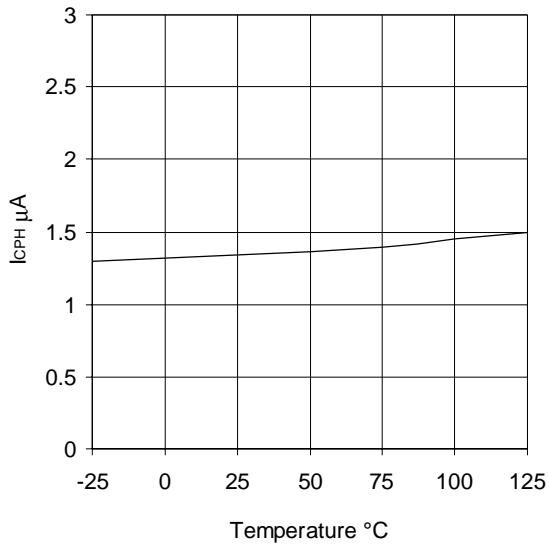
IR2159/IR21591 (S)



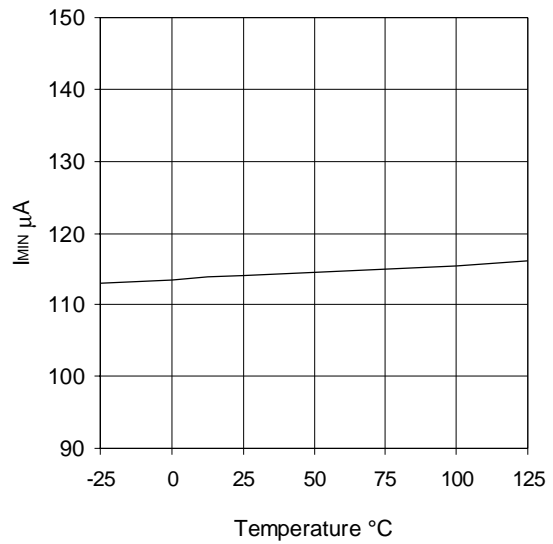
Graph 9. $\phi_{II_{VS}/V_{VS1}}$ vs V_{MIN} (IR2159/IR21591)



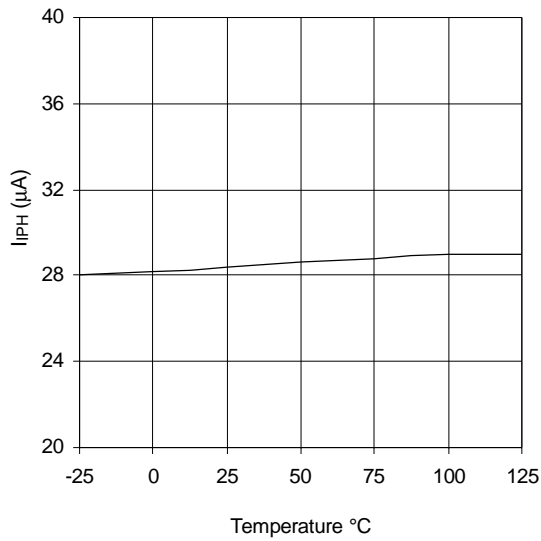
Graph 10. R_{MIN} vs V_{MIN}



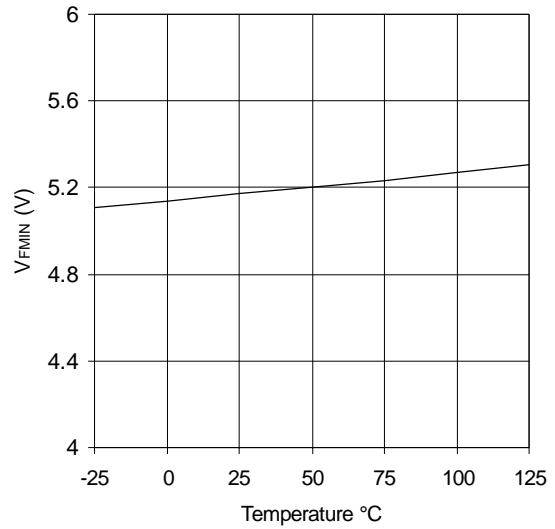
Graph 11. I_{CPH} vs Temperature (IR2159/IR21591)



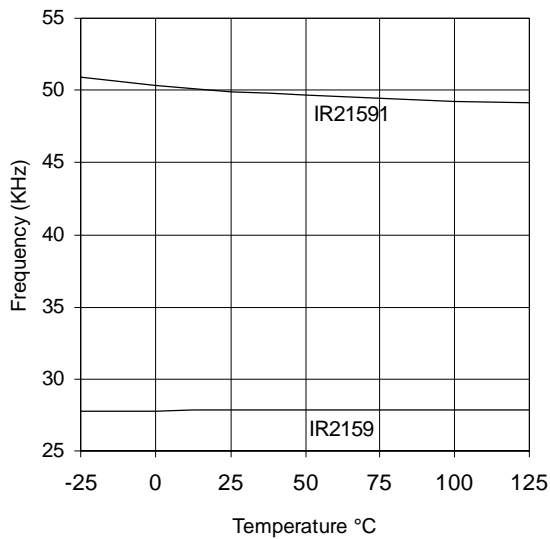
Graph 12. I_{MIN} vs Temperature (IR2159/IR21591)



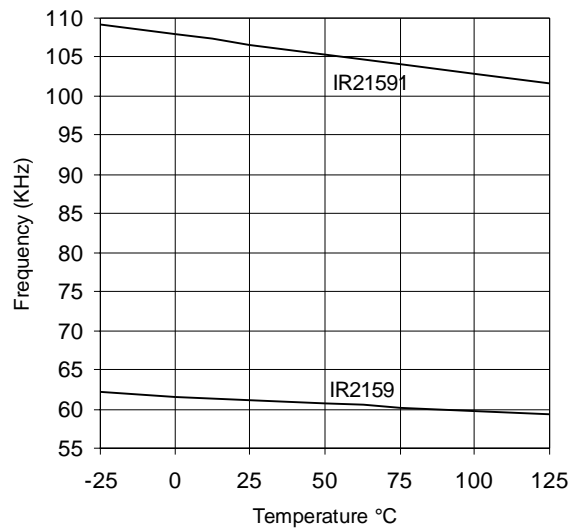
Graph 13. I_{PH} vs Temperature (IR2159/IR21591)



Graph 14. V_{FMIN} vs Temperature (IR2159/IR21591)

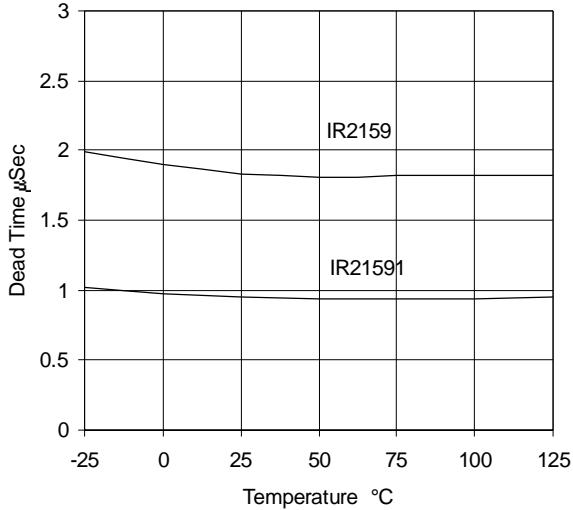


Graph 15. Frequency vs Temperature
 $V_{CO}=0V$ (IR2159/IR21591)



Graph 16. Frequency vs Temperature
 $V_{CO}=2V$ (IR2159/IR21591)

IR2159/IR21591 (S)



Graph 17. Dead Time vs Temperature (IR2159/IR21591)

Functional Description

Phase Control

To understand phase control, a simplified model for the ballast output stage is used (Figure 1). The lamp and filaments are replaced with resistors, with the lamp inserted between the filament resistors (R1, R2, R3 and R4).

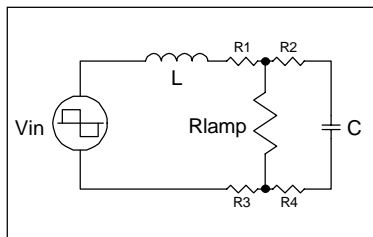


Figure 1, Dimming ballast output stage.

During preheat and ignition (Figure 2), the circuit is a high-Q series LC with a strong input current to input voltage phase inversion from +90 to -90 degrees at the resonance frequency. For operating frequencies slightly above resonance and higher, the phase is fixed at -90 degrees for the duration of preheat and ignition. During dimming, the circuit is an L in series with a parallel R and C, with a weak phase inversion at high lamp power and a strong phase inversion at low lamp power.

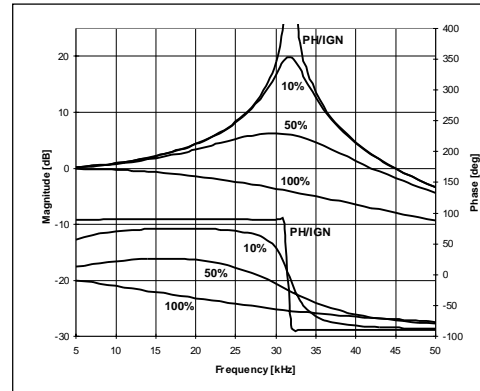


Figure 2, Typical output stage transfer function for different lamp power levels.

In the time domain (Figure 3), the input current is shifted -90 degrees from the input half-bridge voltage during preheat and ignition, and somewhere between 0 and -90 degrees after ignition during running. Zero phase-shift corresponds to maximum power

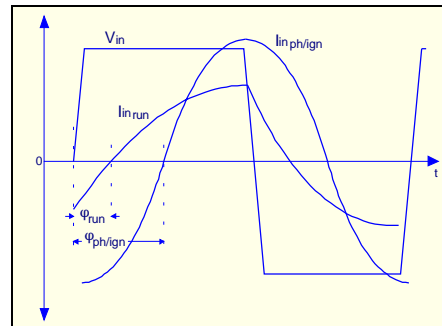


Figure 3, Typical ballast output stage waveforms.

When the phase is calculated and plotted versus lamp power (Figure 4), the result is a linear dimming curve, even down to ultra-low light levels where the resistance of the lamp can change by orders of magnitude.

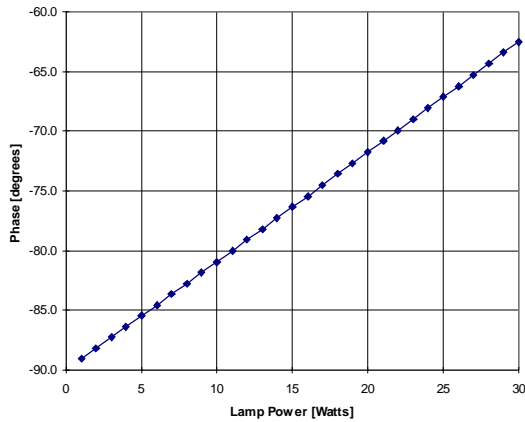


Figure 4, Lamp power vs. phase of output stage.

Under-voltage Lock-Out (UVLO)

The IR2159 undervoltage lock-out is designed to maintain an ultra low quiescent current of less than 200uA, while guaranteeing the IC is fully functional before the high and low side output drivers are activated. Figure 5 shows an efficient supply voltage using the start-up current of the IR2159 together with a charge pump from the ballast output stage (R1, C1, C2, D1 and D2).

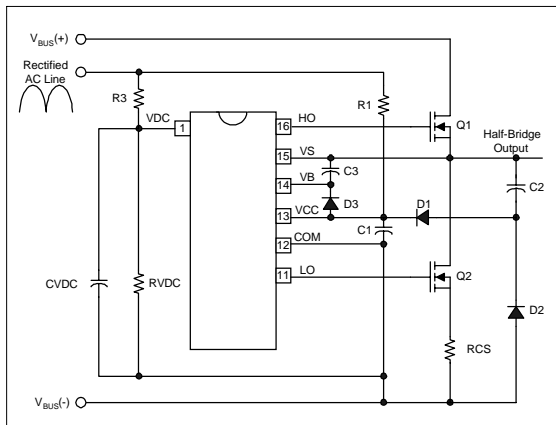


Figure 5, Typical application of start-up circuitry.

The start-up capacitor (C1) is charged by current through resistor (R1) minus the start-up current drawn by the IC. This resistor is typically chosen to provide 2X the maximum start-up current at low line to guarantee start-up under the worst case condition. Once the capacitor voltage reaches the start-up threshold, and, the voltage on pin VDC is above 5.1V (see Brown-out Protection), the IC turns on and HO and LO begin to oscillate. The capacitor begins to discharge due to the increase in IC operating current (Figure 6).

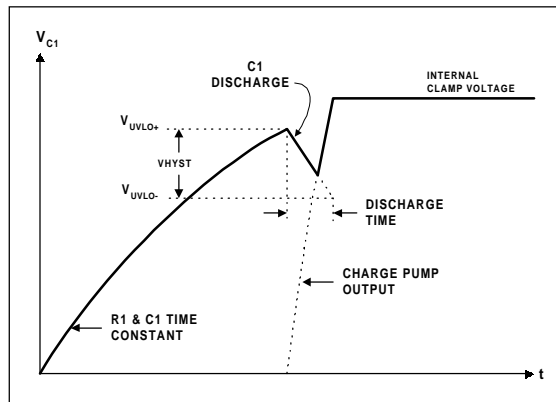


Figure 6, Start-up capacitor (C1) voltage.

During the discharge cycle, the rectified current from the charge pump charges the capacitor above the minimum operating voltage of the device and the charge pump and internal 15.6V zener clamp of the IC take over as the supply voltage. The start-up capacitor and snubber capacitor must be selected such that worst case IC conditions are satisfied. A bootstrap diode (D3) and supply capacitor (C3) comprise the supply voltage for the high side driver circuitry. To guarantee that the high-side supply is charged up before the first pulse on pin HO, the first pulse from the output drivers comes from the LO pin. During UVLO, the high and low side driver outputs are low, pin VCO is pulled-up internally to 5V resetting the starting frequency to the maximum, and pin CPH is short-circuited internally to COM resetting the preheat time.

Brown-out Protection

In addition to the voltage on VCC being above the start-up threshold, pin VDC must also be above 5.1V for HO and LO to begin oscillating. A voltage divider (R3,RVDC) from the rectified AC line connected to pin VDC measures the rectified AC line input voltage to the ballast and programs the turn-on and turn-off line voltages. A filter capacitor (CVDC) is also connected to pin VDC that must be chosen such that the ripple is low enough and the lower turn-off threshold of 3V is not crossed during normal line conditions. This detection is necessary due to the possibility of the lamp extinguishing during low-line conditions before the IC is properly reset. Should a brown-out occur, the DC bus can drop to a level below the minimum required for the tank circuit to maintain the necessary lamp voltage. This detection will insure a clean turn-off before the DC bus drops too low and properly resets the IC to the preheat mode when the line returns.

Preheat (PH)

The IR2159 enters preheat mode when VCC exceeds the UVLO+ threshold and VDC exceeds 5.1V. HO and LO begin to oscillate at the maximum operating frequency with 50% duty cycle and at the internally set dead-time of 2 μ s. Pin CPH is disconnected from COM and an internal 1 μ A current source (Figure 7) charges the external timing capacitor on CPH linearly.

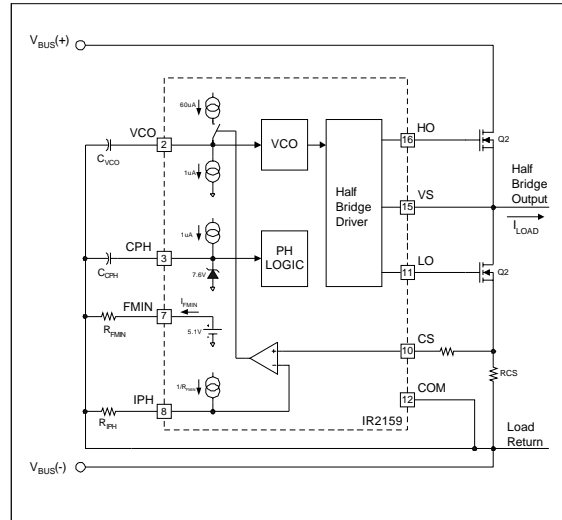


Figure 7, IR2159 preheat circuitry.

An internal 1 μ A current source slowly discharges the external capacitor on pin VCO and the voltage on pin VCO begins to decrease. This decreases the frequency, which, for operating frequencies above resonance, increases the load current. When the peak voltage measured on pin CS, produced by a portion of the load current flowing through an external sense resistor (RCS), exceeds the voltage level on pin IPH, a 60 μ A internal current source is connected to pin VCO and the capacitor charges (Figure 8). This forces the frequency to increase and the load current to decrease. When the voltage on pin CS decreases below IPH, the 60 μ A current source is disconnected and the frequency decreases again.

and the IR2159 enters DIM mode and the phase control loop is closed.

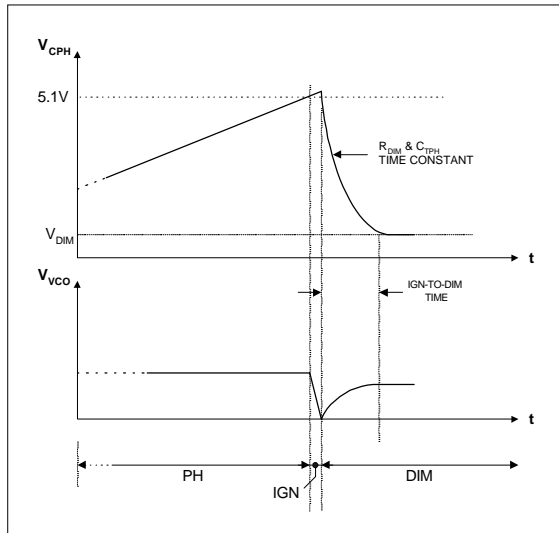


Figure 10, IR2159 ignition timing diagram.

For a reliable ignition with minimal start-up flash, the resistor on FMIN should be set to 5kHz lower than the ignition frequency or the 100% brightness dimming frequency, whichever is lower.

Ignition-to-Dim (IGN-to-DIM)

When the VCO decreases below V_{DIMTH} , the IR2159 enters dim mode. The phase control loop is closed and the phase of the load current is regulated against the user control input on pin DIM. To control the rate at which the dim setting changes from maximum brightness to the user setting (IGN-TO-DIM time, Figure 10), pin DIM is connected internally to pin CPH when the IR2159 enters DIM mode. The resistor on pin DIM (R_{DIM}) discharges the capacitor on pin CPH down to the user dim setting. The resistor can be selected for a fast time constant to minimize the amount of flash visible over the lamp just after ignition, or, a long time constant such that the brightness ramps

down smoothly to the user setting. Should the ignition-to-dim time be too fast, however, the loop can respond faster than the ionization constant of the lamp (milliseconds) causing the VCO to over-shoot. This can result in a frequency that is higher than the minimum brightness frequency and can extinguish the lamp. The capacitor on pin CPH serves multiple functions by setting the preheat time, the travel rate just after ignition (together with resistor R_{DIM}), and, serving as a filter capacitor on pin DIM during dimming to increase high-frequency noise immunity and minimize component count.

Dimming (DIM)

To regulate lamp power, the error between the reference phase and the phase of the output stage current forces the VCO to steer the frequency in the proper direction, as determined by the transfer function of the output stage, such that the error is forced to zero. An internal 15uA current source is connected to pin VCO during dimming mode (Figure 11) to discharge the VCO capacitor and decrease the frequency towards lock.

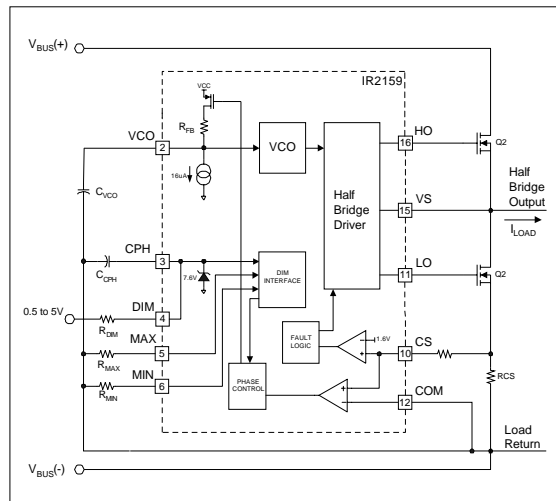


Figure 11, IR2159 dimming circuitry.

Once lock is achieved, the phase detector (PDET) outputs short pulses to an open-drain PMOS that charges the VCO capacitor through an internal resistor (RFB) each time an error pulse occurs (Figure 12). This action "nudges" the integrator at the input of the VCO to keep the phase of the output stage current exactly locked in phase with the reference.

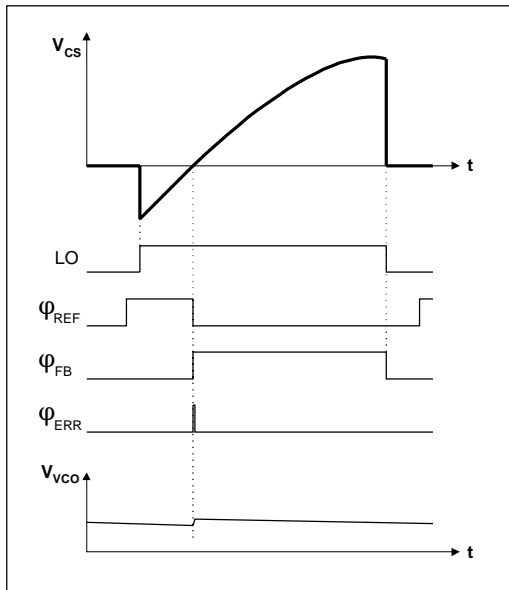


Figure 12, Phase control timing diagram.

The IR2159 includes a dimming interface for analog lamp power control. The DIM pin input requires a voltage in the range of 0.5 to 5VDC, with 5V corresponding to minimum phase shift (maximum lamp power). The output of the dim interface is the voltage on pin MIN, which is compared with the internal timing capacitor (CT) voltage to produce a frequency-independent digital reference phase (Figure 13).

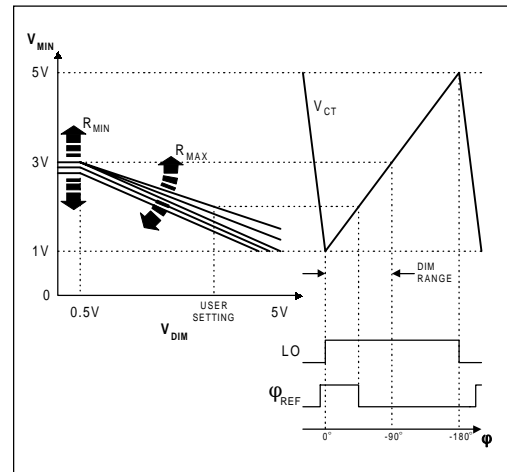


Figure 13, Dimming interface

The charging time of CT from 1V to 5.1V determines the on-time of output gate drivers HO and LO and corresponds to -180 degrees of possible phase shift in load current (minus deadtime). For the 0 to -90 degree dim range, the voltage on pin MIN is bounded between 1V and 3V using pins MIN and MAX. An external resistor on pin MAX programs the minimum phase shift reference (maximum lamp power) corresponding to 5V on pin DIM, and an external resistor on pin MIN sets the maximum phase shift (minimum lamp power) corresponding to 0.5V on pin DIM.

Current Sensing

During dimming, the current sensing circuitry (Figure 14) detects over-current which can occur during hard-switching (see Fault section), and zero-crossing to measure the phase of the total load current. To reject any switching noise which can occur at the turn-on of the low-side MOSFET or IGBT, a digital current sense blanking circuit blanks out the signal from the zero-crossing

detection comparator for 400ns after LO goes 'high' (Figure 15).

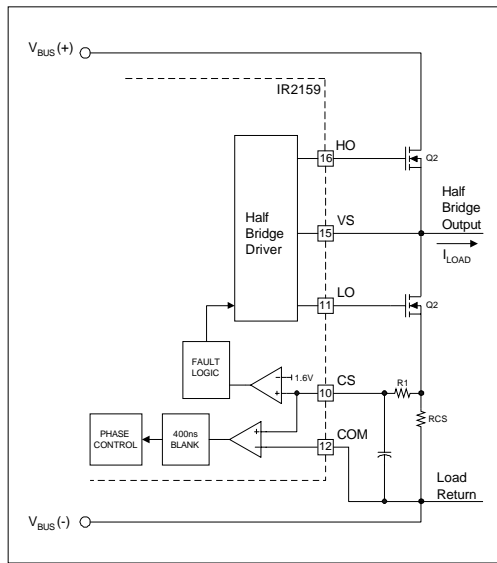


Figure 14, Current sensing circuitry.

The internal blank time reduces the dimming range slightly (Figure 15) when operating at minimum phase shift (maximum lamp power). The external programming resistor on pin MAX must be selected such that the minimum phase shift is set a safe margin away from the blank time. A series resistor (R1) is required to limit the amount of current flowing out of pin CS when the voltage across RCS goes below -0.7V. A filter capacitor at pin CS may be required due to other possible asynchronous noise sources present in the ballast system.

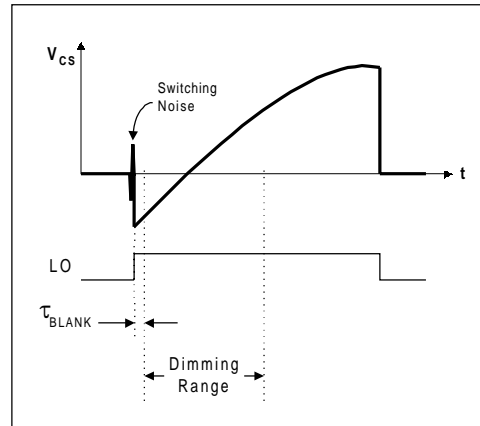


Figure 15, Current sense timing diagram.

Fault Mode (FAULT)

During dimming, the peak current regulation circuit active during preheat and ignition is disabled. Should non-zero voltage switching at the output of the half-bridge occur (Figure 18), high current spikes will result. A lamp filament failure, lamp end-of-life, lamp removal, or a deadtime shorter than what is required for commutation, can all cause hard-switching.

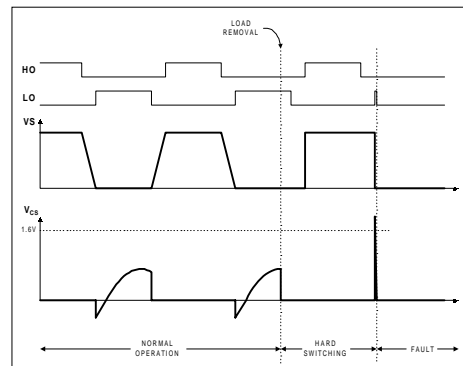


Figure 18, hard-switching with latch off

Should the peak voltage on pin CS exceed 1.6V at any time during dimming, the IR2159 enters FAULT mode and the high and low-side driver outputs, HO and LO, are both turned off. Cycling the supply voltage on VCC below or the voltage on pin SD will reset the IR2159 to preheat (PH) mode (see STATE DIAGRAM).

Ballast Design

Lamp Requirements

Before selecting component values for the ballast output stage and the programmable inputs of the IR2159, the following lamp requirements must first be defined:

Variable	Description	Units
I_{ph}	Filament pre-heat current	Arms
t_{ph}	Filament pre-heat time	s
V_{phmax}	Maximum lamp pre-heat voltage	Vpp
V_{ign}	Lamp ignition voltage	Vpp
$P_{100\%}$	Lamp power at 100% brightness	W
$V_{100\%}$	Lamp voltage at 100% brightness	Vpp
$P_{1\%}$	Lamp power at 1% brightness	W
$V_{1\%}$	Lamp voltage at 1% brightness	Vpp
$I_{Cathmin}$	Minimum cathode heating current	Arms

Table 1, Typical lamp requirements

Ballast Output Stage

The components comprising the output stage are selected using a set of equations. Different ballast operating frequencies and their respective voltages and currents are calculated.

The inductor and capacitor values are obtained using equations (2) through (7). The results of these equations reveal the location of each operating frequency and the corresponding voltages and currents. For a given L, C, DC bus voltage, and pre-heat current, the resulting voltage over the lamp during pre-heat is given as:

$$V_{ph} = \left[\left(\frac{2V_{DC}}{\pi} \right)^2 + \frac{8L}{C} I_{ph}^2 \right]^{\frac{1}{2}} - \frac{2V_{DC}}{\pi} \quad (2)$$

The resulting operating frequency during pre-heat is given as:

$$f_{ph} = \frac{\sqrt{2}I_{ph}}{\pi CV_{ph}} \quad [\text{Hz}] \quad (3)$$

The resulting operating frequency during ignition is given as:

$$f_{ign} = \frac{1}{2\pi} \sqrt{\frac{1 + \frac{4}{\pi} \frac{V_{DC}}{V_{ign}}}{LC}} \quad [\text{Hz}] \quad (4)$$

The total load current during ignition is given as:

$$I_{ign} = f_{ign} CV_{ign} 2\pi \quad [\text{App}] \quad (5)$$

The operating frequency [Hz] at maximum lamp power is given as:

$$f_{100\%} = \frac{1}{2\pi} \sqrt{\frac{1}{LC} - \frac{32P_{100\%}^2}{C^2V_{100\%}^4} + \sqrt{\left[\frac{1}{LC} - \frac{32P_{100\%}^2}{C^2V_{100\%}^4}\right]^2 - \frac{1 - \left(\frac{4V_{DC}}{V_{100\%}\pi}\right)^2}{LC^2}}} \quad (6)$$

The cathode heating current at minimum lamp power is given as:

$$I_{Cath1\%} = \frac{V_{1\%} f_{1\%} \pi C}{\sqrt{2}} \quad (7)$$

Design Constraints

The inductor and capacitor values should be iterated until the following design constraints have been fulfilled (Table II).

Design Constraint	Reason
$V_{ph} < V_{ph_{max}}$	Ignition during pre-heat
$f_{ph} - f_{ign} > 5kHz$	Production tolerances
$I_{ign} < I_{ign_{max}}$	Inductor saturation
$I_{Cath1\%} \geq I_{Cath_{min}}$	Lamp extinguishing during dimming

Table II, Ballast design constraints

IR2159 Programmable Inputs

In order to program the MIN and MAX settings of the dimming interface, the phase of the output stage current at minimum and maximum lamp power must be calculated. This is obtained using the following equations:

$$f_{\%} = \frac{1}{2\pi} \sqrt{\frac{1}{LC} - \frac{32P_{\%}^2}{C^2V_{\%}^4} + \sqrt{\left[\frac{1}{LC} - \frac{32P_{\%}^2}{C^2V_{\%}^4}\right]^2 - \frac{1 - \left(\frac{4V_{DC}}{V_{\%}\pi}\right)^2}{LC^2}}} \quad (8)$$

$$\phi_{\%} = \frac{180}{\pi} \tan^{-1} \left[\left(\frac{V_{\%}^2}{2P_{\%}} C - \frac{2P_{\%}}{V_{\%}^2} L \right) 2\pi f_{\%} - 4 \frac{V_{\%}^2}{P_{\%}} LC^2 \pi^3 f_{\%}^3 \right] \quad (9)$$

With the lamp requirements defined, the L and C of the ballast output stage selected, and the minimum and maximum phase calculated, the component values for setting the programmable inputs of the IR2159 are obtained with the following equations:

$$R_{FMIN} = \frac{(25e - 6) - (f_{MIN} - 10000) \cdot (1e - 10)}{(f_{MIN} - 10000) \cdot (2e - 14)} \quad [\text{Ohms}] \quad (10)$$

$$R_{CS} = \frac{2 \cdot (1.6)}{I_{ign}} \quad [\text{Ohms}] \quad (11)$$

$$R_{IPH} = R_{FMIN} R_{CS} I_{ph} \sqrt{2} \quad [\text{Ohms}] \quad (12)$$

$$C_{CPH} = (2.6E - 7)(t_{PH}) \quad [\text{Farads}] \quad (13)$$

$$R_{MIN} = \frac{R_{FMIN}}{4} \left(1 - \frac{\phi_{1\%}}{45} \right) \quad [\text{Ohms}] \quad (14)$$

$$R_{MAX} = \frac{R_{FMIN} \cdot R_{MIN}}{4 \cdot R_{MIN} - R_{FMIN} \cdot \left(1 - \frac{\phi_{100\%}}{45} \right)} \quad [\text{Ohms}] \quad (15)$$

This ballast design procedure has been summarized into the following 3 steps:

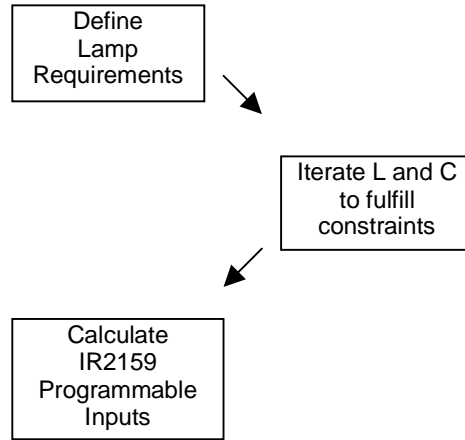
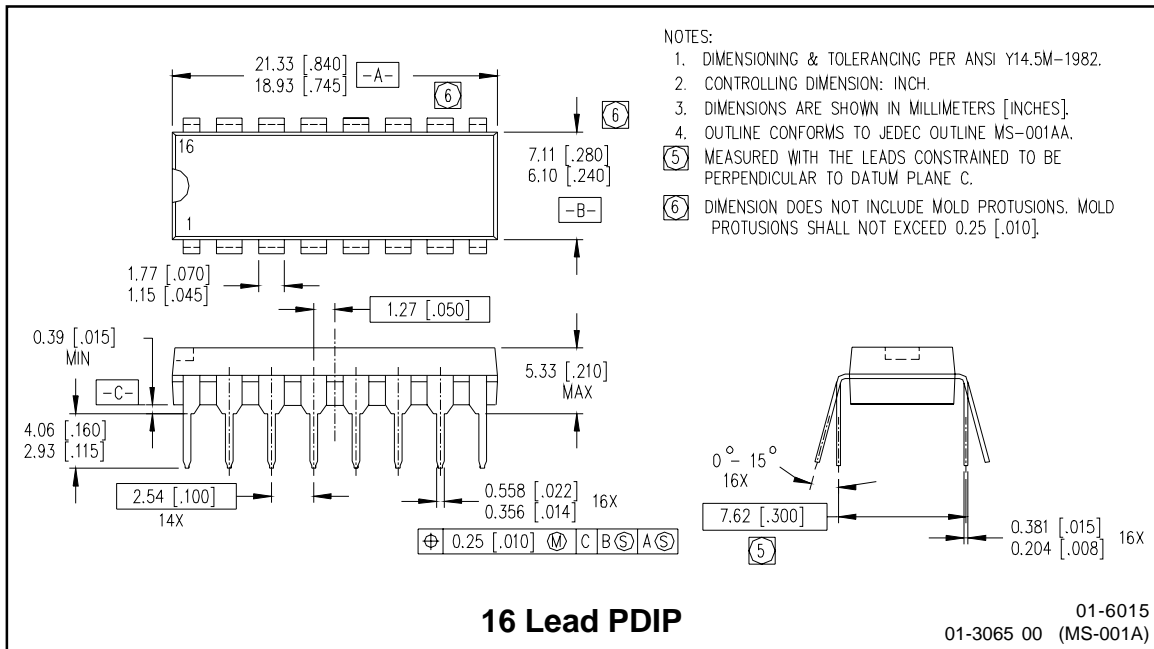


Figure 19, Simplified Ballast Design Procedure

Case outline



IR2159/IR21591 (S)

