

High and Low Side Driver

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage
- dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
- Separate logic supply range from 3.3V to 20V
- Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

600V max.
2A / 2A
10 – 20V
120 & 94 ns
20 ns

Description

The IR25607 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 V.

Package Options



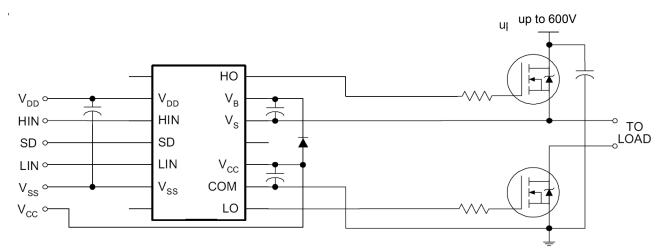
Ordering Information

Dana Bart Nambar		Standar	d Pack	Ondonakla Bart Namakan
Base Part Number	Package Type	Form	Quantity	Orderable Part Number
IR25607SPBF	SO16W	Tube	45	IR25607SPBF
IR25607SPBF	SO16W	Tape and Reel	1000	IR25607STRPBF



Typical Connection Diagram

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(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply voltage	-0.3	625	
Vs	High side floating supply offset voltage	V _B - 25	V _B + 0.3	
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3	
V _C C	Low side and logic fixed supply voltage	-0.3	25	V
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3	_ v
V_{DD}	Logic supply voltage	-0.3	V _{SS} + 25	
V _{SS}	Logic supply offset voltage	V _{CC} – 25	V _{CC} + 0.3	
V _{IN}	Logic input voltage (HIN, LIN & SD)	V _{SS} -0.3	V _{DD} + 0.3	
dVs/dt	Allowable offset supply voltage transient	_	50	V/ns
P_{D}	Package power dissipation @ T _A ≤ +25°C	_	1.25	w
Rth _{JA}	Thermal resistance, junction to ambient	_	100	°C/W
ТJ	Junction temperature	_	150	
Ts	Storage temperature	-55	150	°C
TL	Lead temperature (soldering, 10 seconds)	_	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply absolute voltage	V _S + 10	V _S + 20	
Vs	High side floating supply offset voltage	†	600	
V_{HO}	High side floating output voltage	V _S	V _B	
V _{CC}	Low side fixed supply voltage	10	20	V
V_{LO}	Low side output voltage	0	V _{CC}	V
V_{DD}	Logic supply voltage	V _{SS} + 3	V _{SS} + 20	
V _{SS}	Logic supply offset voltage	-5 ††	5	
V _{IN}	Logic input voltage (HIN, LIN & SD)	V _{SS}	V_{DD}	
T _A	Ambient temperature	-40	125	°C

⁺ Logic operational for VS of -5 to +600V. Logic state held for VS of -5V to -VBS. (Please refer to Design Tip DT97-3 for more details).

⁺⁺ When V_{DD} < 5V, the minimum V_{SS} offset is limited to - V_{DD} .



Dynamic Electrical Characteristics

 V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, CL = 1000 pF, V_{SS} = COM and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Тур.	Max.	Units	Test Conditions
ton	Turn-on propagation delay	_	120	150		$V_S = 0V$
toff	Turn-off propagation delay	_	94	125		$V_{S} = 600V$
tsd	Shutdown propagation delay	_	110	140	ns	V _S = 600V
tr	Turn-on rise time	_	25	35	113	
tf	Turn-off fall time	_	17	25		
MT	Delay matching, HS & LS turn-on/off	_	_	20		

Static Electrical Characteristics

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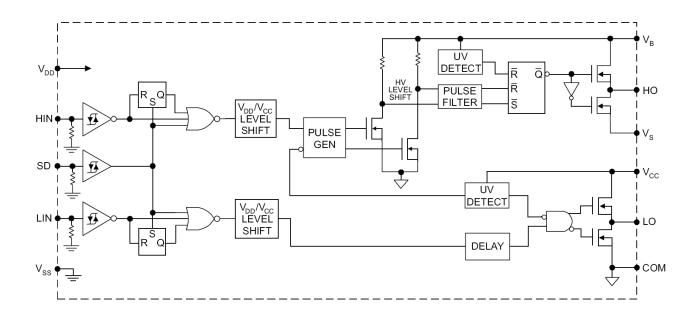
 V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Тур.	Max.	Units	Test Conditions
V _{IH}	Logic "1" input voltage	9.5	_			
V _{IL}	Logic "0" input voltage	_	_	6.0	V	
V _{OH}	High level output voltage, V_{BIAS} - V_{O}	_	_	1.2]	I _O = 0A
V _{OL}	Low level output voltage, Vo	_	_	0.1		I _O = 0A
I _{LK}	Offset supply leakage current	_	_	50		$V_{B} = V_{S} = 600V$
I_{QBS}	Quiescent V _{BS} supply current	_	125	230		$V_{IN} = 0V \text{ or } V_{DD}$
I _{QCC}	Quiescent V _{CC} supply current	_	180	340		$V_{IN} = 0V \text{ or } V_{DD}$
I_{QDD}	Quiescent V _{CC} supply current	_	15	30	μA	$V_{IN} = 0V \text{ or } V_{DD}$
I _{IN+}	Logic "1" input bias current	_	20	40		$V_{IN} = V_{DD}$
I _{IN-}	Logic "0" input bias current	_	_	1		$V_{IN} = 0V$
V _{BSUV+}	V _{BS} supply undervoltage positive going threshold	7.5	8.6	9.7		
V _{BSUV-}	V _{BS} supply undervoltage negative going threshold	7.0	8.2	9.4	V	
V _{CCUV+}	V _{CC} supply undervoltage positive going threshold	7.4	8.5	9.6		
V _{CCUV-}	V _{CC} supply undervoltage negative going threshold	7.0	8.2	9.4		
I _{O+}	Output high short circuit pulsed current	2	2.5		_	$V_O = 0V$, $V_{IN} = V_{DD}$ $PW \le 10 \ \mu s$
I _{O-}	Output low short circuit pulsed current	2	2.5	_	A	$V_O = 15V$, $V_{IN} = V_{DD}$ $PW \le 10 \mu s$



Functional Block Diagram

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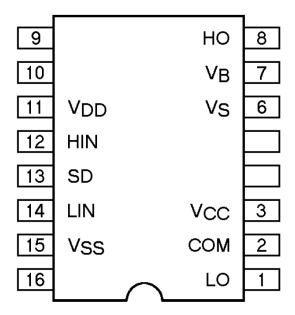


Lead Definitions

Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
НО	High side gate drive output
Vs	High side floating supply return
V _{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

6 www.irf.com





Application Information and Additional Details

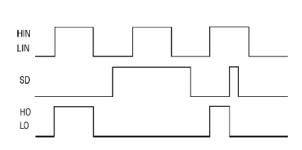


Figure 1. Input/Output Timing Diagram

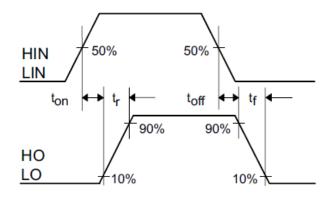


Figure 2. Switching Time Waveform Definitions

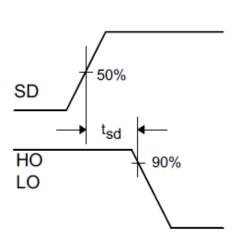


Figure 3. Shutdown Waveform Definitions

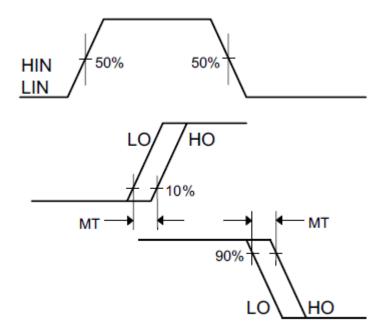


Figure 4. Delay matching Waveform Definitions



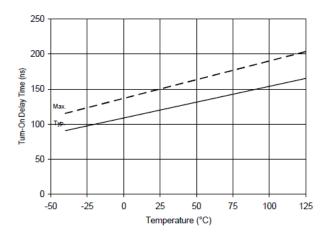


Figure 5A. Turn On Time vs. Temperature

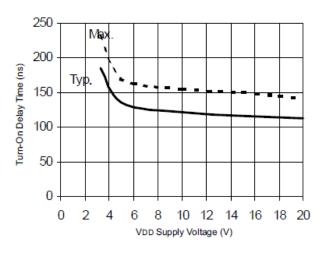


Figure 5C. Turn On Time vs. V_{DD} Supply Voltage

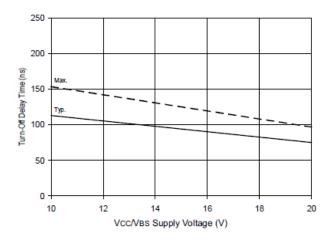


Figure 6B. Turn Off Time vs. V_{CC}/V_{BS} Supply Voltage

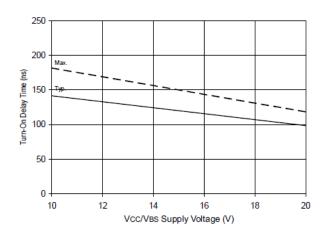


Figure 5B. Turn On Time vs. V_{CC}/V_{BS} Supply Voltage

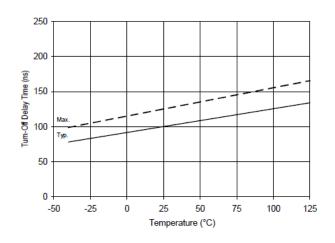


Figure 6A. Turn Off Time vs. Temperature

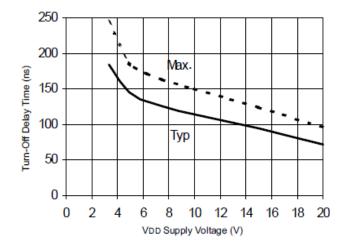


Figure 6C. Turn Off Time vs. V_{DD} Supply Voltage



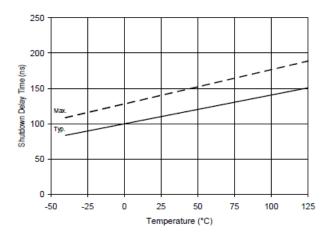


Figure 7A. Shutdown Time vs. Temperature

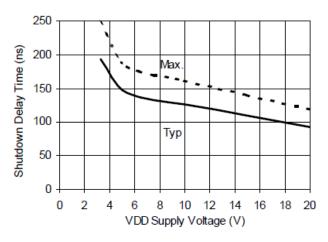


Figure 7C. Shutdown Time vs. V_{DD} Supply Voltage

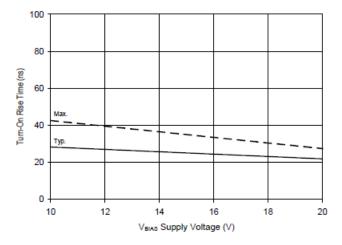


Figure 8B. Turn On Rise Time vs. Voltage

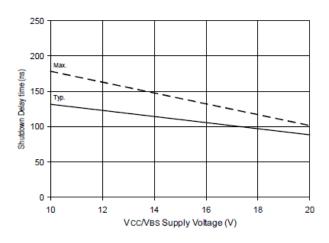


Figure 7B. Shutdown Time vs. V_{CC}/V_{BS} Supply Voltage

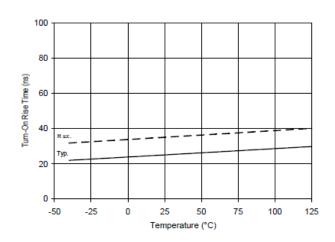


Figure 8A. Turn On Rise Time vs. Temperature

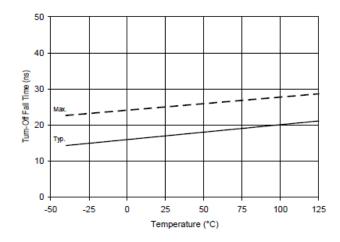


Figure 9A. Turn Off Fall Time vs. Temperature



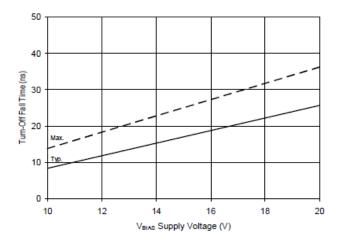


Figure 9B. Turn Off Fall Time vs. Voltage

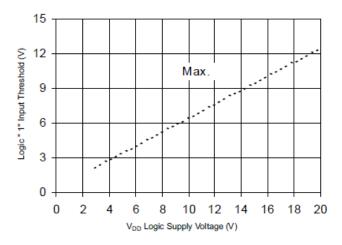


Figure 10B. Logic '1' Input Threshold vs. Voltage

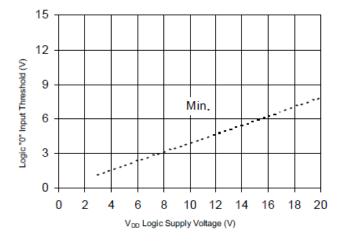


Figure 11B. Logic '0' Input Threshold vs. Voltage

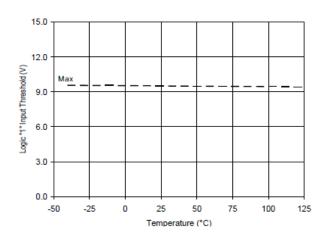


Figure 10A. logic '1' Input Threshold vs. Temperature

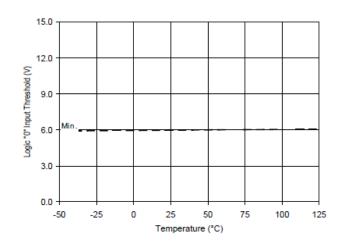


Figure 11A. Logic '0' Input Threshold vs. Temperature

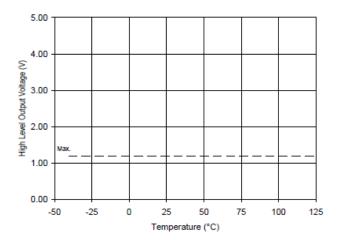


Figure 12A. High Level Output vs. Temperature



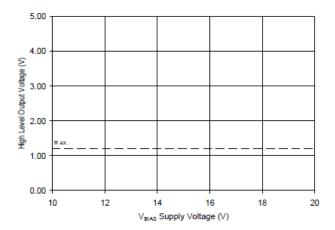


Figure 12B. High Level Output vs. Voltage

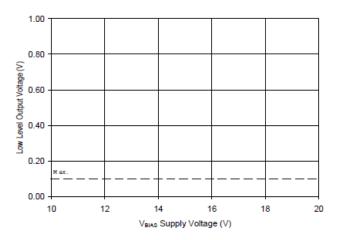


Figure 13B. Low Level Output vs. Voltage

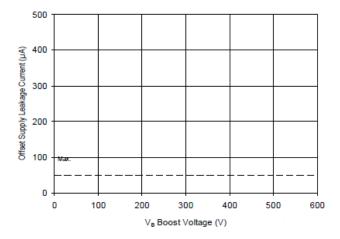


Figure 14B. Offset Supply Current vs. Voltage

11

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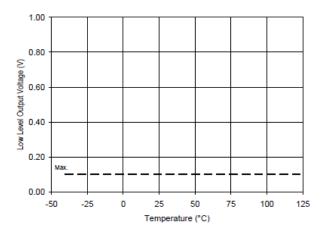


Figure 13A. Low Level Output vs. Temperature

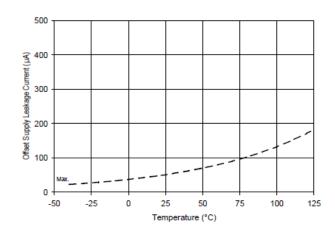


Figure 14A. Offset Supply Current vs. Temperature

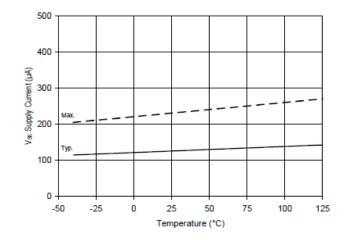


Figure 15A. V_{BS} Supply Current vs. Temperature



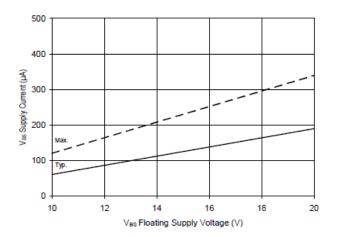


Figure 15B. V_{BS} Supply Current vs. Voltage

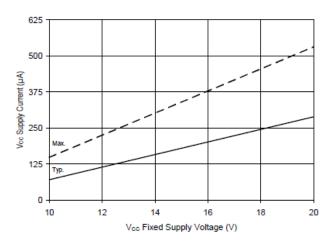


Figure 16B. V_{CC} Supply Current vs. Voltage

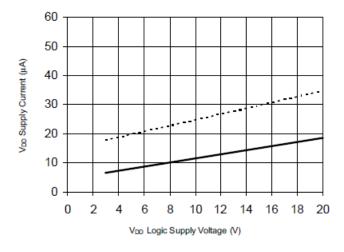


Figure 17B. V_{DD} Supply Current vs. V_{DD} Voltage

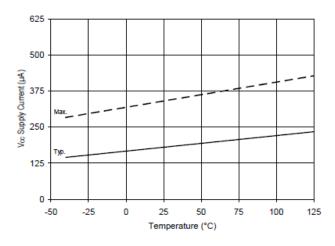


Figure 16A. V_{CC} Supply Current vs. Temperature

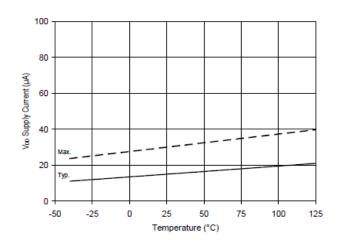


Figure 17A. V_{DD} Supply Current vs. Temperature

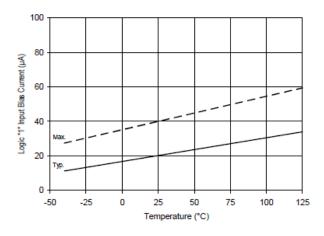
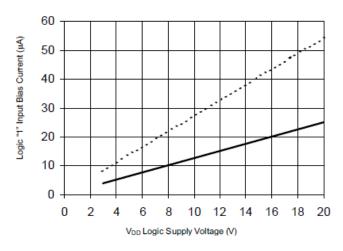


Figure 18A. Logic '1' Input Current vs. Temperature

March 26, 2013

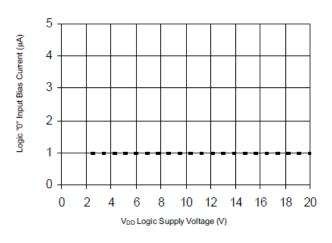




5.00 4.00 Logic "0" Input Bias Current (µA) 2.00 1.00 0.00 -50 -25 0 25 50 75 100 125 Temperature (°C)

Figure 18B. Logic '1' Input Current vs. V_{DD} Voltage

Figure 19A. Logic '0' Input Current vs. Temperature



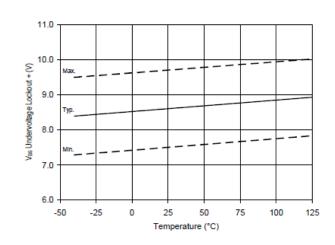
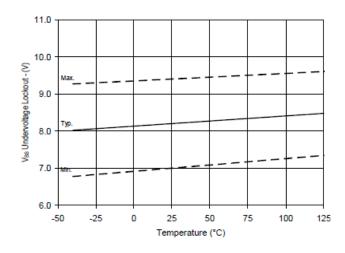


Figure 19B. Logic '0' Input Current vs. V_{DD} Voltage

Figure 20. V_{BS} Undervoltage (+) vs. Temperature



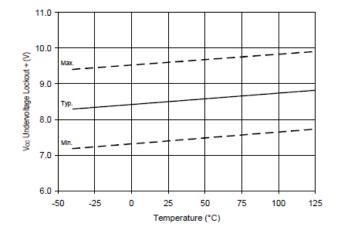
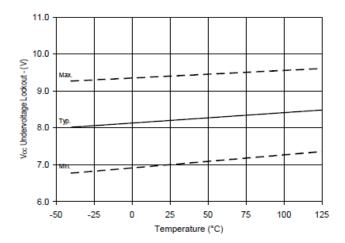


Figure 21 V_{BS} Undervoltage (-) vs. Temperature

Figure 22. V_{CC} Undervoltage (+) vs. Temperature

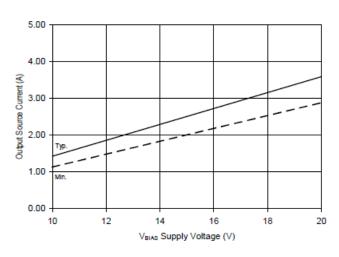




5.00 4.00 Output Source Current (A) 3.00 2.00 1.00 0.00 -50 -25 25 75 100 125 Temperature (°C)

Figure 23. V_{CC} Undervoltage (-) vs. Temperature

Figure 24A. Output Source Current vs. Temperature



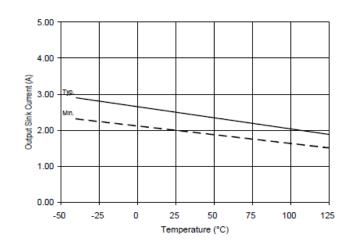
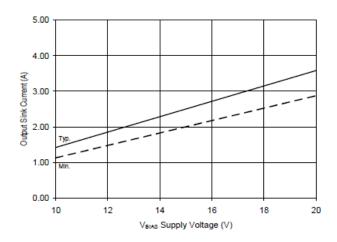


Figure 24B. Output Source Current vs. Voltage

Figure 25A. Output Sink Current vs. Temperature



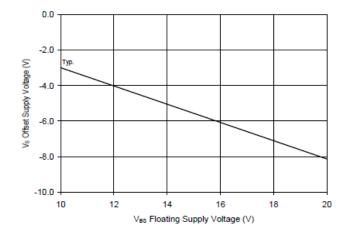


Figure 25B. Output Sink Current vs. Voltage

Figure 26. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

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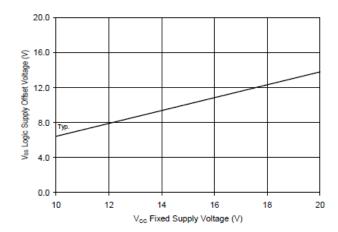
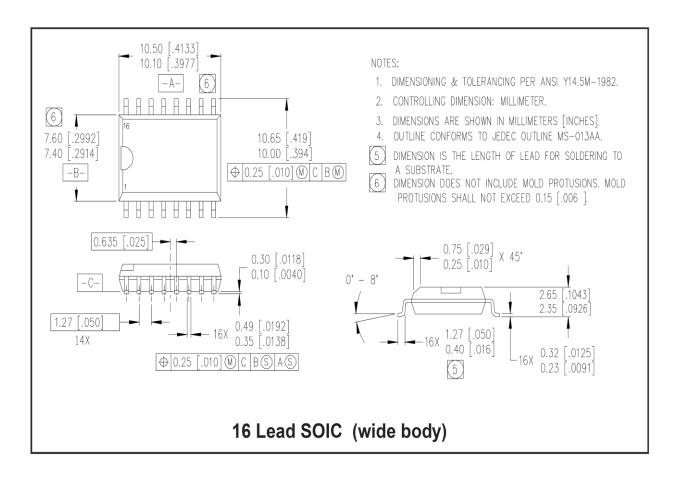


Figure 27. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

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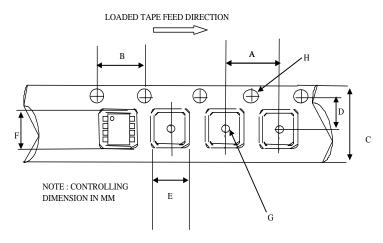
Package Details



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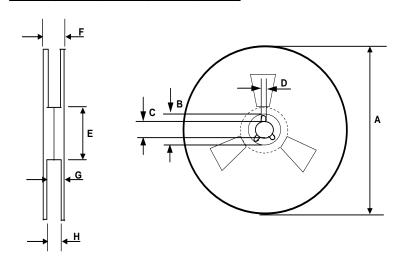


Tape and Reel Details



CARRIER TAPE DIMENSION FOR 16SOICN

	Me	etric	Imp	erial
Code	Min	Max	Min	Max
Α	7.90	8.10	0.311	0.318
В	3.90	4.10	0.153	0.161
С	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
Е	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
Н	1.50	1.60	0.059	0.062

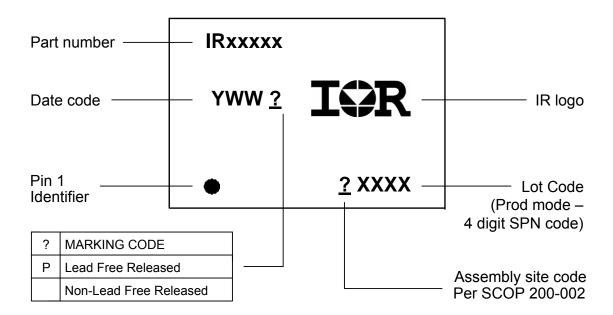


REEL DIMENSIONS FOR 16SOICN

	Metric		Imp	erial
Code	Min	Max	Min	Max
Α	329.60	330.25	12.976	13.001
В	20.95	21.45	0.824	0.844
С	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
Н	16.40	18.40	0.645	0.724



Part Marking Information



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Qualification Information[†]

	Industrial ^{††} (per JEDEC JESD 47)
Qualification Level	Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level	MSL3 ^{†††} (per IPC/JEDEC J-STD-020)
RoHS Compliant	Yes

- Qualification standards can be found at International Rectifier's web site http://www.irf.com/
- Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.
- ††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105