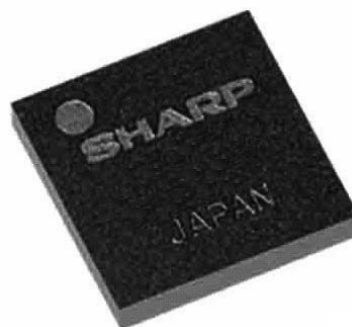


# IR2E46Y

## Illumination and Flash RGB-LED Driver



### ■ Description

**IR2E46Y** incorporates the illumination driver and the flash driver for an RGB-LED, and is equipped with the step-up DC/DC converter.

This product is optimum for use as the RGB-LED driver IC for PDA and cellular phone applications, etc.

### ■ Features

1. Power supply: 2.7 V to 4.5 V
2. Supports I<sup>2</sup>C-bus interface
  - The I<sup>2</sup>C address extension function enables simultaneous controlling of four devices.
3. SCL pin and SDA pin are installed with noise filters.
4. Sink-type variable constant current driver for RGB-LED (maximum current 155mA x 3ch)
  - Stroboscopic mode: 0mA to 155mA  
(32 steps per output, 5.0mA STEP)
  - Illumination mode: 0mA to 31.5mA  
(64 steps per output, 0.5mA STEP)
5. VF control circuit embedded (VDD to 13V)
6. LED brightness adjustment circuit embedded (16 steps, PWM control)
7. Stroboscopic timer embedded
8. Independent RGB control output enable circuit embedded
9. Current slope control circuit embedded
10. Voltage/current PWM control type step-up DC/DC converter circuit embedded (oscillatory frequency 1.2 MHz)
11. Low ON resistance switch (0.2Ω TYP.)
12. SW transistor overcurrent protection circuit embedded
13. Voltage reference embedded
14. Stand-by circuit embedded
15. Power-on-reset circuit embedded
16. UVLO circuit embedded
17. Digital soft-start circuit embedded
18. Thermal shutdown circuit embedded

### ■ Agency approvals/Compliance

1. Compliant with RoHS directive(2002/95/EC)

### ■ Applications

1. Torch light and illuminations (RGB LED)

Notice The content of data sheet is subject to change without prior notice.

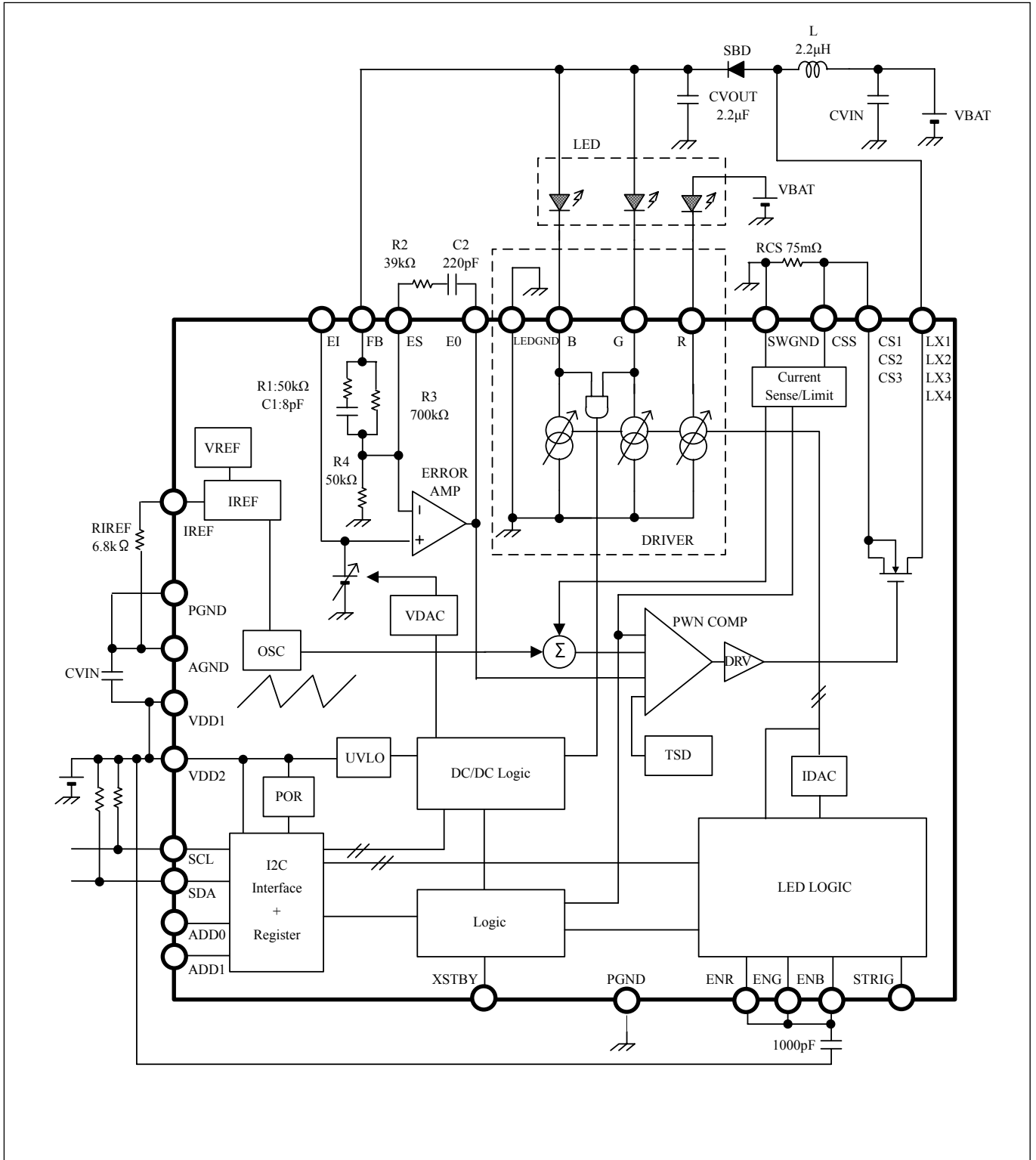
In the absence of confirmation by device specification sheets, SHARP takes no responsibility for any defects that may occur in equipment using any SHARP devices shown in catalogs, data books, etc. Contact SHARP in order to obtain the latest device specification sheets before using any SHARP devices.

Sheet No.: F1-A00301EN

Date Dec.01.2006

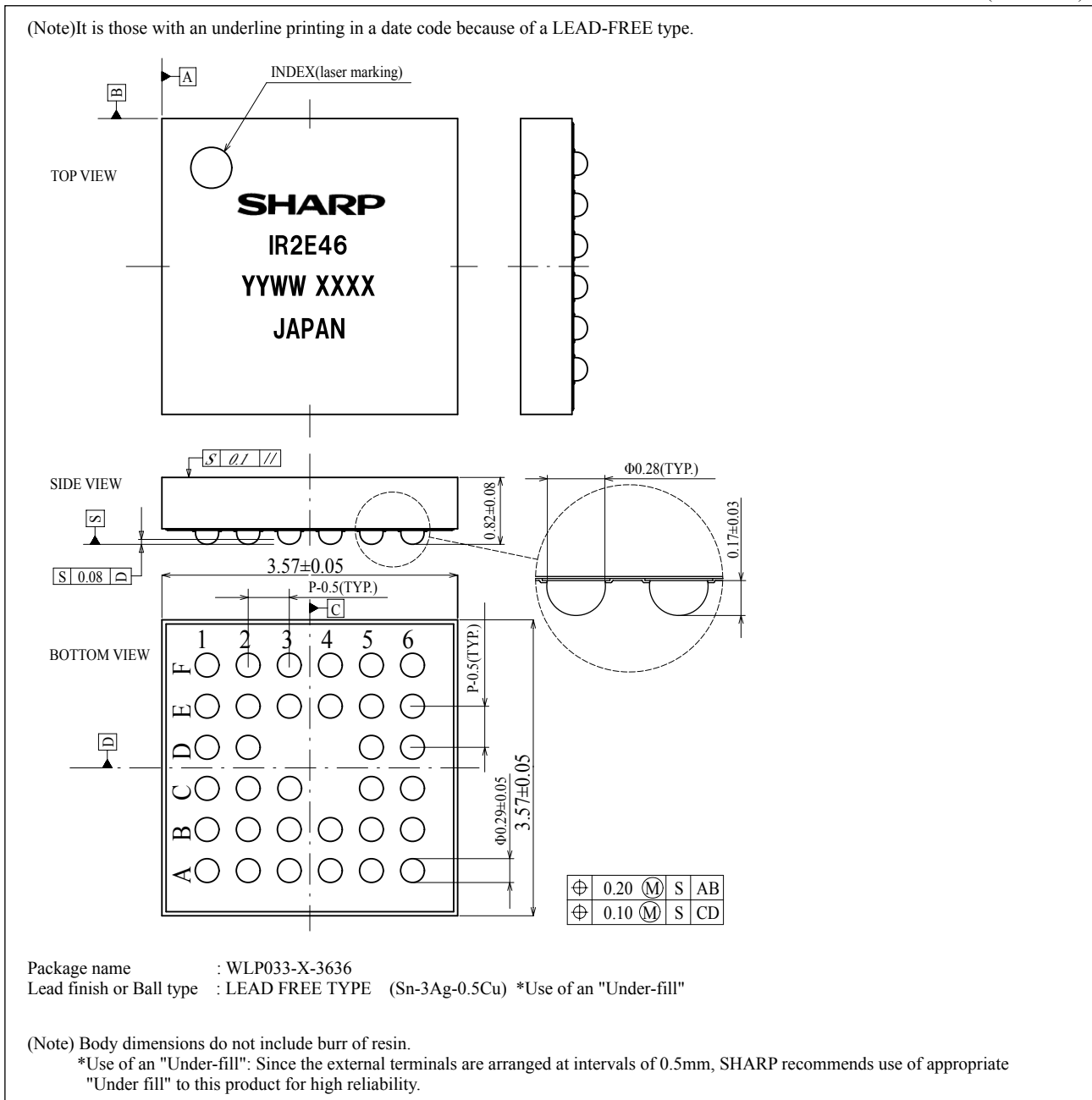
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## ■ Block diagram



## ■ Outline Dimensions

(Unit : mm)



## ■ Markings.

- (1) Product name : IR2E46
- (2) Company name : SHARP
- (3) Date code : (Example) YYWW XXXX  
 YY → Denotes the production year. (Last two digits of the year.)  
 WW → Denotes the production week. (01 · 02 · ~ · 52 · 53)  
 XXXX → Denotes the production ref. code(3~4 digits).
- (4) "JAPAN" indicates the country of origin.

## ■ Terminal Name

Pin No	Pin name	Description
A1	U1	Non-connect. This terminal is connected pin No. F1(U1).
A2	ENG	Enable input terminal for G.
A3	ENB	Enable input terminal for B.
A4	LX1	SW Tr. drain terminal.
A5	LX2	SW Tr. drain terminal.
A6	U2	Non-connect. This terminal is connected pin No. F6(U2).
B1	R	Constant current output terminal for red LED.
B2	VDD2	Power supply terminal (digital).
B3	ENR	Enable input terminal for R.
B4	PGND	Power ground.
B5	CS1	SW Tr. Source terminal.
B6	CS2	SW Tr. Source terminal.
C1	G	Constant current output terminal for green LED.
C2	B	Constant current output terminal for blue LED.
C3	NC	Non-connect.
C5	CSS	SW Tr. source terminal (current sense terminal).
C6	SWGND	SW Tr. source terminal (current sense terminal).
D1	LEDGND	LED ground.
D2	ADD1	I <sup>2</sup> C address extension input terminal.
D5	EO	Error amplifier output terminal.
D6	AGND	Analog ground.
E1	STRIG	Stroboscopic timer trigger input terminal.
E2	SDA	I <sup>2</sup> C Data Input/Output.
E3	XSTBY	Stand-by input terminal.
E4	EI	Error amplifier reference input terminal.
E5	FB	Output voltage feedback input terminal.
E6	ES	Error amplifier negative input terminal.
F1	U1	Non-connect. This terminal is connected pin No. A1(U1).
F2	ADD0	I <sup>2</sup> C address extension input terminal.
F3	SCL	I <sup>2</sup> C Clock.
F4	IREF	Resistor connection terminal for reference current setting.
F5	VDD1	Power supply terminal (analog).
F6	U2	Non-connect. This terminal is connected pin No. A6(U2).

## ■ Pin Assignment

	1	2	3	4	5	6
A	U1	ENG	ENB	LX1	LX2	U2
B	R	VDD2	ENR	PGND	CS1	CS2
C	G	B	NC		CSS	SWGND
D	LEDGND	ADD1			EO	AGND
E	STRIG	SDA	XSTBY	EI	FB	ES
F	U1	ADD0	SCL	IREF	VDD1	U2

Note: Pins are located on the underside.

### ■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Conditions
Power supply	VDD1,VDD2	6.0	V	
Terminal voltage	LX1,LX2,LX3,LX4 FB,G, B	-0.3 to 22.0	V	
	R	-0.3 to 6.0		
	Others	-0.3V to VDD+0.3		
Output current	R,G,B	155 x 3ch	mA	
Power dissipation	Pd	1667	mW	Ta≤25°C Note1
Derating ratio	ΔPd	16.67	mW/°C	Ta>25°C Note1
Operating temperature range	Topr	-30 to 85	°C	
Storage temperature range	Tstg	-55 to 125	°C	

Note1: Free convection,on-board,compiled with SEMI42-996

### ■ Recommended Operating Condition

Parameter	Symbol	Value	Unit	Conditions
Power supply	VDD1, VDD2	2.7 to 4.5	V	
Terminal voltage	LX1,LX2,LX3,LX4 FB,G, B	0 to 13	V	
	R	0 to 4.5		
	Others	0 to VDD		
I <sup>2</sup> C communication frequency	fCLK	3.4	MHz	
Switching frequency	fOSC	1.2	MHz	

## ■ Electric Characteristics

See the Block Diagram unless otherwise specified.

VDD1=VDD2=3.6V, ENR=ENG=ENB=XSTBY=3.6V, ADD0=ADD1=STRIG=0V, R=G=B=1.0V, Ta=25°C

I<sup>2</sup>C register setting: XSTB=1, BOOST=1

The current direction is regarded positive when entering the IC and negative when exiting.

### Current consumption

Parameter	Symbol	Measurement condition	MIN.	TYP.	MAX.	Unit
Stand-by supply current	ISS	XSTBY=0V or XSTB=0	-	1	3	μA
Supply current	IDD	BOOST=0	0.8	1.3	1.8	mA

### Step-up DC/DC converter circuit

Parameter	Symbol	Measurement condition	MIN.	TYP.	MAX.	Unit
Conversion efficiency	PEff			85		%
Switch ON resistance	RDSON		0.1	0.2	0.3	Ω
Switching frequency	fOSC		1.0	1.2	1.4	MHz
Maximum duty	DT			85		%
FET current limiting voltage	VCL	Voltage between CCS pin and SWGND pin	84	120	156	mV
SW Tr. OFF leak current	ILEAKSW	XSTBY=0V or XSTB=0 LX1, LX2=20V		1	5	μA

### ENR pin, ENG pin, ENB pin, STRIG pin, SDA pin, SCL pin, ADD0 pin, ADD1 pin

Parameter	Symbol	Measurement condition	MIN.	TYP.	MAX.	Unit
High level input voltage	VIH		0.8VDD	-	VDD	V
Low level input voltage	VIL		0	-	0.2VDD	V
High level input current	I <sub>IH</sub>		-1	-	1	μA
Low level input current	I <sub>IL</sub>		-1	-	1	μA
Hysteresis voltage	V <sub>hys</sub>	SDA pin, SCL pin, ADD0 pin , ADD1 pin, and STRIG pin		0.05VDD		V
ENx pulse width	PWEN	Duration when ENx is "H" or "L"	1.0	-	-	μs
SDA output terminal voltage	VOL	IOL=3mA	-	0.2	0.4	V

### XSTBY pin

Parameter	Symbol	Measurement condition	MIN.	TYP.	MAX.	Unit
High level input voltage	VIH		1.44	-	VDD	V
Low level input voltage	VIL		0	-	0.90	V
High level input current	I <sub>IH</sub>		-1	25	75	μA
Low level input current	I <sub>IL</sub>		-1	-	1	μA

### UVLO circuit

Parameter	Symbol	Measurement condition	MIN.	TYP.	MAX.	Unit
UVLO threshold voltage	TUTh		2.15	2.35	2.55	V
UVLO hysteresis	UVHys			100		mV

### Thermal shutdown circuit

Parameter	Symbol	Measurement condition	MIN.	TYP.	MAX.	Unit
Operation stop temperature			150			°C

## Constant current driver circuit

Parameter	Symbol	Measurement condition	MIN.	TYP.	MAX.	Unit
R output current (stroboscopic mode)	IoRS	RSDUTY[00000], R=1, S/I=1	-	1.0	5.0	μA
		RSDUTY[00001], R=1, S/I=1	0.0	5.0	15.0	mA
		RSDUTY[00010], R=1, S/I=1	5.0	10.0	20.0	mA
		RSDUTY[00100], R=1, S/I=1	10.0	20.0	30.0	mA
		RSDUTY[01000], R=1, S/I=1	30.0	40.0	50.0	mA
		RSDUTY[10000], R=1, S/I=1	70.0	80.0	90.0	mA
		RSDUTY[11111], R=1, S/I=1	139.5	155.0	170.5	mA
R output current (illumination mode)	IoRI	RIDUTY[000000], R=1	-	1.00	5.00	μA
		RIDUTY[000001], R=1	0.00	0.50	1.50	mA
		RIDUTY[000010], R=1	0.50	1.00	2.00	mA
		RIDUTY[000100], R=1	1.00	2.00	3.00	mA
		RIDUTY[001000], R=1	3.00	4.00	5.00	mA
		RIDUTY[010000], R=1	7.00	8.00	9.00	mA
		RIDUTY[100000], R=1	15.00	16.00	17.00	mA
RIDUTY[111111], R=1	28.35	31.50	34.65	mA		
G output current (stroboscopic mode)	IoGS	GSDUTY[00000], G=1, S/I=1	-	1.0	5.0	μA
		GSDUTY[00001], G=1, S/I=1	0.0	5.0	15.0	mA
		GSDUTY[00010], G=1, S/I=1	5.0	10.0	20.0	mA
		GSDUTY[00100], G=1, S/I=1	10.0	20.0	30.0	mA
		GSDUTY[01000], G=1, S/I=1	30.0	40.0	50.0	mA
		GSDUTY[10000], G=1, S/I=1	70.0	80.0	90.0	mA
		GSDUTY[11111], G=1, S/I=1	139.5	155.0	170.5	mA
G output current (illumination mode)	IoGI	GIDUTY[000000], G=1	-	1.00	5.00	μA
		GIDUTY[000001], G=1	0.00	0.50	1.50	mA
		GIDUTY[000010], G=1	0.50	1.00	2.00	mA
		GIDUTY[000100], G=1	1.00	2.00	3.00	mA
		GIDUTY[001000], G=1	3.00	4.00	5.00	mA
		GIDUTY[010000], G=1	7.00	8.00	9.00	mA
		GIDUTY[100000], G=1	15.00	16.00	17.00	mA
GIDUTY[111111], G=1	28.35	31.50	34.65	mA		
B output current (stroboscopic mode)	IoBS	BSDUTY[00000], B=1, S/I=1	-	1.0	5.0	μA
		BSDUTY[00001], B=1, S/I=1	0.0	5.0	15.0	mA
		BSDUTY[00010], B=1, S/I=1	5.0	10.0	20.0	mA
		BSDUTY[00100], B=1, S/I=1	10.0	20.0	30.0	mA
		BSDUTY[01000], B=1, S/I=1	30.0	40.0	50.0	mA
		BSDUTY[10000], B=1, S/I=1	70.0	80.0	90.0	mA
		BSDUTY[11111], B=1, S/I=1	139.5	155.0	170.5	mA
B output current (illumination mode)	IoBI	BIDUTY[000000], B=1	-	1.00	5.00	μA
		BIDUTY[000001], B=1	0.00	0.50	1.50	mA
		BIDUTY[000010], B=1	0.50	1.00	2.00	mA
		BIDUTY[000100], B=1	1.00	2.00	3.00	mA
		BIDUTY[001000], B=1	3.00	4.00	5.00	mA
		BIDUTY[010000], B=1	7.00	8.00	9.00	mA
		BIDUTY[100000], B=1	15.00	16.00	17.00	mA
BIDUTY[111111], B=1	28.35	31.50	34.65	mA		
R terminal leak current	ILEAKR	Terminal voltage =4.5V		1	5	μA
G terminal leak current	ILEAKG	Terminal voltage =15V		1	5	μA
B terminal leak current	ILEAKB	Terminal voltage =15V		1	5	μA



## ■ I<sup>2</sup>C-BUS Interface timing characteristics

All specified output timings are based on 20% and 80% of VDD.

### Fs-mode

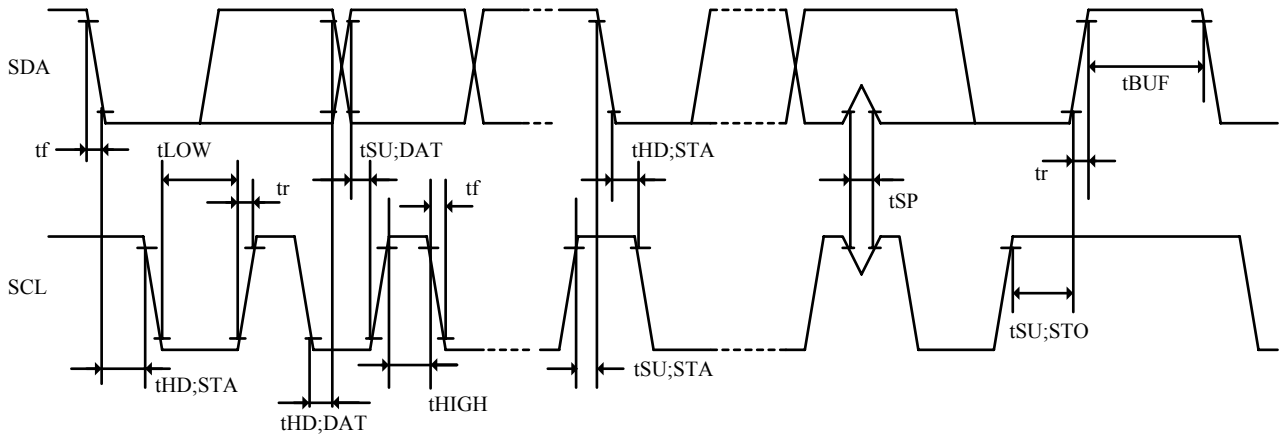
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCL clock frequency	fSCL		0	-	400	kHz
Hold time(repeated) START condition	tHD;STA		600	-	-	ns
LOW period of the SCL clock	tLOW		1300	-	-	ns
HIGH period of the SCL clock	tHIGH		600	-	-	ns
Data set-up time	tSU;DAT		100	-	-	ns
Data hold time	tHD;DAT		0	-	900	ns
SCL and SDA rise time	tr	Note 1.	20+0.1Cb	-	300	ns
SCL and SDA fall time	tf	Note 1.	20+0.1Cb	-	300	ns
Capacitive load represented by each bus line	Cb		-	-	400	pF
Set-up time for STOP condition	tSU;STO		600	-	-	ns
Tolerable spike width on bus	tSP		-	-	50	ns
Bus free time between START and STOP condition	tBUF		1300	-	-	ns
Noise margin at the LOW level for each connected device (including hysteresis)	VnL		0.1VDD	-	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	VnH		0.2VDD	-	-	V

### Hs-mode

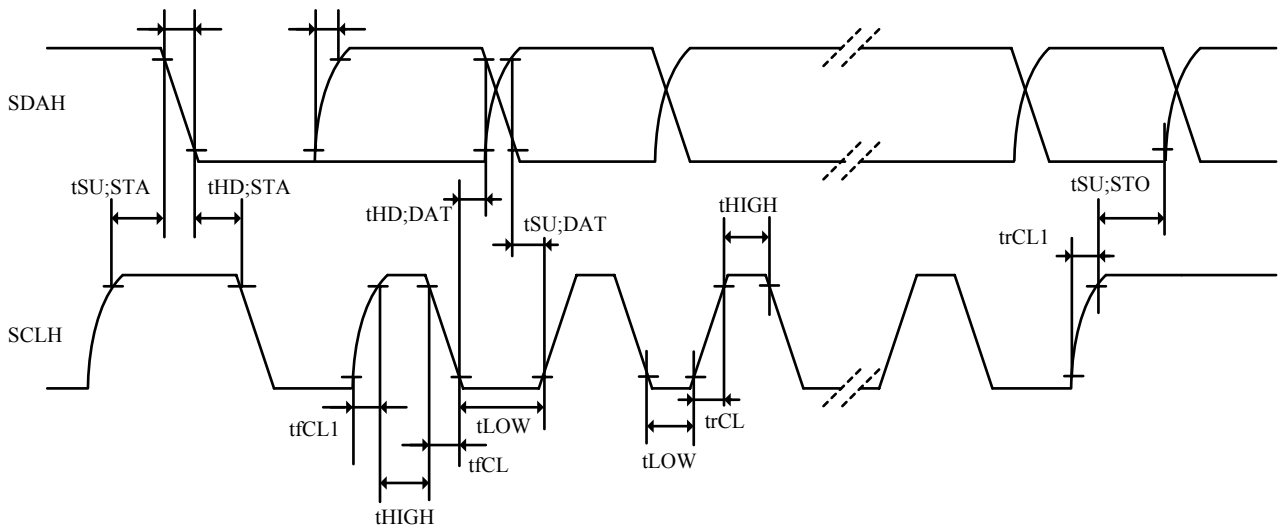
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCL clock frequency	fSCLH		0	-	3.4	MHz
Set-up time(repeated) START condition	tSU;STA		160	-	-	ns
Hold time(repeated) START condition	tHD;STA		160	-	-	ns
LOW period of the SCL clock	tLOW		160	-	-	ns
HIGH period of the SCL clock	tHIGH		60	-	-	ns
Data set-up time	tSU;DAT		10	-	-	ns
Data hold time	tHD;DAT		20	-	70	ns
Rise time of the SCL signal	trCL		10	-	40	ns
Rise time of the SCL signal after the acknowledge bit	trCL1		10	-	80	ns
Fall time of the SCL signal	tfCL		10	-	40	ns
Rise time of the SDA signal	trDA		10	-	80	ns
Fall time of the SCL signal	tfCL1		10	-	80	ns
Set-up time for STOP condition	tSU;STO		160	-	-	ns
Capacitive load for the SDA and SCL lines	Cb		-	-	100	pF
Capacitive load for the SDA and SCL lines	Cb2		-	-	400	pF
Tolerable spike width on bus	tSP		-	-	5	ns
Noise margin at the LOW level for each connected device (including hysteresis)	VnL		0.1VDD	-	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	VnH		0.2VDD	-	-	V

Note 1: Cb=100pF total capacitance of one bus line.

**Fig.1 I<sup>2</sup>C-Bus timing diagram (Fs-mode)**



**Fig.2 I<sup>2</sup>C-Bus timing diagram (Hs-mode)**



■ Example of typical characteristics

Fig.3 fOSC vs. VDD

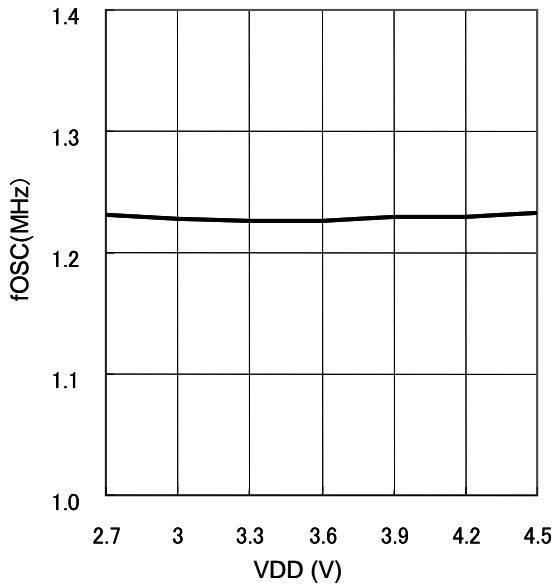


Fig.4 fOSC vs. temperature

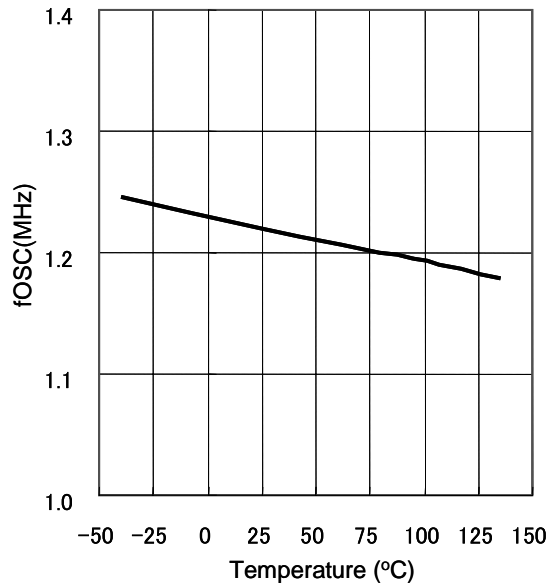


Fig.5 IDD vs. VDD

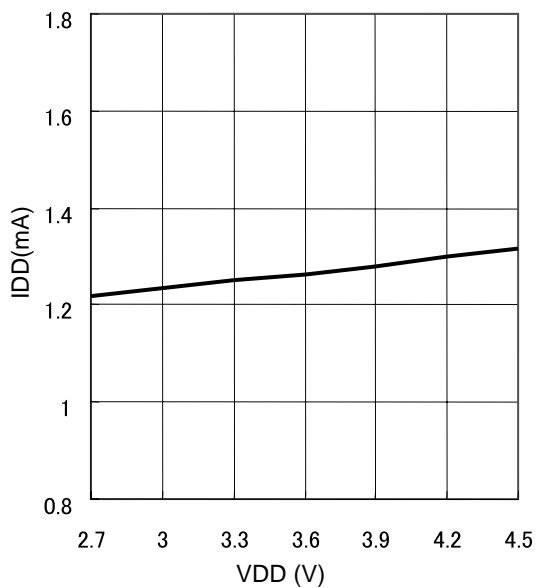
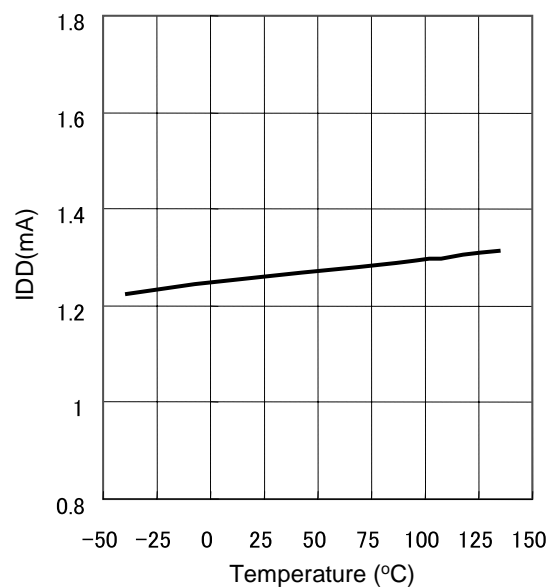
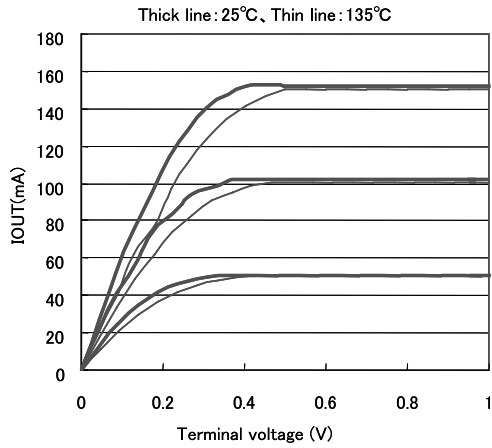


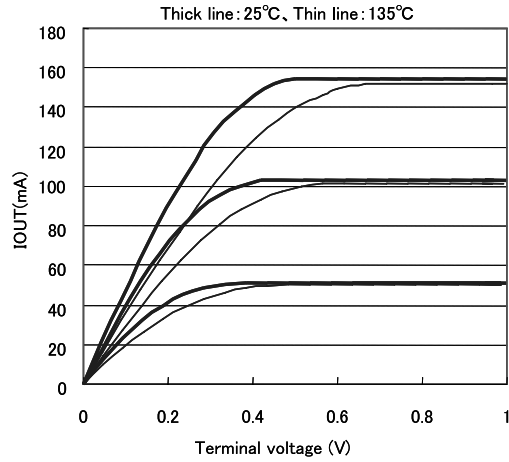
Fig.6 IDD vs. temperature



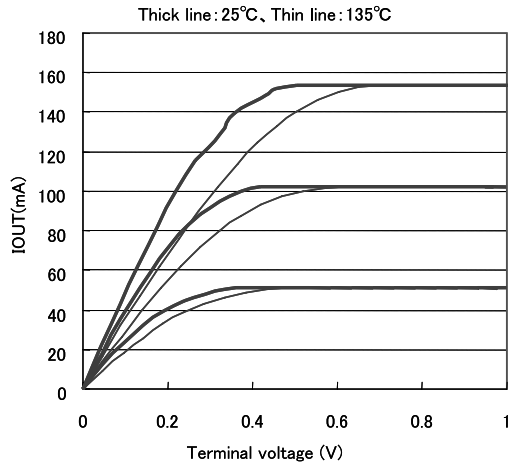
**Fig.7 IOUT(R) vs. Terminal voltage**



**Fig.8 IOUT(B) vs. Terminal voltage**



**Fig.9 IOUT(G) vs. Terminal voltage**



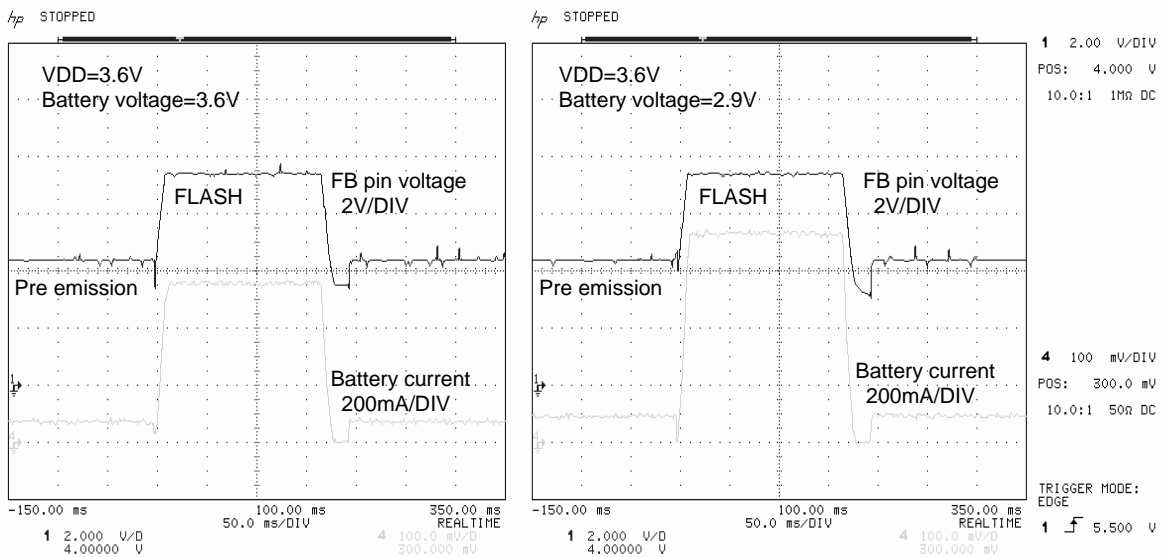
Voltage and current pulse of pre illuminating (RGB each 20mA) to flashing (R=80mA, G=120mA, B=75mA).

Pin: VDD1=VDD2=3.6V, ENR=ENG=ENB=XSTBY=3.6V, ADD0=ADD1=STRIG=0V

Resister setting: RSLSET:h'F1, GBSLSET: h'01, STSET: h'10, RGSASET:h'10, GBSASET: h'3F, RIDSET: h'E8,

GIDSET: h'E8, BIDSET: h'E8, RONSET: h'80, START: h'9F

Stroboscopic trigger: START:h'3F



**■ Cautions**

- Connect the power supply terminals (VDD1 pin and VDD2 pin) with the shortest distance and set terminals same potential.
- Connect the grounding terminals (PGND pin, SWGND pin, AGND pin, and LEDGND pin) with the shortest distance and set terminals same potential.
- Connect the LX terminals (LX1 pin, LX2 pin) with the shortest distance and set terminals same potential.
- Connect the CS terminals (CS1 pin, CS2 pin, and CSS pin) with the shortest distance and set terminals same potential.
- It is recommended to install a capacitor between the power supply terminal and grounding terminal.
- Position a bypass capacitor between the power supply terminal and grounding terminal close to the IC and use broad patterns.
- It is recommended to install an approximately 1000-pF capacitor between the Power supply terminal and ENx pin for countermeasure against static electricity.
- Use a broad and short patterns for the line that is connected from CVIN GND to CVIN GND through L and RCS.
- Position the Schottky-barrier diode (SBD) close to the CVOUT.
- Use patterns as broad and as short as possible for the power supply lines and grounding lines.
- Don't set input terminals (ENR pin, ENG pin, ENB pin, STRIG pin, SDA pin, SCL pin, ADD0 pin, and ADD1pin) floating.
- Apply the voltage to input terminals (ENR pin, ENG pin, ENB pin, STRIG pin, SDA pin, SCL pin, ADD0 pin, and ADD1pin) with input voltage range specified electric characteristics.
- In any cases including the timing of power on and power off, do not use absolute maximum ratings.
- Continuous running with the maximum output power may be caused exceeding maximum power dissipation. Be careful not to exceed maximum power dissipation in consideration of heat transfer resistance of a mounting board, ambient air temperature, and output electric power.
- Position the RIREF close to the IC to circumvent the effect of noise.

## ■ Important Notices

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- Personal computers
- Office automation equipment
- Telecommunication equipment [terminal]
- Test and measurement equipment
- Industrial control
- Audio visual equipment
- Consumer electronics

(ii) Measures such as fail-safe function and redundant design should be taken to ensure reliability and safety when SHARP devices are used for or in connection

with equipment that requires higher reliability such as:

- Transportation control and safety equipment (i.e., aircraft, trains, automobiles, etc.)
- Traffic signals
- Gas leakage sensor breakers
- Alarm equipment
- Various safety devices, etc.

(iii) SHARP devices shall not be used for or in connection with equipment that requires an extremely high level of reliability and safety such as:

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- Telecommunication equipment [trunk lines]
- Nuclear power control equipment
- Medical and other life support equipment (e.g., scuba).

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