IR3P69 CCD Signal Processing IC

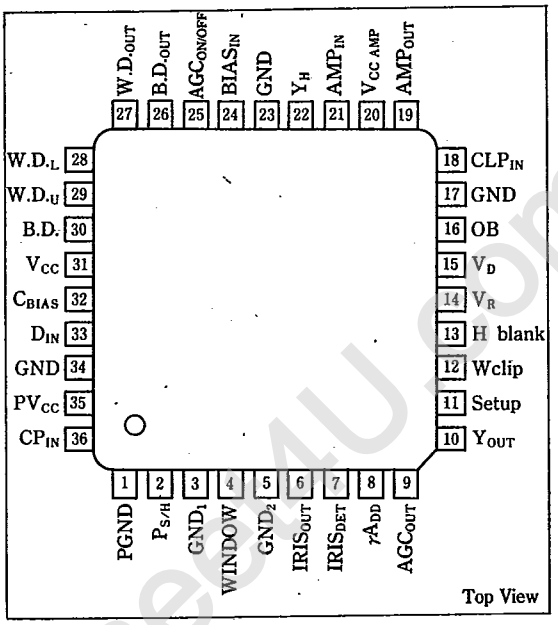
Description

The IR3P69 is a signal processing IC for monochrome CCD video cameras. With the output signal from CCD area sensor as its input, this IC performs a series of signal processing operations on its input through such circuits as clamp, sample-hold, amplifier, setup, and gamma corrects and outputs a brightness signal.

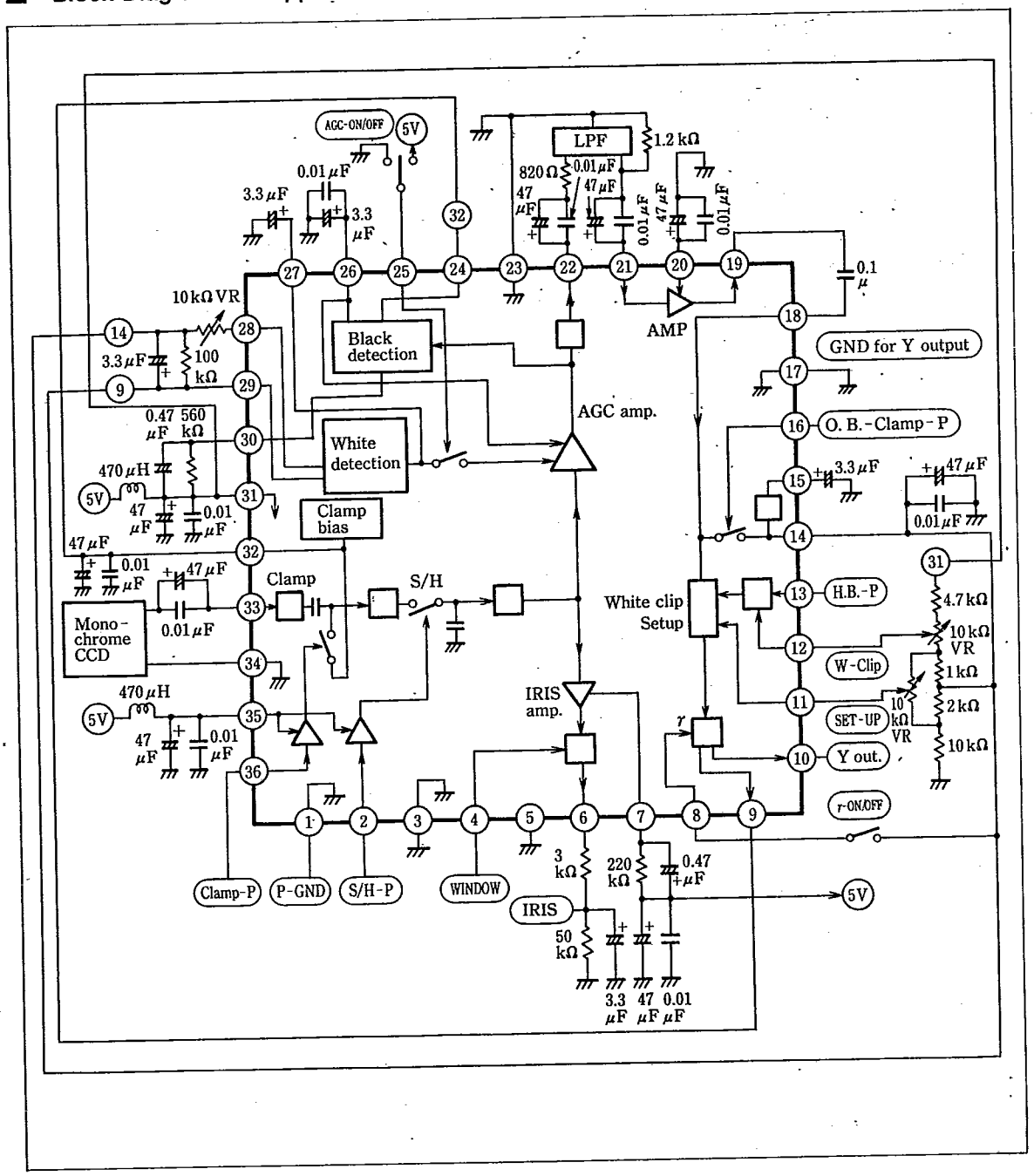
Features

1. Minimum operating input (CCD area sensor output) $20mV_{P-P}$
2. +5V single power supply
3. Built-in amplifier for iris
4. Window capability
5. Built-in clamp and sample-hold capacitor
6. Built-in 18dB amplifier
7. Built-in setup and white clip circuits
8. Built-in 2.2V reference voltage
9. Built-in gamma correction circuits
10. 36-pin quad flat package

Pin Connections



■ Block Diagram and Application



Pin Functions

Pin No.	Pin name	Function
1	Pulse GND	GND for pulse circuits
2	S/H pulse	Sample-hold pulse input
3	GND_1	GND for analog circuits
4	WINDOW	Window input for iris amp. Pin 4 going "High" causes the output signal to pass pin 6 and going "Low" outputs a black level potential.
5	GND_2	GND for analog circuits
6	Iris output	Output for iris amp
7	Iris detection	Detection for iris amp Controls input bias level for iris amp and standardizes pin 6 output black level.
8	γA_{DD}	Gamma correction control Connecting pin 8 to pin 14 turns gamma ON, opening turns gamma OFF.
9	Output for AGC	Provides output signal for AGC to white detection circuit. To be connected as well as pin 14 to white detection (pins 28 and 29) to perform white detection.
10	Y output	Brightness signal output (Sync. pulse not contained)
11	Setup	Sets the setup level
12	White clip	Sets the white clip level
13	H blanking	Input for horizontal blanking signal
14	V_R	Reference voltage output.
15	V_D	Reference voltage bias. Connects bypass capacitor with respect to GND.
16	O.B.	Optical, black, clamp pulse input. Clamps black level of pin 18.
17	GND for Y output	GND for Y output (pin 10)
18	Clamp input	Input for gamma correction, setup circuits
19	AMP output	Output for amp
20	V_{CC} for AMP	Connects amp power supply bypass capacitor
21	AMP input	Input for amp
22	Y_H output	Output for AGC amp
23	GND	GND for analog circuits
24	AGC clamp bias	Bias input for AGC amp. Connects pin 32 and bypass capacitor with respect to GND.
25	AGC ON/OFF	AGC ON/OFF control. Pin 25 going "High" turns AGC ON and going "Low" turns AGC OFF.
26	Black detection output	Output for black detection circuit. Controls bias potential of AGC amp.
27	White detection output	Output for white detection circuit. Controls AGC amp gain.
28	White detection lower	White detection
29	White detection upper	Receives output signal for AGC and detects white level.
30	Black detection	Black detection
31	V_{CC}	Power supply for analog circuits
32	S/H clamp bias	Bias for S/H, clamp circuits. Connnects bypass capacitor with respect to GND.
33	Input	Receives output signal from CCD.
34	GND for input	GND for input (pin 33)
35	Pulse V_{CC}	Power supply for pulse circuits
36	Clamp pulse	Input for clamp pulse

■ Functional Operation

Using the timing chart shown in Fig.1, let us describe a series of operations from pin 33 input to pin 19 AMP output.

The input signal (CCD signal) through pin 33 has its feedthrough level clamped by the clamp circuit, its signal level held by the S/H circuit to input to the AGC amp. The AGC amp amplifies a gain (0.2dB→18dB) to this faint input signal to keep Y_H output above a certain level controlled by white detection output.

The black detection circuit is a bias control circuit that stabilizes the black level of Y_H output.

After having its unwanted high frequency components eliminated by an external LPF, the Y_H output is applied as input to the AMP input at pin 21 and amplified to 17.5dB and appears as output at pin 19. It is finally sent to clamp input at pin 18.

The timing chart shown in Fig. 2 describes the operations from the clamp input to pin 18 to the Y output at pin 10.

The input signal to pin 18 has its black (optical) level clamped by the O. B. clamp circuit and blanked by H blanking. The white clip circuit sets the upper limit of white peak, while the setup circuit determines the setup level (raising the O. B. clamp edge higher than the black level).

And with γ on by the SW of pin 8, the signal goes through with gamma correction by γ ADD circuit and appears as Y output at pin 10. With γ OFF, it does not go through with gamma correction. Meanwhile, there is the other input signal from the S/H circuit going to the IRIS amp.

Following is a description of IRIS amp operation. The IRIS amp detects the black level of the input signal at pin 7 and stabilizes the black level of IRIS output at pin 6.

Also the WINDOW input to pin 4 provides gating to the IRIS output at pin 6.

Precautions

(1) To adjust the IRIS, monitor the AMP output at pin 19.

(2) Connect the capacitor of 0.01 μF or more to V_{CC} pin for AMP(pin 20).

(3) Connect the capacitor of 33 μF or more to the white detection output pin 27.

(4) The GND_2 (pin5) is a non-connection white detection output pin 27.

(5) Connect the L.P.F. which has a cut-off frequency of a half or less sampling frequency between pin 21 and 22.

(6) Special care must be taken for electro-static discharge.

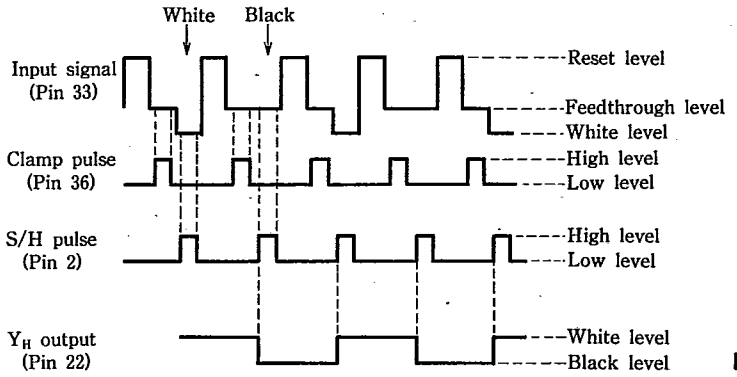


Fig. 1

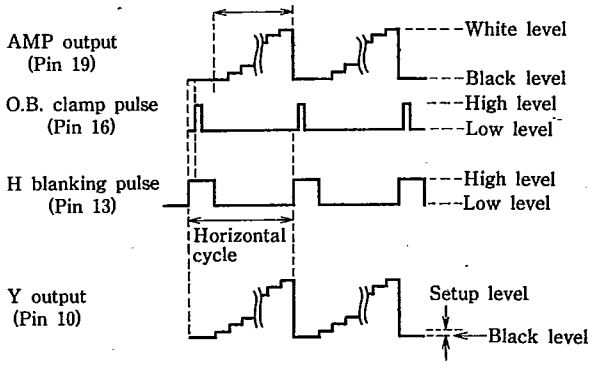


Fig. 2

■ Absolute Maximum Ratings

(Unless otherwise specified Ta=+25℃)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	PV_{CC}		7	V
	V_{CC}		7	V
Input voltage	V_{IP}	Input voltage≦supply voltage	−0.3~PV_{CC}	V
	V_I		−0.3~V_{CC}	V
Output current	I_{O1}	Applies to pins 6 and 10	−3	mA
	I_{O2}	Applies to pins 9, 19 and 22	−1	mA
Power dissipation	P_D	Ta=−10~+25℃	500	mW
P_D derating ratio	ΔP_D/℃	Ta=+25~+60℃	5	mW/℃
Operating temperature	T_{opr}		−10~+60	℃
Storage temperature	T_{stg}		−55~+150	℃

■ Electrical Characteristics (1)

(Unless othewise specified $PV_{CC}=V_{CC}$=4.75~5.25V, Ta=−10~+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage range	PV_{CC}		4.75	5	5.25	V
	V_{CC}		4.75	5	5.25	V
Supply current	PI_{CC}	Test circuit 1	3	7	11	mA
	I_{CC}		12	20	28	mA
Clamp circuit						
Low range attenuation	G_{LF}	Test circuit 2	−20	−25	−	dB
Input range	V_{I33}		−	−	0.3	V_{P-P}
S/H clamp bias	$V_{S/H}$	V_{CC}=5V	2.95	3.1	3.25	V
AGC amplifier						
Minimum gain	AV_{MIN}	Pin 25→GND Input 0.2V_{P-P}, f=1MHz	−4	−2	0	dB
Maximum gain	AV_{MAX}	Pin 25→V_{CC} Input 0.02V_{P-P}, f=1MHz	16	18	20	dB
Output resistance	R_{OUT}		90	150	240	Ω
Output dynamic range	D_{R22}		0.6	1.0	−	V_{P-P}
Frequency bandwidth	BW_{22}	(Note 1)	10	15	−	MHz
Black level	AGC-B	V_{CC}=5V	2.1	2.3	2.5	V
IRIS amplifier						
Gain	AV_6	Test circuit 3	10.5	12.5	14.5	dB
Output dynamic range	DR_6		1.0	1.6	−	V_{P-P}
Frequency bandwidth	BW_6	(Note 1)	0.8	1.3	1.8	MHz
Black level	IRIS-B	V_{CC}=5V	1.95	2.15	2.35	V
Amplifier						
Input resistance	R_{IN}		5	10	15	kΩ
Input voltage	V_{I21}		−	−	0.15	V_{P-P}
Gain	AV_{19}	Test circuit 4	15.5	17.5	19.5	dB
Output dynamic range	DR_{19}	V_{CC}=5V	1.0	1.6	−	V_{P-P}
Frequency bandwidth	BW_{19}	(Note 1)	10	15	−	MHz
Reference voltage circuit						
V_R output voltage	V_R	V_{CC}=5V	1.95	2.15	2.35	V
V_R output variation		I_O=0.1mA and I_O=−0.1mA	−	±0.05	±0.15	V
V_D voltage	V_{15}	V_{CC}=5V	1.95	2.15	2.35	V

(Unless otherwise specified $PV_{CC}=V_{CC}=4.75\sim5.25V$, Ta=−10~+60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Setup circuit						
Input current	I_{I11}		−	−0.6	−2.0	μA
Setting range	S_V		0	−	200	mV_{P-P}
Temperature characteristics		Setup: $100mV_{P-P}$	−	−	±50	
White clip circuit						
Input current	I_{I12}	Pin 12→V_{CC}	−	1.5	5.0	μA
Setting range	W_C		0.3	−	1.5	V_{P-P}
Temperature characteristics		White clip: $1V_{P-P}$	−	−	±0.1	V_{P-P}
γ A_{DD} circuit						
Gain 1	γ_1	Gradient for clamp input of $V_R+0.05V$	0.8	1	1.2	time
Gain 2	γ_2	Gradient for clamp input of $V_R+0.4V$	0.3	0.4	0.5	time
Gain 3	γ_3	Gradient for clamp input of $V_R+0.8V$	0.15	0.2	0.25	time
γ Correction variation		Output at pin 10 for the input at pin 18 of $V_R+0.8V_{P-P}$	−5	−	+5	%
Frequency bandwidth	BW_9, BW_{10}	For γ_1 (Note 1)	4	−	−	MHz
Output dynamic range	DR_9, DR_{10}	Pin 8→V_{CC} Pin 12→V_{CC}	1.0	1.6	−	V_{P-P}
γ output black level DC voltage	Y-B	$V_{CC}=5V$	1.8	2.0	2.2	V
γ Output sink current	Y_I	Distortion 1%	−	−	0.1	mA
Pulse amplifier 1, 2						
Input "High" voltage	V_{IH}		3.0	−	PV_{CC}	V
Input "Low" voltage	V_{IL}		−0.1	−	0.7	V
Input current	I_I	Input voltage; 0V	−0.4	−0.8	−1.2	mA
H blanking circuit						
H. B. input "High" voltage	V_{HBH}		2.7	−	PV_{CC}	V
H. B. input "Low" voltage	V_{HBL}		−0.1	−	0.5	V
H. B. input current	I_{HB}	Input voltage; 0V	0.2	0.4	0.6	mA
O. B. clamp circuit						
O. B. input "High" voltage	V_{OBH}		4.0	−	V_{CC}	V
O. B. input "Low" voltage	V_{OBL}		−0.1	−	0.7	V
WINDOW circuit						
Window "High" voltage	V_{WIH}		2.7	−	V_{CC}	V
Window "Low" voltage	V_{WIL}		−0.1	−	0.5	V

Note 1 Frequency bandwidth: The frequency at which the gain is 3dB down from the gain at 100kHz. If it's variable gain, it refers to maximum gain.

Electrical Characteristics (2)

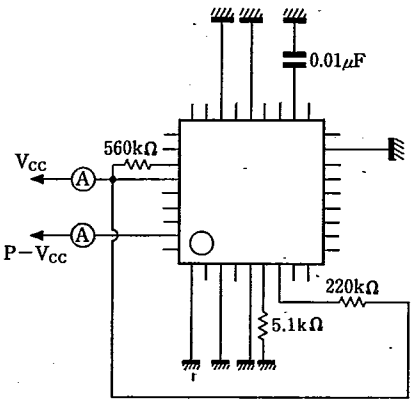
(Unless otherwise specified $PV_{CC}=V_{CC}=5V$, Ta=+25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	PI_{CC}		5	7	9	mA
	I_{CC}		14	20	26	mA
Clamp circuit						
Low range attenuation	G_{LF}	Attenuation from f=10MHz to f=100kHz	−23	−25	−	dB
Input range	V_{I33}		−	−	0.4	V_{P-P}
S/H clamp bias	$V_{S/H}$		2.97	3.1	3.23	V
AGC amplifier						
Minimum gain	AV_{MIN}	Pin 25→GND Input $0.2V_{P-P}$, f=1MHz	−3	−2	−1	dB
Maximum gain	AV_{MAX}	Pin 25→V_{CC} Input $0.02V_{P-P}$, f=1MHz	17	18	19	dB
Output resistance	R_{OUT}		100	150	220	Ω
Output dynamic range	DR_{22}		0.7	1.1	−	V_{P-P}
Frequency bandwidth	BW_{22}	(Note 1)	12	15	−	MHz
Black level	AGC-B		2.15	2.3	2.45	V
IRIS amplifier						
Gain	AV_6		11.0	12.5	14.0	dB
Output dynamic range	DR_6		1.1	1.7	−	V_{P-P}
Frequency bandwidth	BW_6	(Note 1)	0.9	1.3	1.7	MHz
Black level	IRIS-B		2.0	2.15	2.3	V
Amplifier						
Input resistance	R_{IN}		7	10	13	kΩ
Input voltage	V_{I21}		−	−	0.15	V_{P-P}
Gain	AV_{19}	Test circuit 4	16	17.5	19	dB
Output dynamic range	DR_{19}		1.1	1.7	−	V_{P-P}
Frequency bandwidth	BW_{19}	(Note 1)	12	15	−	MHz
Reference voltage circuit						
V_R output voltage	V_R		2.0	2.15	2.3	V
V_R output variation		I_O=0.1mA and I_O=−0.1mA	−	±0.05	±0.1	V
V_D terminal voltage	V_{15}		2.0	2.15	2.3	V
Setup circuit						
Input current	I_{I11}		−	−0.6	−1.5	μA
Setting range	SV		0	−	220	mV
White clip circuit						
Input current	I_{I12}	Pin 12→V_{CC}	−	1.5	4.0	μA
Setting range	WC		0.25	−	1.55	V
γ A_{DD} circuit						
Gain 1	γ_1	Gradient for clamp input of V_R+0.05V	0.85	1	1.15	time
Gain 2	γ_2	Gradient for clamp input of V_R+0.4V	0.32	0.4	0.48	time
Gain 3	γ_3	Gradient for clamp input of V_R+0.8V	0.16	0.2	0.24	time
γ correction variation		Output at pin 10 for the input at pin 18 of V_R+$0.8V_{P-P}$	−4	−	+4	%

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Frequency bandwidth	BW_7, BW_{10}	For γ_1(Note 1)	4.5	–	–	MHz
Output dynamic range	DR_9, DR_{10}	Pin 8→V_{CC}, Pin 12→V_{CC}	1.1	1.7	–	V_{P-P}
Y output black level DC voltage	Y-B		1.9	2.0	2.1	V
Y output sync current	Y_I	Distortion 1%	–	–	0.2	mA
Pulse amplifier 1, 2						
Input "High" voltage	V_{IH}		2.9	–	PV_{CC}	V
Input "Low" voltage	V_{IL}		−0.1	–	0.8	V
Input current	I_I	Input voltage 0V	−0.5	−0.8	−1.1	mA
H blanking circuit						
H. B. input "High" voltage	V_{HBH}		2.6	–	PV_{CC}	V
H. B. input "Low" voltage	V_{HBL}		−0.1	–	0.6	V
H. B. input current	I_{HB}	Input voltage 0V	0.25	0.4	0.55	mA
O. B. clamp circuit						
O. B. input "High" voltage	V_{OBH}		3.9	–	V_{CC}	V
O. B. input "Low" voltage	V_{OBL}		−0.1	–	0.6	V
WINDOW circuit						
WINDOW "High" voltage	V_{WIH}		2.6	–	V_{CC}	V
WINDOW "Low" voltage	V_{WIL}		−0.1	–	0.6	V

■ Test Circuits

(1) Supply current

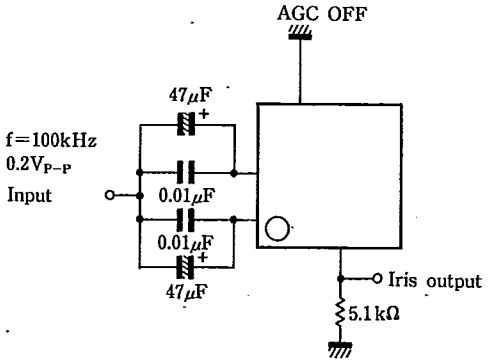


(2) AGC amplifier's I/O characteristics, Y correction's I/O characteristics.

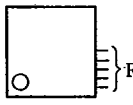
Apply CCD signal and each pulse signal, and measure on the basic connection diagram.

(Measurement) Observe the Y_H output on the spectrum analyzer. Define the level difference between f=10MHz and f=100kHz to be the low range attenuation.

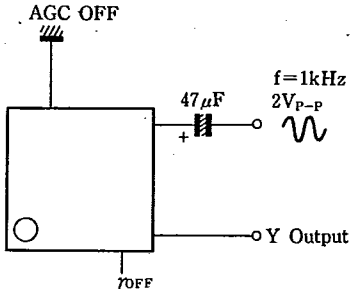
(3) IRIS amp gain, I/O characteristics



Note 1



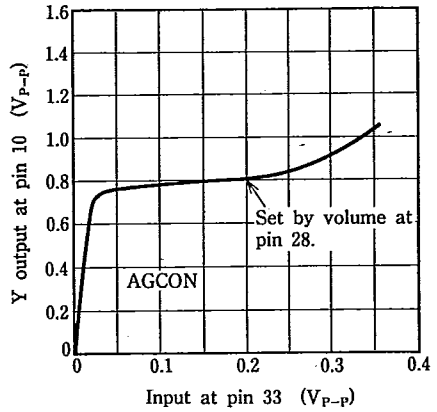
(4) Setup, white clip characteristics



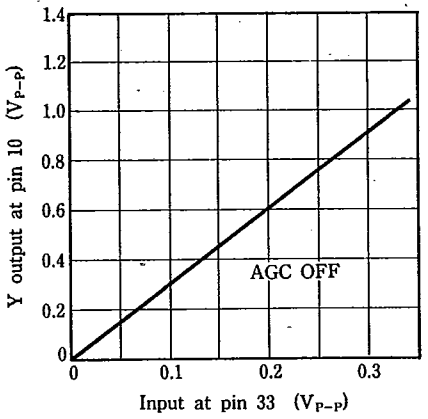
Note 2 The pins that are not shown in the above test circuit are subject to the same conditions as they are in the basic connection diagram. For items not given above, refer to the above test circuit and basic connection diagram.

Electrical Characteristic Curves

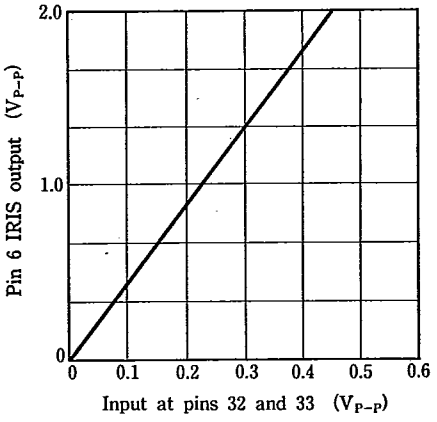
AGC amp I/O Characteristics (Y OFF)



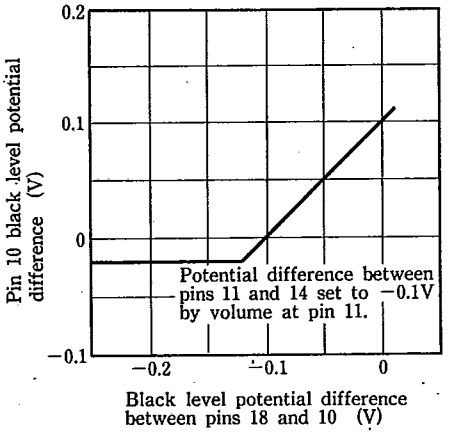
AGC amp I/O Characteristics (Y OFF)



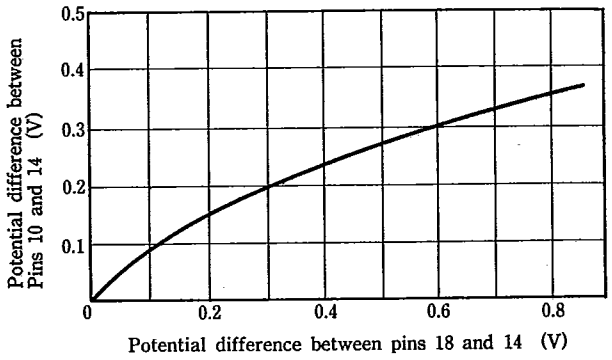
IRIS amp I/O Characteristics



Setup Characteristics (Y OFF)



Y correction I/O Characteristics



White clip Characteristics (Y OFF)