International
IOR Rectifier

REFERENCE DESIGN

IRAUDAMP3

120W x 6 Channel Class D Audio Power Amplifier using IRS20124S and IRF6645

By

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The IRAUDAMP3 reference design is an example of a complete six-channel 120W half-bridge Class D audio power amplifier. The reference design is intended to demonstrate how to use the IRS20124S, implement protection circuits, and design an optimum PCB layout using IRF6645 DirectFET® MOSFETs. The modular design consists of a motherboard with three identical daughter boards. The resulting design requires no heat-sinking for normal operation. The reference design includes all the required housekeeping power supplies for ease of use.

Introduction

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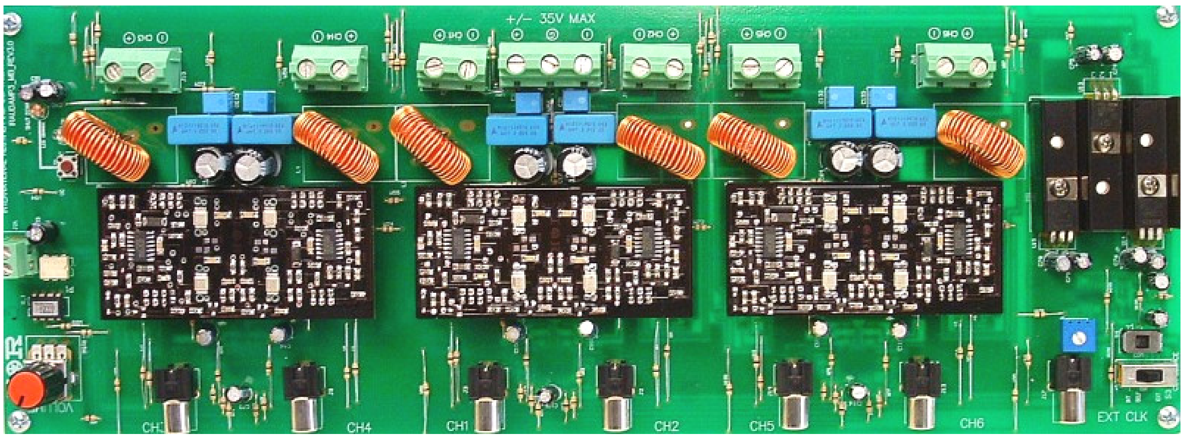


Applications

AV receivers
Home theater systems
Mini component stereos
Sub-woofers

Features

Output power:	120W x 6 Channels, (THD = 1%)
Residual noise:	56μV, IHF-A weighted, AES-17 filter
Distortion:	0.01% THD+N @ 60W, 4Ω
Efficiency:	94% @ 120W, 4Ωsingle channel driven, Class D stage
Multiple protection features:	OCP, OVP, UVP, DC protection, OTP
PWM modulator:	Self-oscillating half-bridge topology with optional clock synchronization

Specifications

General Test Conditions (unless otherwise noted)		Notes / Conditions
Supply Voltage	±35V	
Load Impedance	4Ω	
Self-Oscillating Frequency (Adjustable)	400kHz	No input signal
Gain Setting	26dB	1Vrms input sensitivity

Electrical Data	(Typical)	Notes / Conditions
IR Devices Used		IRS20124S gate driver, IRF6645 DirectFET MOSFET
Modulator		Self-oscillating, 2nd order Sigma-Delta modulation, analog input
Power Supply Range	± 25-35V	
Output Power CH1-6: (1% THD+N)	120W	1kHz
Output Power CH1-6: (10% THD+N)	170W	1kHz
Rated Load Impedance	4Ω	
Damping Factor	40	1kHz, relative to 4Ω load
Supply Current	<250mA	No input signal
Total Idle Power Consumption	14W	No input signal
Board Efficiency	94%	Single channel driven, 120W, Class D stage

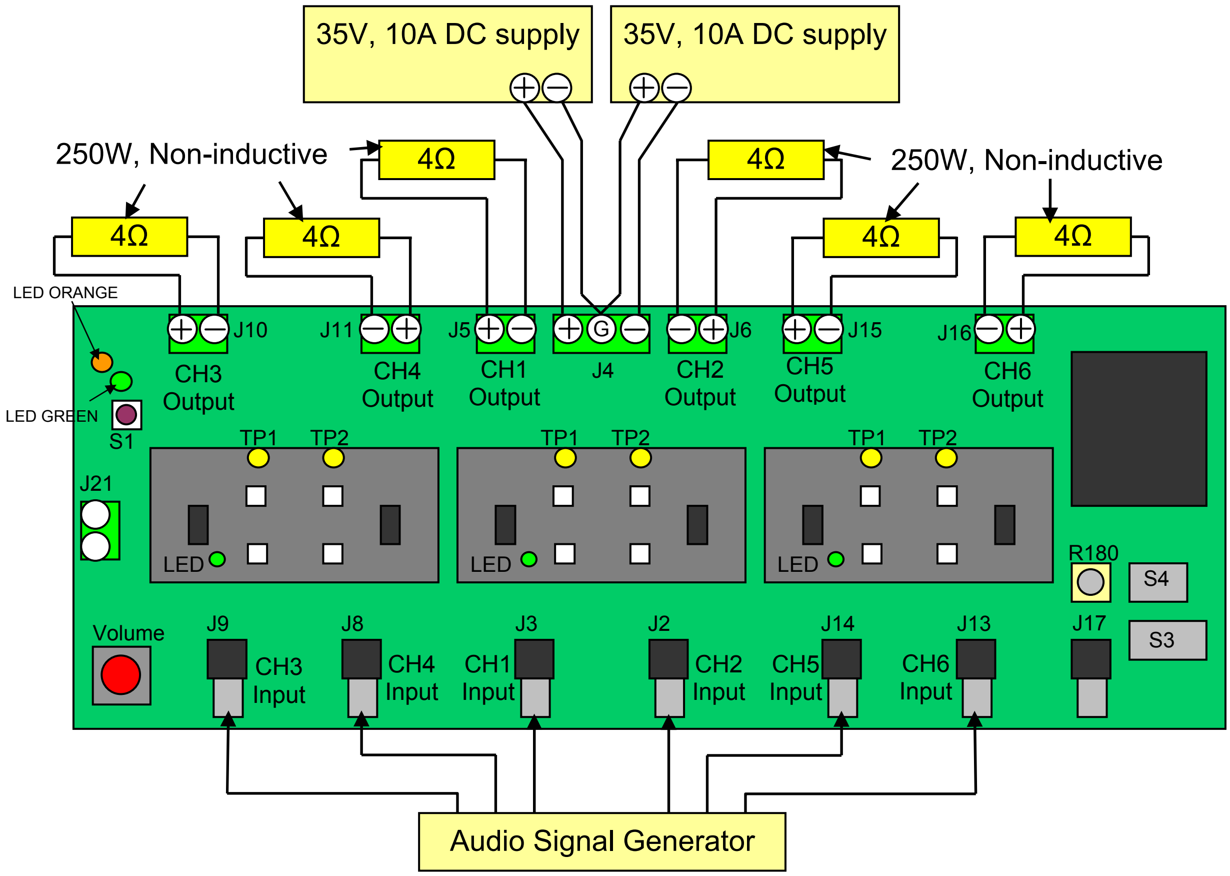
Audio Performance	(Typical)	Notes / Conditions
THD+N, 1W THD+N, 10W THD+N, 60W	0.006% 0.005% 0.010%	1kHz, single channel driven
Dynamic Range	112dB	A-weighted, AES-17 filter, single channel operation
Residual Noise 20Hz - 20kHz BW, A-Weighted	97μV 56μV	Self-oscillating – 400kHz internal clock – 395kHz
Channel Separation	87dB 72dB	100Hz 10kHz
Frequency Response : 20Hz-20kHz : 20Hz-40kHz	±1dB ±3dB	1W, 4Ω - 8Ω Load

Thermal Performance	(Typical)	Notes / Conditions
Idling	T_C =33°C T_{PCB}=42°C	No signal input, TA=25°C
2ch x 15W (1/8 Rated Power)	T_C =58°C T_{PCB}=77°C	Continuous
2ch x 120W (Rated Power)	T_C =79°C T_{PCB}=101°C	90 seconds

Physical Specifications	(Typical)	Notes / Conditions
Dimensions	13.7”(L) x 5.0”(W)	

Note: Specifications are typical and not guaranteed.

Connection Diagram



Typical Test Setup

Pin Description

CH-1 IN	J3	Analog Input for CH-1
CH-2 IN	J2	Analog Input for CH-2
CH-3 IN	J9	Analog Input for CH-3
CH-4 IN	J8	Analog Input for CH-4
CH-5 IN	J14	Analog Input for CH-5
CH-6 IN	J13	Analog Input for CH-6
POWER	J4	Positive and Negative Supply (+B / -B)
CH-1 OUT	J5	Output for CH-1
CH-2 OUT	J6	Output for CH-2
CH-3 OUT	J10	Output for CH-3
CH-4 OUT	J11	Output for CH-4
CH-5 OUT	J15	Output for CH-5
CH-6 OUT	J16	Output for CH-6
EXT CLK	J17	External Clock Sync
DCP OUT	J21	DC Protection Relay output

Power-on Procedure

1. Apply ±35V at the same time
2. Apply audio signal

Note: Improper power on procedure could result start up failure.

Power-off Procedure

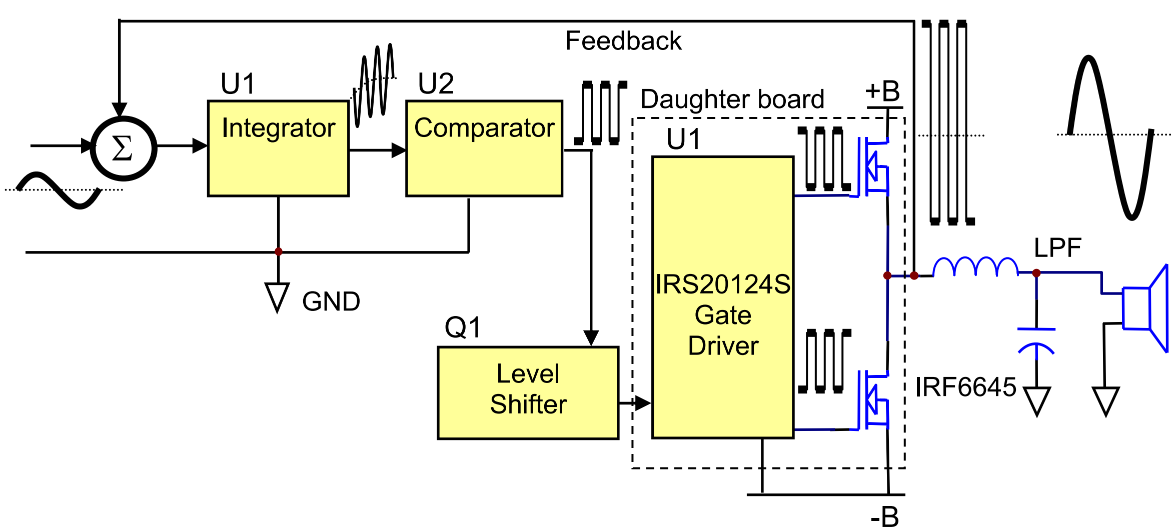
1. Remove audio input signal
2. Turn off ±35V at the same time

Functional Description

Class D operation

Referring to CH-1 as an example, the op-amp U1 forms a front-end second-order integrator with C1 & C2. This integrator receives a rectangular waveform from the Class D switching stage and outputs a quadratic oscillatory waveform as a carrier signal. To create the modulated PWM, the input signal shifts the average value of this quadratic waveform (through gain relationship between R28 and R9 + R1) so that the duty varies according to the instantaneous value of the analog input signal. The signal is then quantized by the threshold of the CMOS inverter U2. The transistor Q1 level-shifts the PWM signal down to the IRS20124S gate-driver (referenced to –B) which internally splits this signal into two signals, with opposite polarity and added deadtime, for high-side and low-side MOSFET gate signals respectively.

The IRS20124S drives two IRF6645 DirectFET MOSFETs in the power-stage to provide the amplified digital PWM waveform. The amplified analog output is re-created by demodulating the amplified PWM. This is done by means of the LC low-pass filter (LPF) formed by L1 and C18, which filters out the Class D switching carrier signal.



Simplified block diagram of Class D amplifier

Power Supplies

The IRAUDAMP3 has all the necessary housekeeping power supplies onboard and only requires a pair of symmetric dual power supplies ranging from ±25V to ±35V (+B, GND, -B) for operation. The internally generated housekeeping power supplies include a ±5V supply for signal processing, while a +12V supply, referenced to –B, is included to supply the Class D gate driver stage.

For the externally applied power, a regulated power supply is preferable for performance measurements, but not always necessary. The bus capacitors, C16-17 (C40-41, C64-64), on the board along with high-frequency bypass caps, C88-89 (C90-91, C92-93) are designed to take care of the high-frequency ripple-current components from switching action only. A set of bus capacitors having enough capacitance to handle the audio ripple current must be placed outside the board if an unregulated power supply is used. At initial power-on, the shutdown condition (orange LED) will latch for about three seconds before starting normal operation. Always apply supply voltages before applying any audio signals and always remove audio signals prior to removing the power supplies.

Bus Pumping

Since the IRAUDAMP3 is a half bridge configuration, bus pumping occurs when the amplifier outputs a low frequency signal below 100Hz. Under normal operation during one half cycle, energy flows from one supply, through the load and into the other supply, thus causing a voltage imbalance by pumping up the bus voltage. This condition is reversed during the next half cycle (resulting in bus pumping of the other supply). Bus pumping is worsened under the following conditions:

– Lower frequency (bus pumping continues longer)
– Higher power / output voltage and / or lower load impedance (more energy is transferred between supplies)
– Smaller bus capacitors (the same energy will cause a larger voltage increase)

The IRAUDAMP3 has protection features that will shutdown the switching operation if the bus voltage becomes too high (> 40V) or too low (< 20V). One of the easiest countermeasures is to drive both of the channels out of phase so that the energy flow from one channel is consumed by the other and does not return to the power supply.

Input

A proper input signal is an analog signal below 20kHz, up to ±3.5V peak, having a source impedance of less than 600Ω. A 30kHz to 60kHz input signal can cause LC resonance in the output LPF, resulting in an abnormally large amount of reactive current flowing through the switching stage (especially at 8Ω or open load), causing OCP activation. The IRAUDAMP3 has an RC (Zobel) network, to damp the resonance and protect the board in such a condition. However, these supersonic input frequencies should be avoided. The input to each of the six channels is made using a separate mono RCA connector. Although all six channels share a common ground, it is necessary to connect each channel separately to limit noise and crosstalk between channels.

Output

All the outputs for the IRAUDAMP3 are single-ended and therefore have terminals labeled (+) and (-) with the (-) terminal connected to Power Ground. Each channel is optimized for a 4Ω speaker load for a maximum output power (120W), but is capable of operating with higher load impedances, at reduced power, at which point, the frequency response will have a small peak at the corner frequency of the output LC LPF. The IRAUDAMP3 is stable with capacitive loading, however, it should be realized that the frequency response will be degraded by heavy capacitive loading of more than 0.1µF

Gain Setting / Volume Control

The IRAUDAMP3 has an internal volume control (potentiometer R156 labeled 'VOLUME') for gain adjustment. Gain settings for all six channels are tracked and controlled by the volume control IC setting the gain from the micro controller IC, U1. The maximum volume setting (fully clockwise) corresponds to a total gain of +37.9dB (78.8V/V). The total gain is a product of the power stage gain, which is a constant +23.2dB, and the input-stage gain is directly controlled by the volume adjustment. The volume range is about 100dB with minimum volume setting to 'mute' the system with an overall gain of less than -60dB. For best performance in your testing, the internal volume control should be set to a gain of 21.9V/V, or 1Vrms input will result in rated output power (120W into 4Ω),allowing for a >11dB overdrive.

Self-Oscillating PWM modulator

The IRAUDAMP3 Class D audio power amplifier is based on a self-oscillating type PWM modulator for the lowest component count and a robust design. This topology is basically an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The benefit of Sigma-Delta modulation in comparison to the carrier signal-based modulator is that all the error in the audible frequency range is shifted away into the inaudible upper frequency range by the nature of its operation, and applies a sufficient amount of correction.

The self-oscillating frequency is a determined by the total delay time in the control loop of the system. The delay of the logic circuits, the IRS20124S gate-driver propagation delay, the IRF6645 DirectFET MOSFET switching speed, the time constant of the front end integrator (e.g. R15 + R19, C1 and C2 for Ch-1) and supply-voltages are all critical factors of the self-oscillating frequency. Under nominal conditions, the switching-frequency is around 400kHz with no audio input signal.

Adjustments of Self-Oscillating Frequency

The PWM switching frequency in this type of self-oscillating scheme greatly impacts audio performance, both in absolute frequency and frequency relative to the other channels. At higher frequencies, distortion due to switching time becomes significant, while at lower frequencies, the bandwidth of the amplifier suffers. In relative terms, interference between channels is most significant if the relative frequency difference is within the audible range. Normally when adjusting the self-oscillating frequency of the different channels, it is best to either match the frequencies accurately, or have them separated by at least 25kHz. In this design, it is possible to change the self-oscillating frequency from about 180kHz up to 470kHz.

Potentiometers for adjusting self-oscillating frequency	
Component Number	Adjustment
R19	Switching Frequency for CH-1*
R20	Switching Frequency for CH-2*
R54	Switching Frequency for CH-3*
R55	Switching Frequency for CH-4*
R86	Switching Frequency for CH-5*
R87	Switching Frequency for CH-6*
*Adjustments have to be done at an idling condition with no signal input.	

Switches and Indicators

There are three different *indicators* on the reference design:

- An orange LED, signifying a fault / shutdown condition when lit
- A green LED on the motherboard indicates power is applied to the motherboard
- Green LEDs on each of the three daughter boards, signify power is on

There are three *switches* on the reference design:

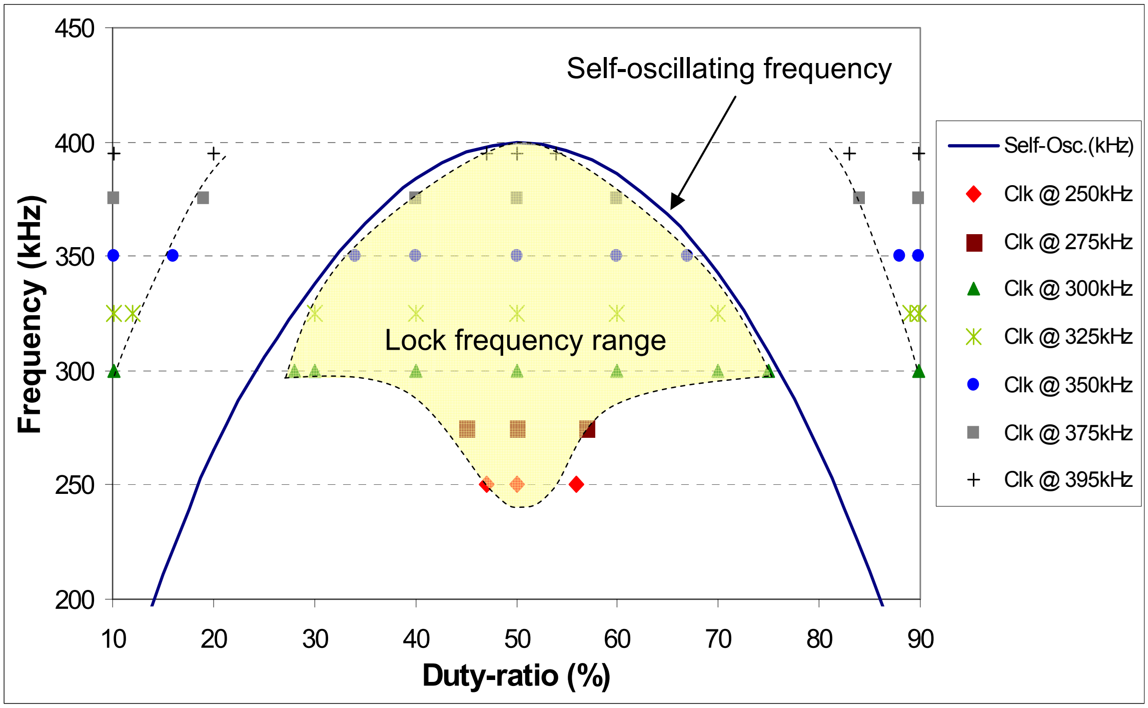
- Switch S1 is a "Shutdown" push-button. Pushing this button has the same effect as having a fault condition. The circuit will re-start about 3 seconds after the shutdown button is released.
- Switch S2: Internal clock-sync frequency selector. This feature demonstrates avoiding AM radio interference by slightly modifying the switching frequency. With S3 is set to INT, the two settings 'H' and 'L' will modify the internal clock frequency by about 20kHz to 40kHz, either higher 'H' or lower 'L'. The actual internal frequency is set by potentiometer R180 - 'INT OSC FREQ'.
- Switch S3: Oscillator selector – This 3-position switch selects between the internal self oscillator ('SELF'), internal- ('INT') or external clock-sync ('EXT').

Switching Frequency Lock / Synchronization Feature

For single-channel operation, the self-oscillating switching scheme will yield the best audio performance. The self-oscillating frequency does, however, change with duty ratio. This varying frequency can interfere with AM radio broadcasts. A constant switching frequency, with its harmonics that are shifted away from the AM carrier frequency, is preferred.

Apart from AM broadcasts, the addition of multiple channels can also reduce audio performance at low power, and can lead to increased residual noise. Both characteristics of the self-oscillating switching scheme can be improved through the addition of clock frequency locking / synchronization.

Please note that the switching frequency lock / synchronization feature is not possible for all frequencies and duty ratios, but only operates within a limited frequency and duty-ratio range below the self-oscillating frequency (see figure below).



Typical lock frequency range vs. PWM duty ratio for different internal clock frequencies

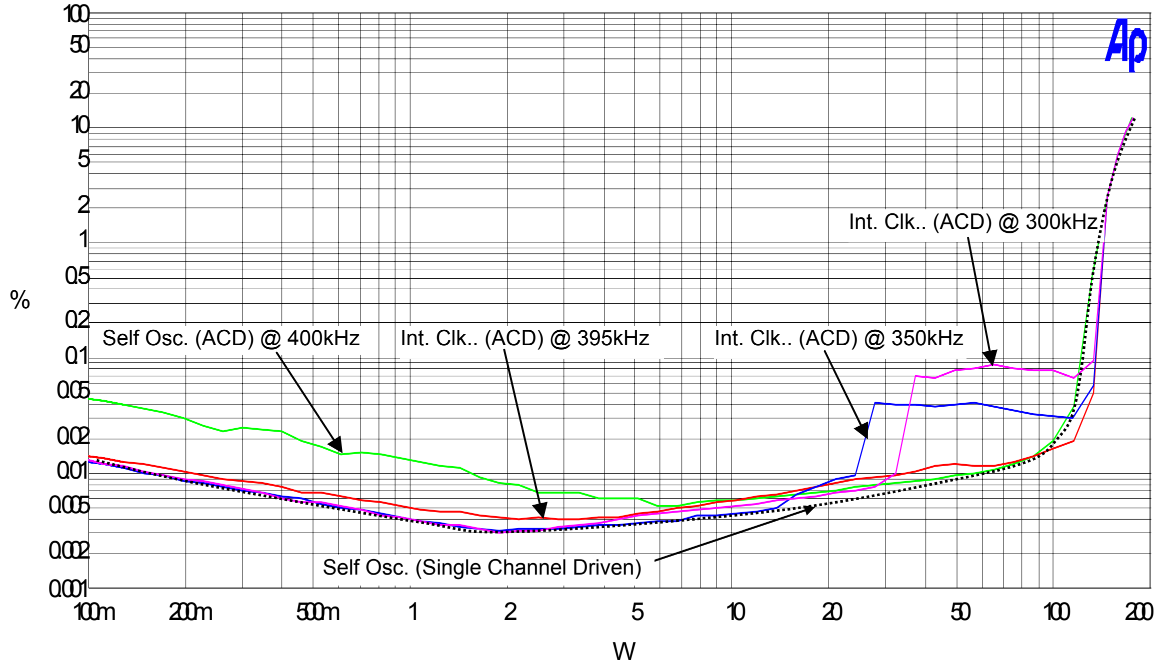
(Self-oscillating frequency set to 400kHz with no input)

Considering the THD+N ratio vs. output power results below, it can be seen that having all channels driven (ACD) with the self oscillator, noise levels increase, especially below the 5W range. Residual noise doubles (see Specifications – Audio Performance) compared to having only a single channel driven. By locking the oscillator frequency, the residual noise can be lowered to that of a single channel driven system. The output power range, for which the frequency locking is successful, depends on how much lower the locking frequency is with respect to the self-oscillating frequency. As the locking frequency is lowered (from 395kHz to 350kHz and then 300kHz), the output power range (where locking is achieved) is extended. Once locking is lost, however, the audio performance is reduced, with lower locking frequencies leading to larger THD.

In the IRAUDAMP3, this switching frequency lock / synchronization feature can be achieved through the use of either an internal or an external clock input (selectable through S3). If internal (INT) clock is selected, the internally generated clock signal will be used and can be adjusted by setting potentiometer R180 - 'INT OSC FREQ'. If external (EXT) clock signal is selected, a 0-5V, square-wave (50% duty-ratio) logic-signal must be applied to J17.

Offset Null (DC Offset)

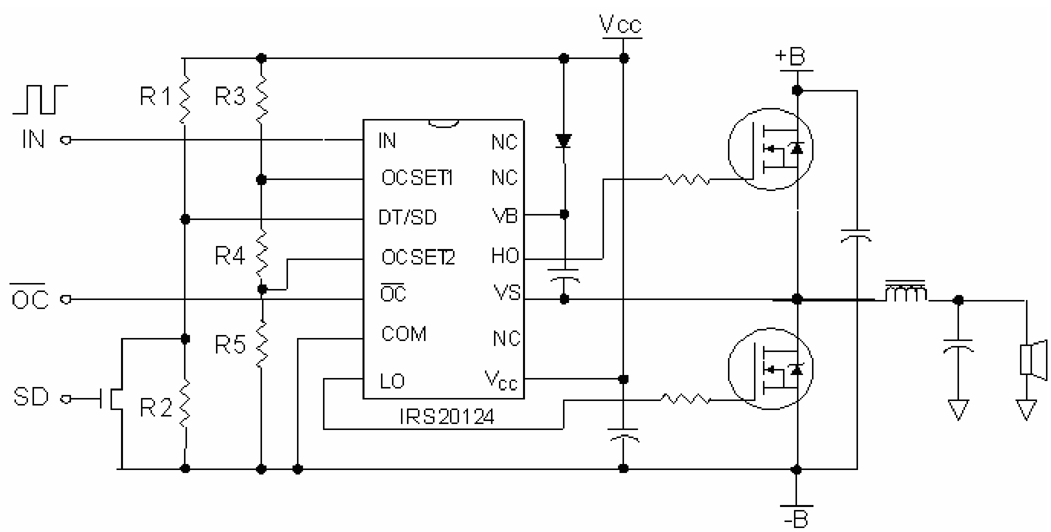
The IRAUDAMP3 has been designed such that no output-offset nulling is required. The reference boards will have DC offsets tested to be less than ±50mV.



THD+N ratio vs. output power for different switching frequency lock / synchronization conditions

Gate Driver IC

The IRAUDAMP3 uses the IRS20124S, which is a high-voltage (200V), high-speed power MOSFET gate driver with internal deadtime and shutdown functions specially designed for Class D audio amplifier applications. In this design, deadtime can be minimized to optimize performance while limiting shoot-through. Because of this, there is no gate timing adjustment on the board. Selectable deadtime through the DT/SD pin voltage is an easy and reliable function which requires only two external resistors, R1 and R2. The bi-directional current sensing feature is also selected externally by resistors R3, R4, and R5 and can protect the IRS20124S and shutdown the DirectFET MOSFETs during over-current conditions.

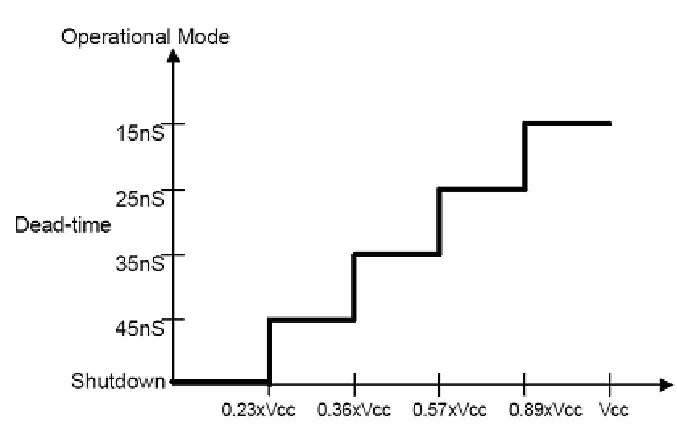


System-level view of gate driver IRS20124S

Selectable Deadtime

The DT/SD pin provides two functions: 1) setting deadtime and 2) selecting shutdown. The IRS20124S determines its operation mode based on the voltage applied to the DT/SD pin. An internal comparator translates which mode is being used by comparing internal reference voltages. Threshold voltages for each mode are set internally by a resistive voltage divider off V_{CC}, negating the need for a precise, absolute voltage to set the mode.

1) Threshold voltages for the mode selection are set internally, based on different ratios of V_{CC} as indicated in the diagram below. In order to avoid drift from the input bias current of the DT/SD pin, a bias current of greater than 0.5mA is suggested for the external resistor divider circuit. Suggested values of resistance that are used to set a deadtime are given below. Resistors with up to 5% tolerance can be used.



Deadtime / operation mode settings vs $V_{DT/SD}$ voltage

Dead-time mode	Dead-time	R1	R2	DT/SD voltage	
DT1	~15ns	<10kΩ	open	1.0 x V_{CC}	
DT2	~25ns	3.3kΩ	8.2kΩ	0.71 x V_{CC}	Default
DT3	~35ns	5.6kΩ	4.7kΩ	0.46 x V_{CC}	
DT4	~45ns	8.2kΩ	3.3kΩ	0.29 x V_{CC}	

2) In Shutdown mode, both MOSFETs are turned off simultaneously to stop operation and protect the circuit during fault conditions. If the DT/SD pin detects an input voltage below the threshold, 0.23 x V_{CC}, the IRS20124S will output 0V at both HO and LO outputs, forcing the switching output node to go into a high impedance state.

Protection

The IRAUDAMP3 includes protection features for over-voltage (OVP), under-voltage (UVP), over-current (OCP), DC-voltage (DCP) and over-temperature protection (OTP). The OVP, DCP, OCP and OTP uses OR logic and will shutdown the output power amplifier (MOSFETs) if any one or more protection feature is activated (by pulling the DT/SD pin low). Once a fault condition is detected and the power amplifier is shutdown, the shutdown pin will remain low (latched) for about three seconds. If a fault is not cleared, or re-occurs after the restart of the power amplifier, the DT/SD pin will again latch. Thus this circuit will hiccup until the fault is removed.

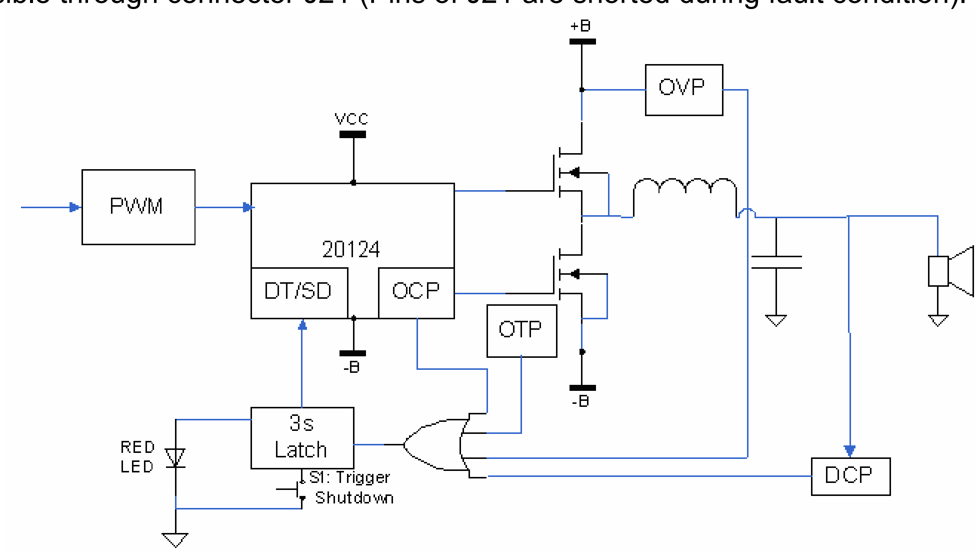
The under-voltage protection (UVP) is separate from the above protection circuit and operates by turning off the V_{CC} into to the IRS20124S once the input voltage drops too low. When V_{CC} starts dropping to zero, the UVLO protection within the IRS20124S will shutdown the power amplifier.

Resetting the Protection Circuit

The IRAUDAMP3 has a number of protection circuits to safeguard the system and speakers during operation. If any fault condition is detected, the Shutdown circuit will latch for about three seconds, during which time the orange LED will turn on. If the fault condition has not cleared, the protection circuit will hiccup until fault is removed. There is no manual reset option.

DC Voltage Protection (DCP)

DC voltage output protection is provided to protect the speakers from DC current. This abnormal condition is rare and is likely caused when the power amplifier fails and one of the high-side or low-side IRF6645 MOSFETs remain in the ON state. DC protection is activated if the output has more than ±4VDC offset (typical). Under this fault condition, the feeding power supplies must be shutdown. Since these are external to the reference design board, an isolated relay is provided (P1) for further systematic evaluation of DC voltage protection to transmit this condition to the power supply controller and is accessible through connector J21 (Pins of J21 are shorted during fault condition).



Functional block diagram of protection circuit implementation

Over-Voltage Protection (OVP)

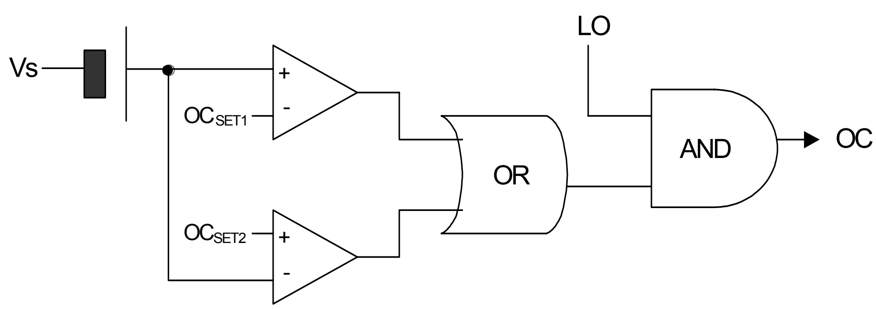
Over-voltage protection will shutdown the amplifier if the bus voltage between GND and +B exceeds 40V. The threshold is determined by the sum of the Zener diode voltage of Z11 and the V_{BE} of Q11. As a result, it protects the board from bus-pumping at very low audio signal frequencies by shutting down the amplifier. OVP will automatically reset after three seconds. The isolated relay is also activated during this fault condition.
Since the +B and –B supplies are normally symmetrical, (bus pumping, although asymmetrical in time, will pump the bus symmetrically in voltage level.) it is considered sufficient to only sense one of the two supply voltages for OVP.

Over-Current Protection (OCP)

The internal over-current protection shuts down the IRS20124S if a trip threshold-level of the bi-directional current-sensing circuit is exceeded. When this fault occurs, the OC-pin is pulled low for at least 100ns. To keep the IRS20124S from re-starting, the OC-pin output is fed back to the DT/SD pin, using the three second latch.

Bi-directional Over-Current Sensing

The bi-directional current sensing block has an internal 2.21V level shifter feeding the signal to a comparator. The OCSET1 pin sets the positive current threshold, and is given a trip level at VSOC+, which is OCSET1 - 2.21V. In the same way, the OCSET2 pin, VSOC- is set at OCSET2 – 2.21V.



Simplified functional block diagram of bi-directional current sensing

How to Set OC-Threshold

The external resistors R3, R4, and R5 are used as voltage dividers to set OCSET1 and OCSET2. The trip threshold voltages, VSOC+ and VSOC-, are determined by the required trip current levels, ITRIP+ and ITRIP-, and the device on-resistance, $R_{DS(on)}$, in the low-side MOSFET. Please note that since the on-resistance of the low-side MOSFET is temperature dependent, the actual over-current trip level will decrease as the MOSFET heats up.

Since the sensed voltage of Vs is shifted up by 2.21V internally and compared with the voltages fed to the OCSET1 and OCSET2 pins, the required value of OCSET1 with respect to COM is:

$$VOCSET1 = VSOC+ + 2.21 = ITRIP+ \times R_{DS(ON)} + 2.21$$

The same relation holds between OCSET2 and VSOC-:

$$VOCSET2 = VSOC- + 2.21 = ITRIP- \times R_{DS(ON)} + 2.21$$

On the reference design, the values of R3, R4 and R5 have been set to 10.0kΩ, 1.30kΩ and 1.74kΩ respectively. These values result in VSOC+ and VSOC- limits of ±0.60V and for an $R_{DS(ON)}$ of 28mΩ (from datasheet of IRF6645), a over-current trip level of approximately 21A is achieved.

Please refer to the IRS20124S data sheet for a complete description and method for choosing R3, R4 and R5.

Due to the duty cycle limitation in bi-directional current sensing in the IRS20124, the OCP will work up to 100W. For short-circuit protection beyond this, a number of alternative solutions can be implemented. These include using either external current-sensing or alternative gate driver IC having current-sensing function that measure both HS and LS MOSFET currents independently, such as the IRS20954.

Over-Temperature Protection (OTP)

A separate PTC resistor is placed in close proximity to the IRF6645 DirectFET MOSFETs on each daughter board for each of the amplifier channels. If the resistor temperature rises above 100°C, the OTP is activated. This temperature protection limit yields a PCB temperature at the MOSFETs of about 100°C. This temperature protection limit is due to the use of FR4 as a substrate material.

Under-Voltage Protection (UVP)

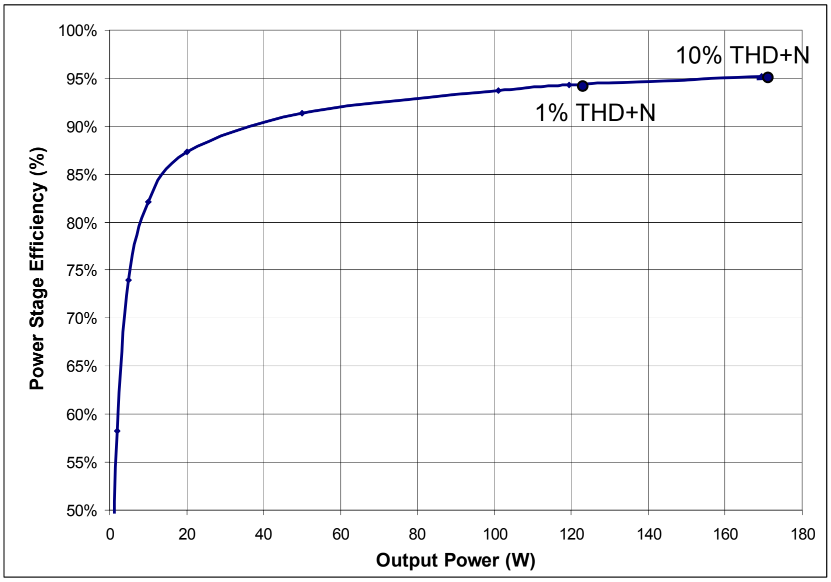
Under-voltage protection will shutdown the amplifier if the bus voltage between GND and +B falls below 20V by cutting of the V_{CC} supply to the IRS20124S IC. If the supply to the IC drops below 9V (typical), the UVLO within the IC will shutdown the power amplifier.

Bridged Output

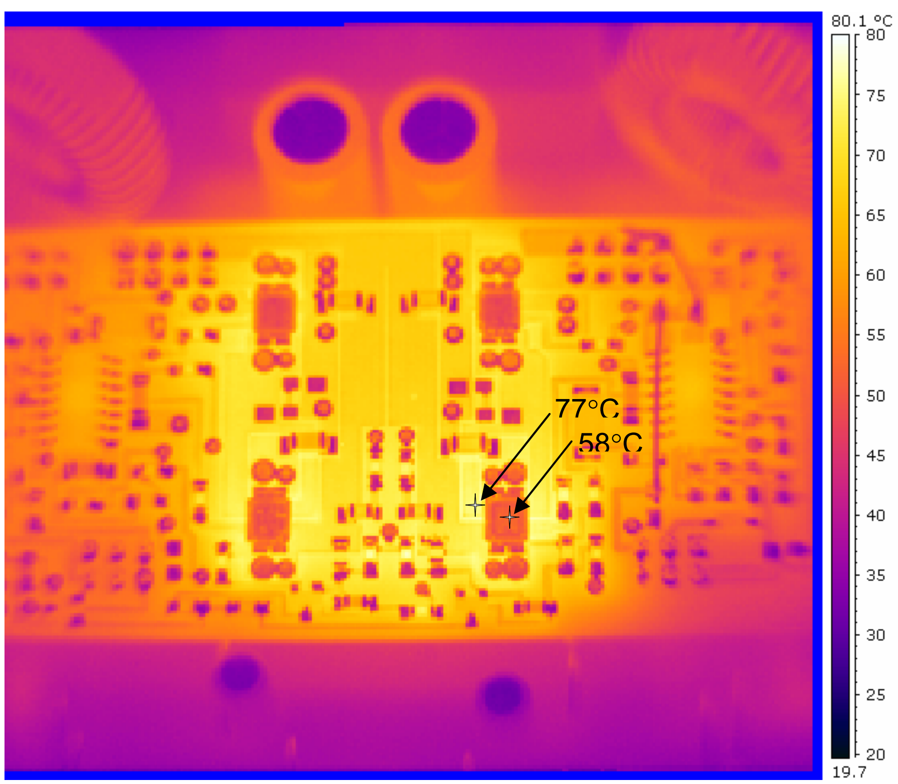
The IRAUDAMP3 is not intended for BTL operation. However, the BTL operation can be achieved by connecting the speaker load between the '+' terminals of two adjacent channels and feeding the same input signal to both channels (with one input signal inverted). In BTL operation, minimum load impedance is 8Ω, rated power is 240W, non-clipping.

Thermal Considerations

From the nature of typical music signals, while the instantaneous power can reach >120W, the average power is limited to 1/8th of rated power. This is generally considered to be the normal operating condition in safety standards and the IRAUDAMP3 requires no heatsinking under normal operation. For higher average power conditions, however, additional cooling would be required.



Efficiency vs. output power, 4Ω single channel driven, $T_{ambient}$ = 25°C

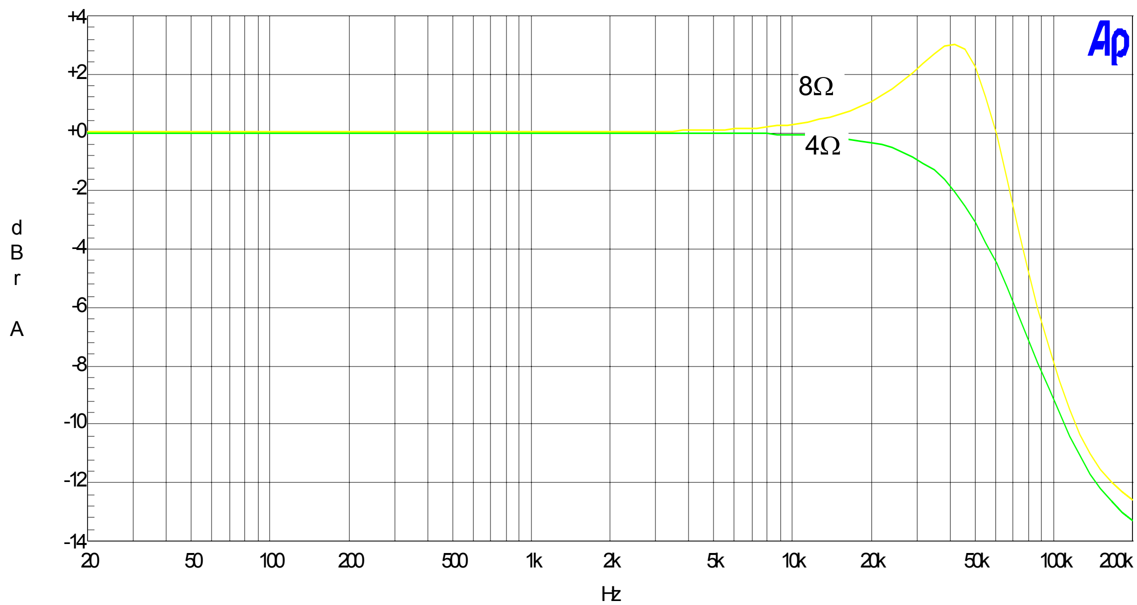


Thermal image of daughter board running at 2ch x 1/8th rated power - steady state, T_C < 58°C

Typical Performance

±B supply = ±35V, load impedance = 4Ω, 1kHz audio signal,
Self Oscillator @ 400kHz and internal volume control set to give required output with 1Vrms input signal, unless otherwise noted.

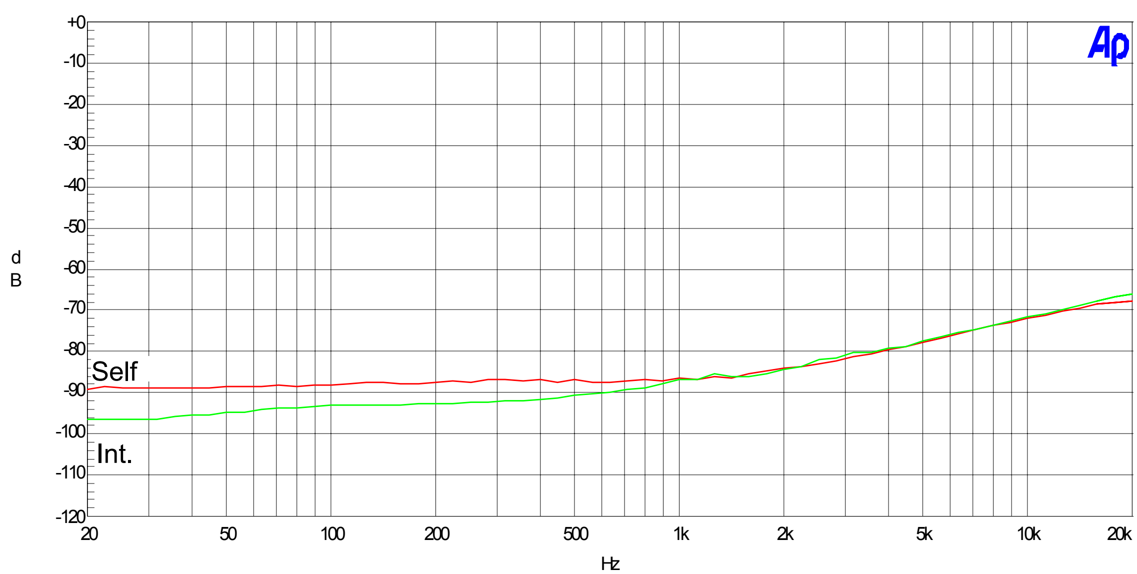
International Rectifier A-A THD+N vs FREQUENCY 11/21/05 19:23:40



Green	CH1 - 4Ω, 2V Output
Yellow	CH1 - 8Ω, 2V Output

Frequency characteristics vs. load impedance

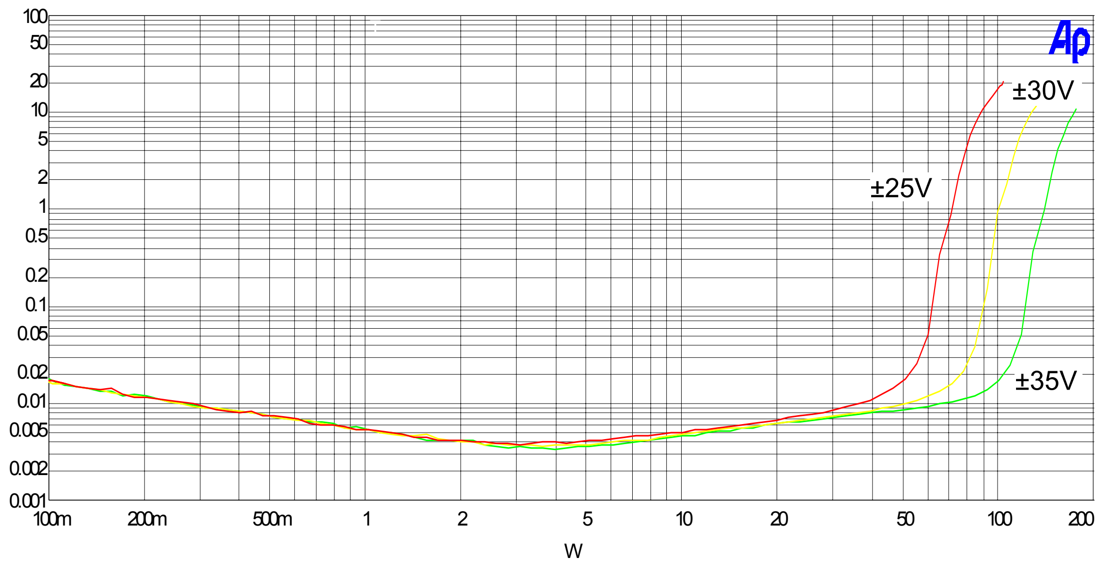
International Rectifier A-A FREQUENCY RESPONSE 12/19/05 09:27:51



Red	CH2 – CH1, 60W, Self Oscillator @ 400kHz
Green	CH2 – CH1, 60W, Internal Clock @ 395kHz

Channel separation vs. frequency

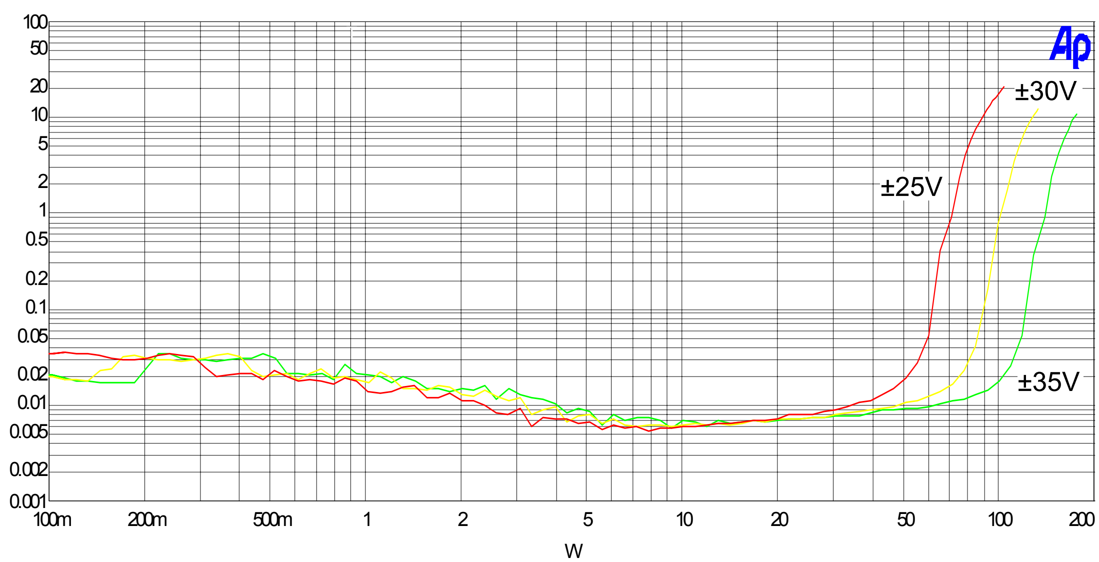
International Rectifier A-A THD+N vs POWER 11/21/05 18:55:20



Green	CH1, ±B = ±35V, Volume gain 21.9V/V
Yellow	CH1, ±B = ±30V, Volume gain 21.9V/V
Red	CH1, ±B = ±25V, Volume gain 21.9V/V

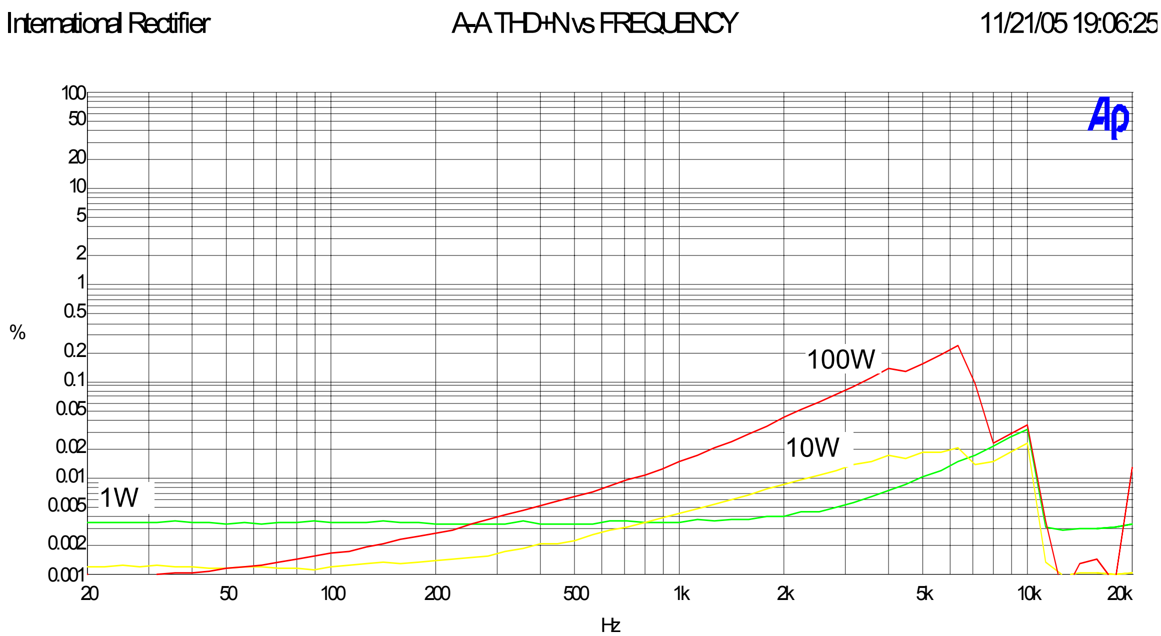
THD+N ratio vs. output power

International Rectifier A-A THD+N vs POWER 11/21/05 18:37:01



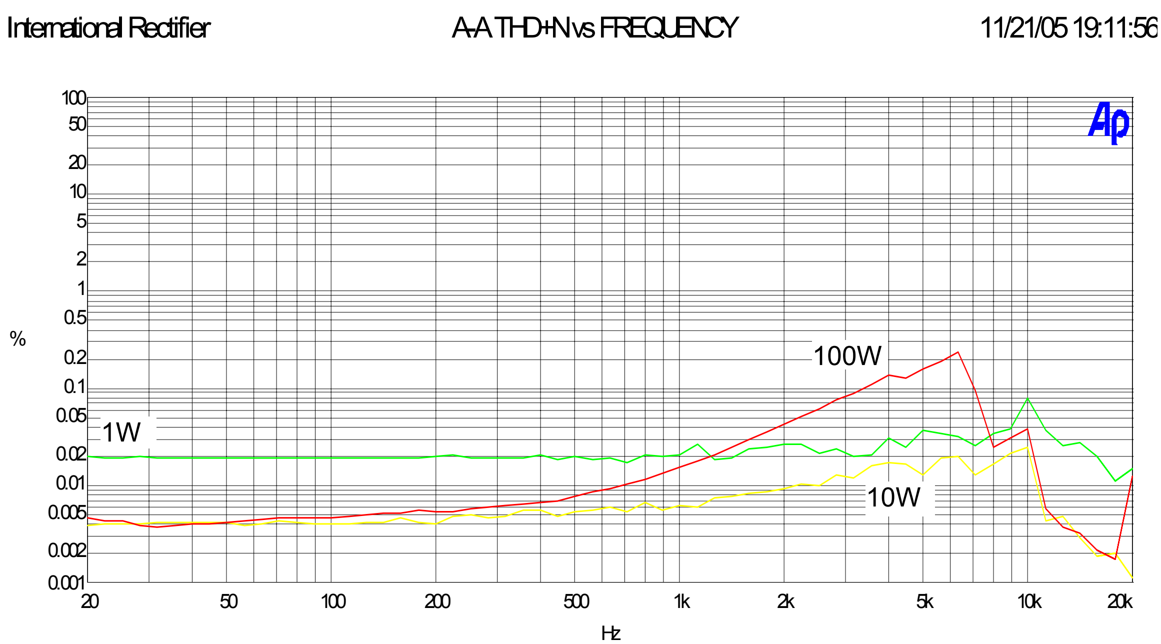
Green	CH1 - ACD, ±B = ±35V, Volume gain 21.9V/V
Yellow	CH1 - ACD, ±B = ±30V, Volume gain 21.9V/V
Red	CH1 - ACD, ±B = ±25V, Volume gain 21.9V/V

THD+N ratio vs. output power (ACD)



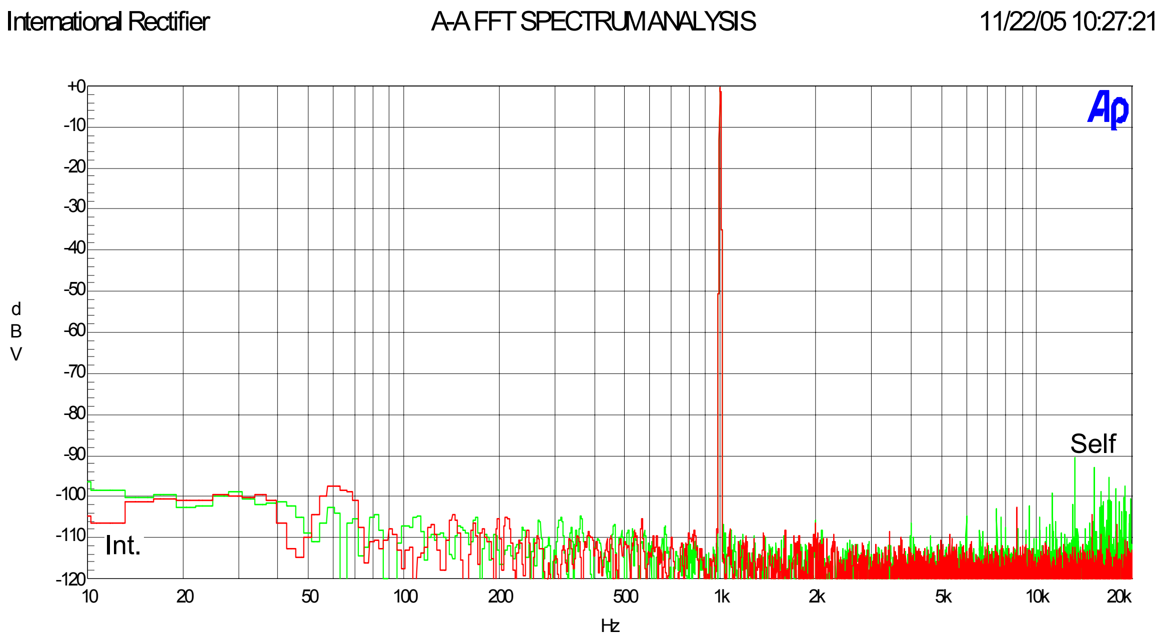
Green	CH1, 1W Output
Yellow	CH1, 10W Output
Red	CH1, 100W Output

THD+N ratio vs. frequency



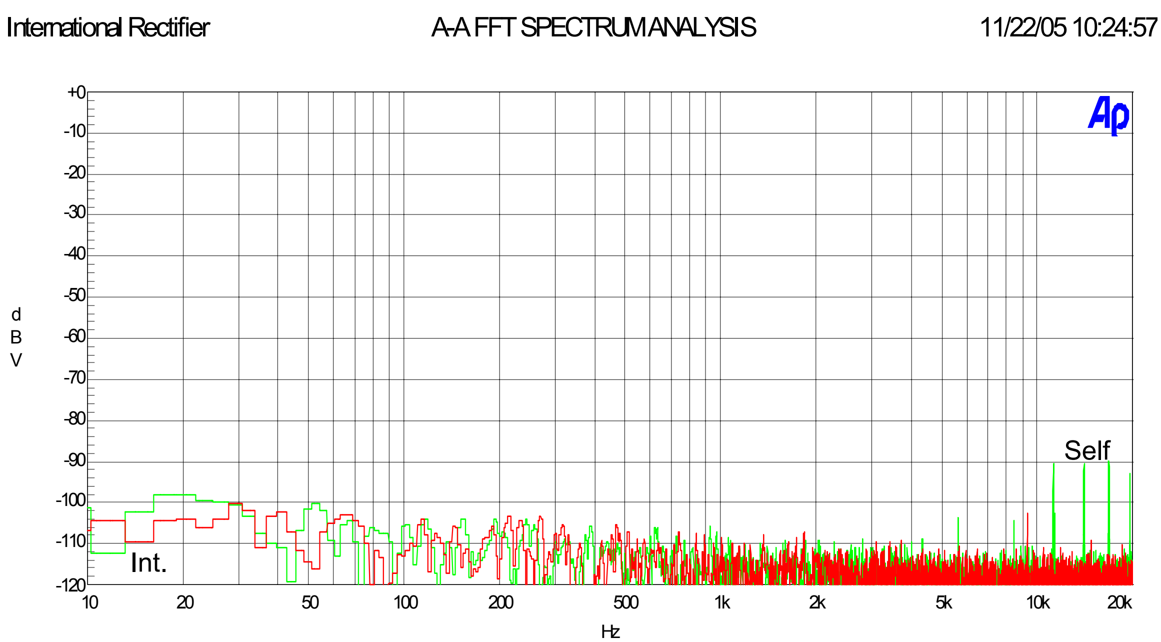
Green	CH1 - ACD, 1W Output
Yellow	CH1 - ACD, 10W Output
Red	CH1 - ACD, 100W Output

THD+N ratio vs. frequency (ACD)



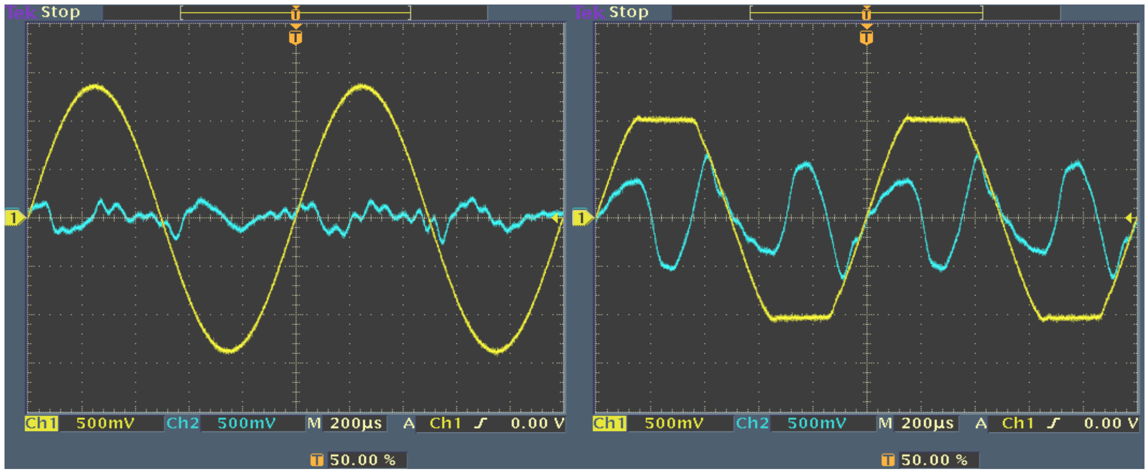
Green	CH1 - ACD, 1V, 1kHz, Self Oscillator @ 400kHz
Red	CH1 - ACD, 1V, 1kHz, Internal Clock @ 395kHz

Frequency spectrum (ACD)



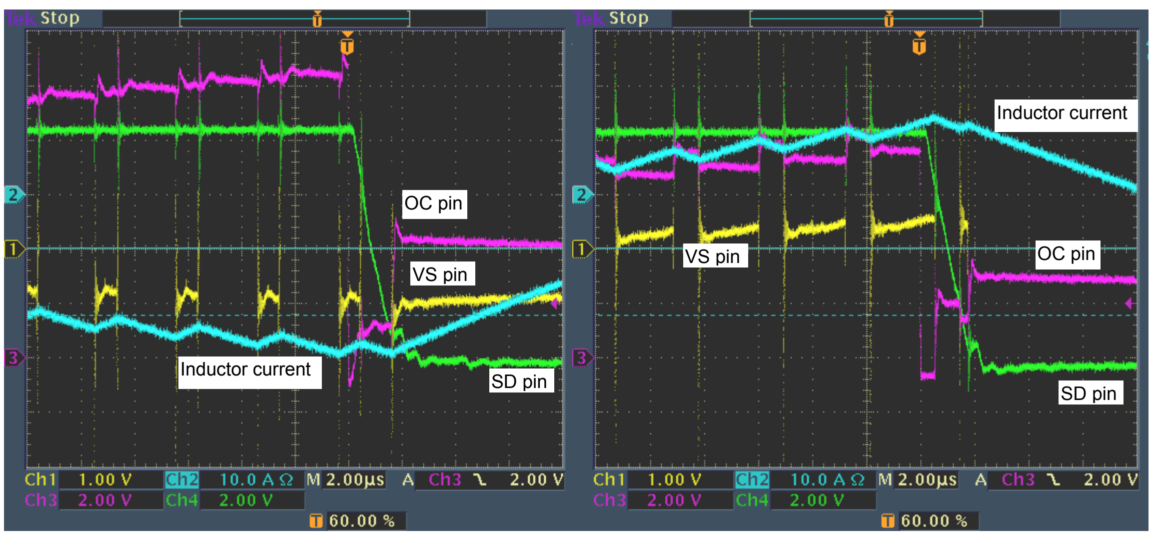
Green	CH1 - ACD, No signal, Self Oscillator @ 400kHz
Red	CH1 - ACD, No signal, Internal Clock @ 395kHz

Residual noise (ACD)



60W / 4Ω, 1kHz, THD+N=0.009% *174W / 4Ω, 1kHz, THD+N=10%*

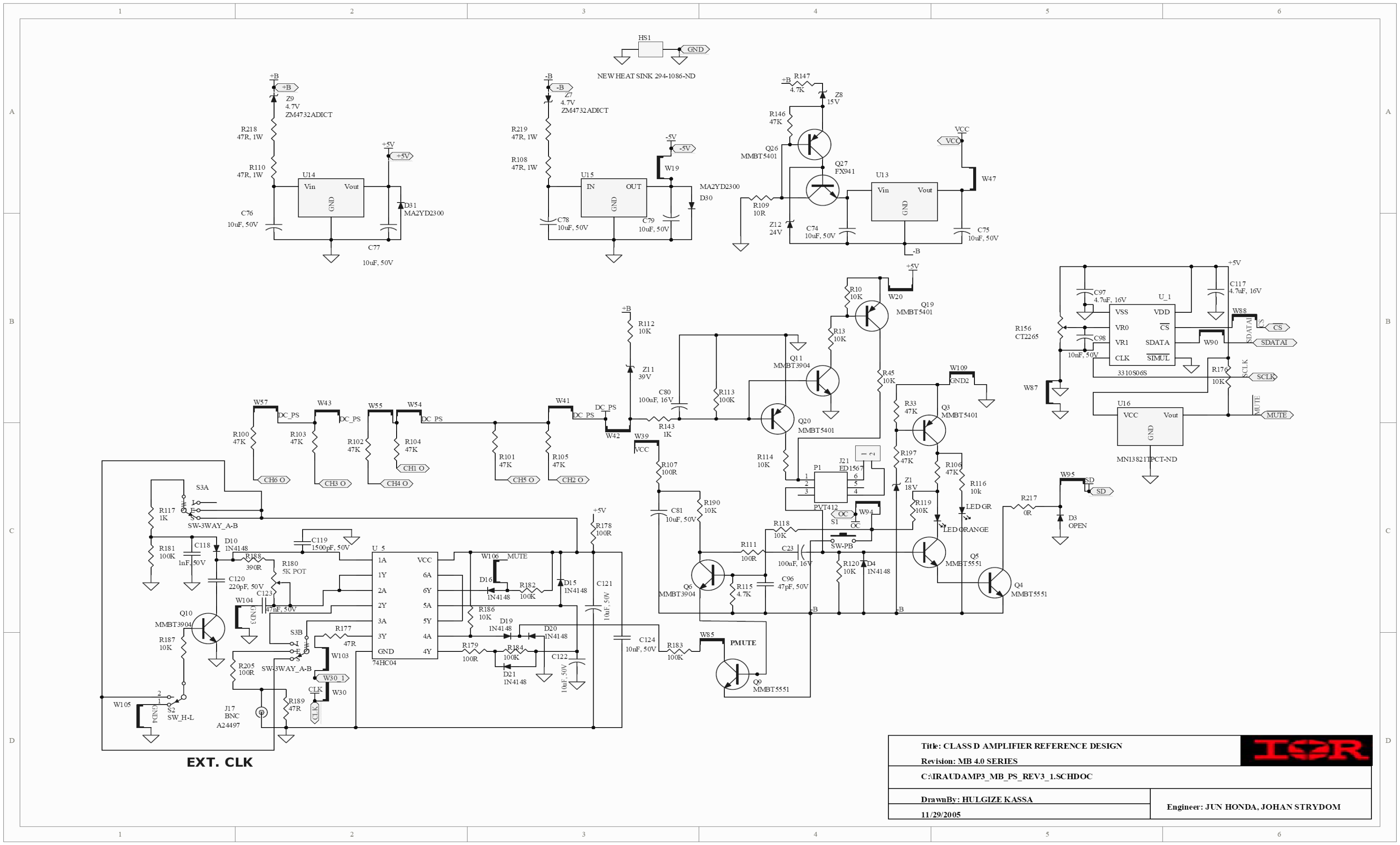
Measured output and distortion waveforms



Typical OCP waveforms showing OC output and SD input

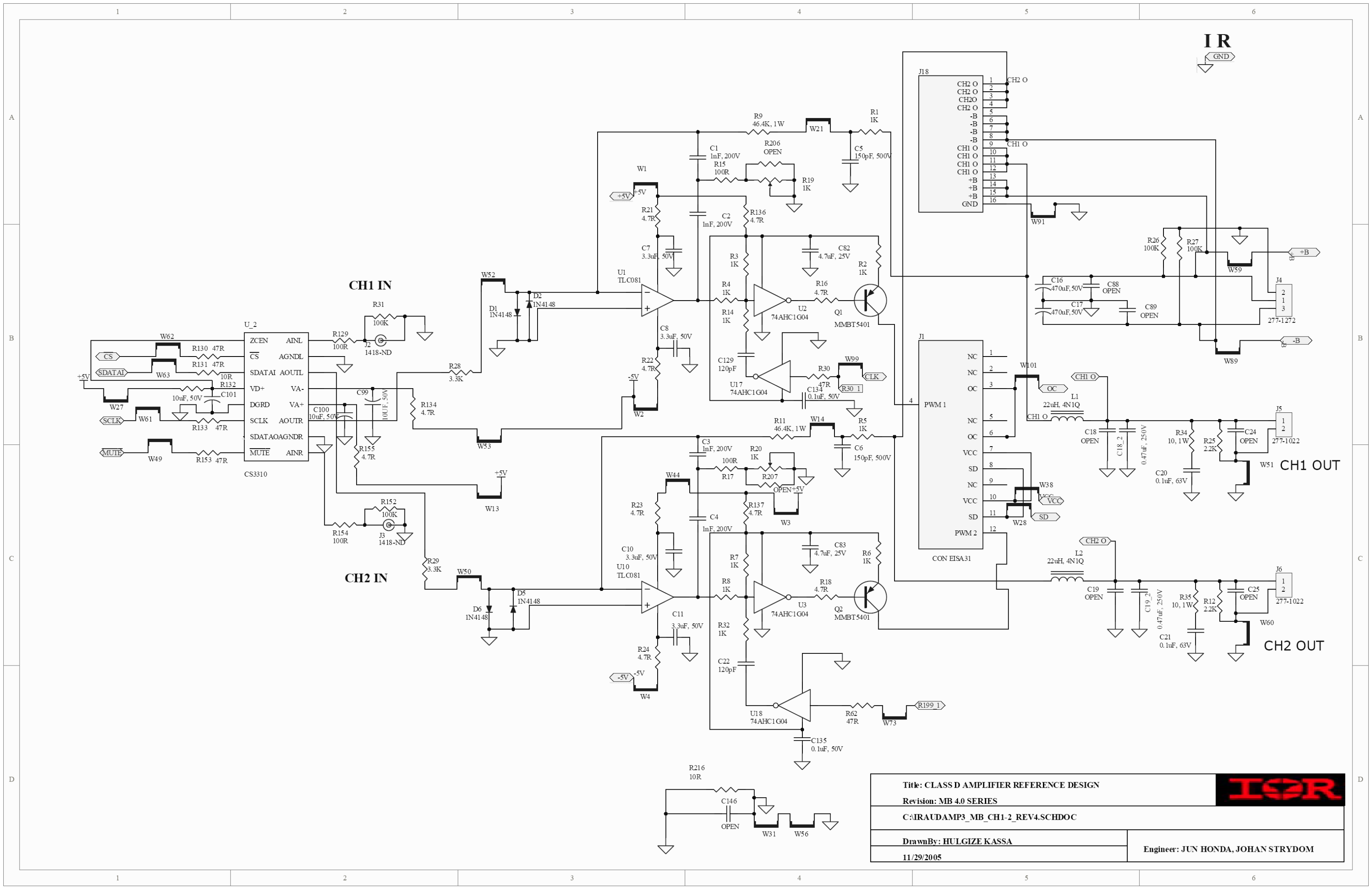
IRAUDAMP3 Design Documents

Motherboard Schematics:

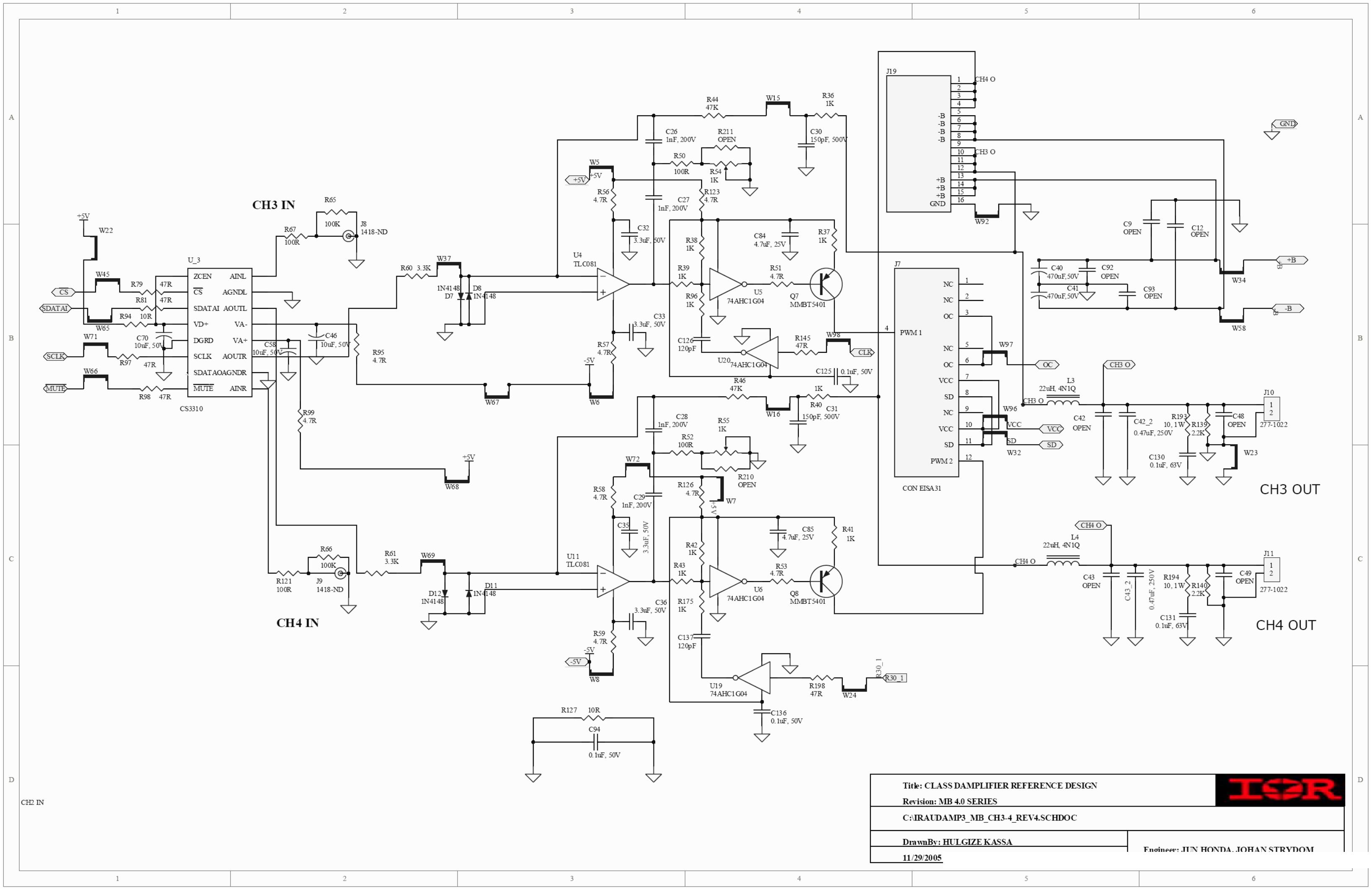


Housekeeping and protection circuits

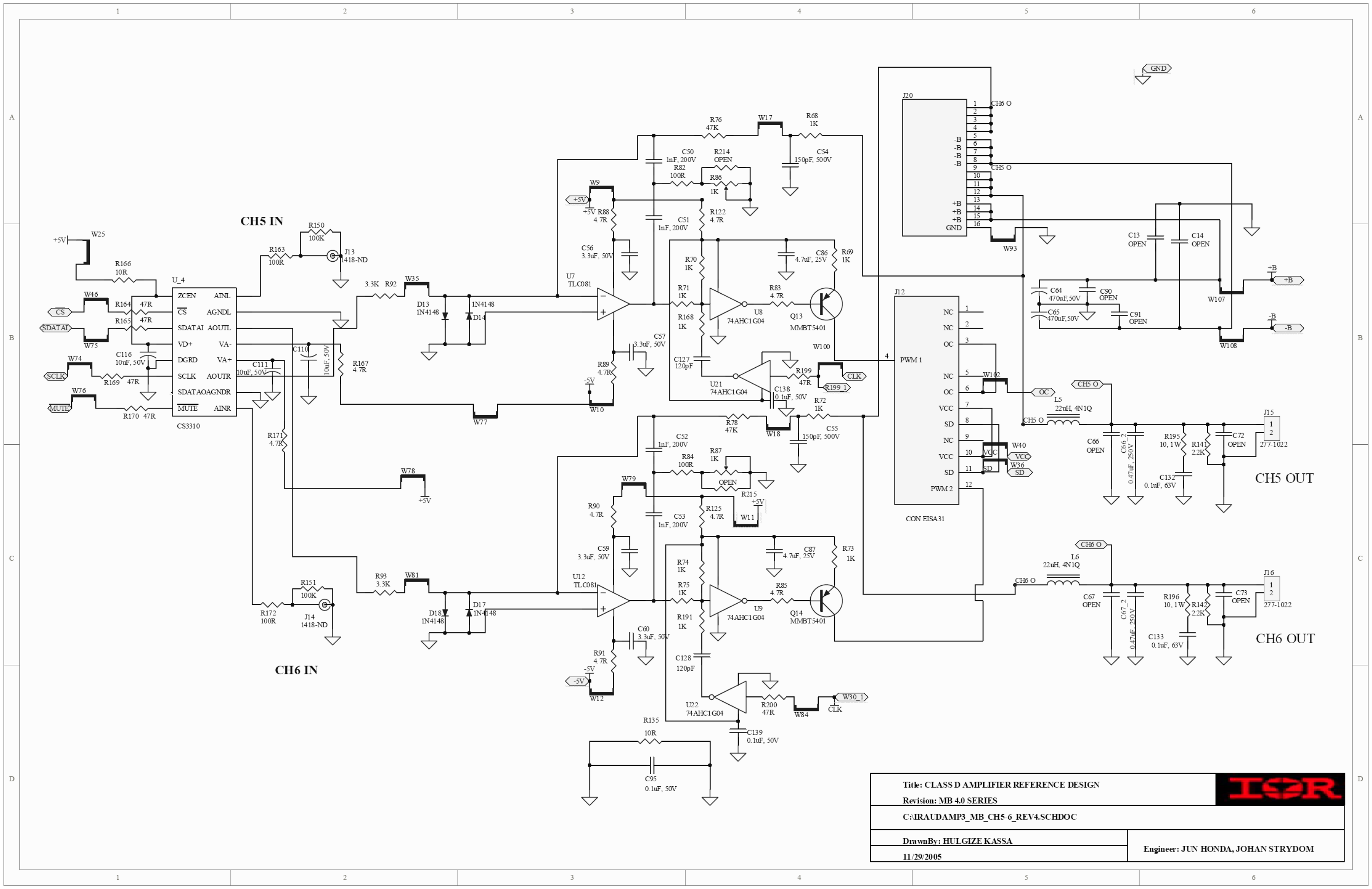
REFERENCE DESIGN



Audio channels 1 and 2



Audio channels 3 and 4

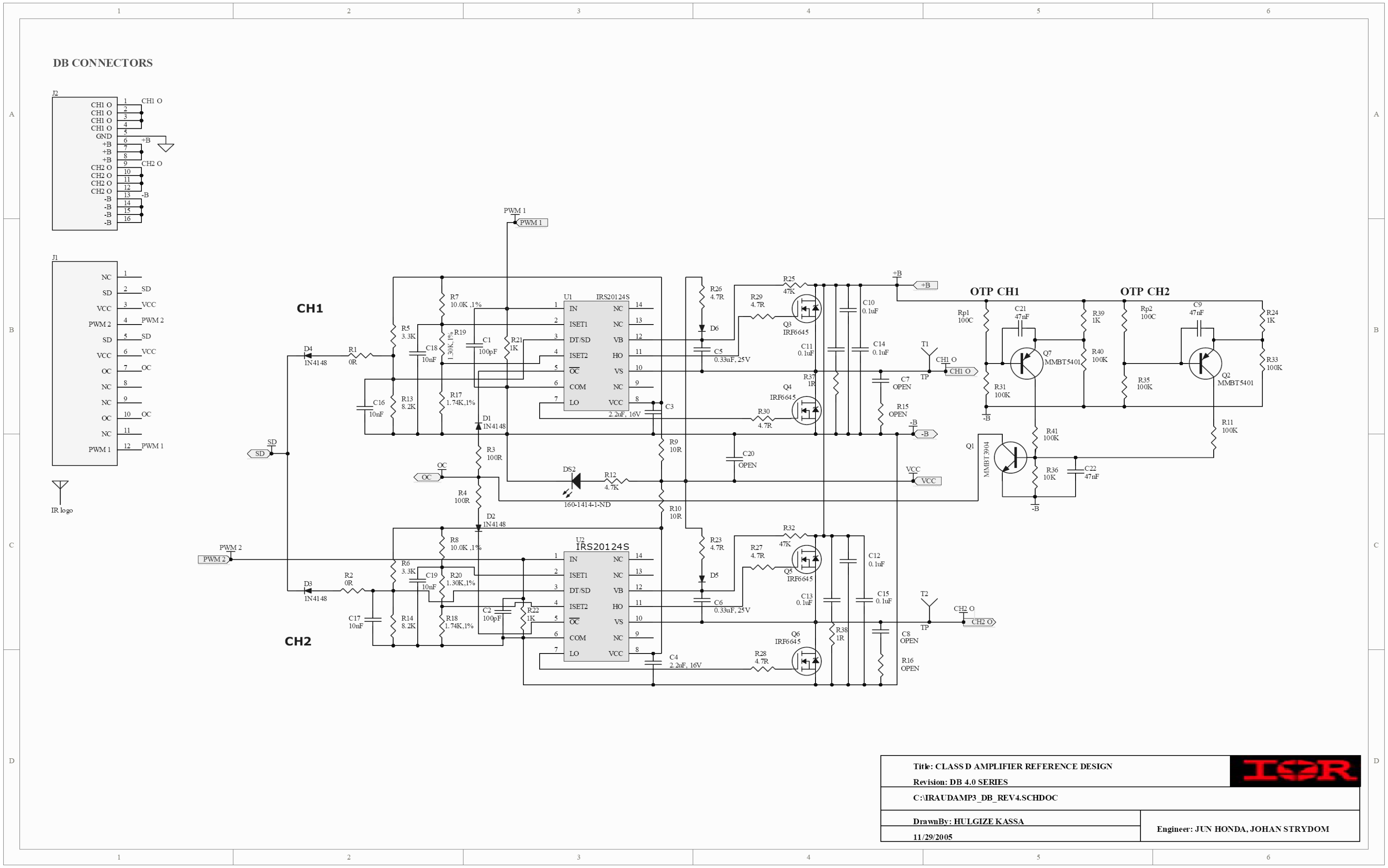


Audio channels 5 and 6

International IOR Rectifier

REFERENCE DESIGN

Daughter Board Schematics:



Daughter-board schematic with Class D stage for 2 audio channels

IRAUDAMP3 Bill of Materials

Motherboard:

IRAUDAMP3 MOTHERBOARD BILL OF MATERIAL						
NO	Designator	#	Footprint	PartType	Part No	Vender
1	C1, C2, C3, C4	4	1206	1nF, 200V	PCC2009CT-ND	Digikey
2	C5, C6, C30, C31, C54, C55	6	AXIAL0.19R	150pF, 500V	338-1052-ND	Digikey
3	C7, C8, C10, C11, C32, C33, C35, C36, C56, C57, C59, C60	12	CR3225-1210	3.3uF, 50V	445-1432-1-ND	Digikey
4	C9, C12, C13, C14, C24, C25, C48, C49, C72, C73, C146	11	0805	OPEN	OPEN	
5	C16, C17, C40, C41, C64, C65	6	RB5/10	470uF,50V	01E9650	Newark
6	C18, C19, C42, C43, C66, C67	6	AXIAL0.2R	CAP	OPEN	
7	C18_2, C19_2, C42_2, C43_2, C66_2, C67_2	6	CAP MKP	0.47uF, 250V	495-1298-ND	Digikey
8	C20, C21, C130, C131, C132, C133	6	AXIAL0.3R	0.1uF, 63V	BC2054-ND	Digikey
9	C22, C126, C127, C128, C129, C137	6	0805	120pF, 50V	PCC121CGCT-ND	Digikey
10	C23, C80	2	RB2/5-16V	100uF, 16V	493-1283-ND	Digikey
11	C26, C27, C28, C29, C50, C51, C52, C53	8	0805	1nF, 200V	PCC1997CT-ND	Digikey
12	C46, C58, C70, C74, ,C75, C76, C77, C78, C79, C81, C99, C100, C101, C110, C111, C116, C121, C122	18	RB2/5	10uF, 50V	03B2235	Newark
13	C82, C83, C84, C85, C86, C87	6	CR3225-1210	4.7uF, 25V	PCC2251CT-ND	Digikey
14	C88, C89, C90, C91, C92, C93	6	AXIAL0.1R	CAP	OPEN	
15	C94, C95	2	0805	0.1uF, 50V	PCC1840CT-ND	Digikey
16	C96	1	0805	47pF, 50V	PCC470CGCT-ND	Digikey
17	C97, C117	2	0805	4.7uF, 16V	PCC2323CT-ND	Digikey
18	C98, C124	2	0805	10nF, 50V	PCC103BNCT-ND	Digikey
19	C118	1	0805	1nF, 50V	PCC102CGCT-ND	Digikey
20	C119	1	0805	1500pF, 50V	PCC2004CT-ND	Digikey
21	C120	1	0805	220pF, 50V	PCC1953CT-ND	Digikey
22	C123	1	1206	47nF, 50V	311-1178-1-ND	Digikey
23	C125, C134, C135, C136, C138, C139	6	1206	0.1uF, 50V	PCC104BCT-ND	Digikey
24	D1, D2, D4, D5, D6, D7, D8, D10, D11, D12, D13, D14, D15, D16, D17,D18, D19, D20, D21	19	SOD-123	1N4148	1N4148WDICT-ND	Digikey
25	D3	1	SOD-123	OPEN		
26	D30, D31	2	SOD-123	MA2YD2300LCT	MA2YD2300LCT-ND	Digikey
27	HS1	1	Heat_S6in1	HEAT SINK	294-1086-ND	Digikey
28	J1, J7, J12	6	CON EISA31	CON EISA31	A26453-ND	Digikey
29	J2, J3, J8, J9, J13, J14	6	CP1418	1418-ND	CP-1418-ND	Digikey
30	J4	1	J HEADER3	277-1272	277-1272-ND	Digikey
31	J5, J6, J10, J11, J15, J16	6	MKDS5/2-9.5	277-1022	277-1271-ND	Digikey
32	J17	1	BNC-RA-CON	BNC	A24497-ND	Digikey
33	J18, J19, J20	6	CON_POWER	CON_POWER	A26454-ND	Digikey
34	J21	1	ED1567	ED1567	ED1567	Digikey
35	L1, L2, L3, L4, L5, L6	6	INDUCTOR	18uH	Custom made	
36	LED GR	1	Led rb2/5	404-1109	404-1109-ND	Digikey
37	LED ORANGE	1	Led rb2/5	404-1107	404-1107-ND	Digikey
38	P1	1	DIP-6	PVT412	PVT412-ND	Digikey
39	Q1, Q2, Q3, Q7, Q8, Q13, Q14, Q19, Q20, Q26	10	SOT23-BCE	MMBT5401	MMBT5401DICT-ND	Digikey
40	Q4, Q5, Q9	3	SOT23-BCE	MMBT5551	MMBT5551DICT-ND	Digikey
41	Q6, Q10, Q11	3	SOT23-BCE	MMBT3904	MMBT3904DICT-ND	Digikey
42	Q27	1	SOT89	FX941	FCX491TR-ND	Digikey
43	R1, R5, R36, R40, R68, R72, R117	7	1206	1K	P1.0KECT-ND	Digikey
44	R2, R3, R4, R6, R7, R8, R14, R32, R37, R38, R39, R41, R42, R43, R69, R70, R71, R73, R74, R75, R96, R143, R168, R175, R191	25	0805	1K	P1.0KACT-ND	Digikey
45	R9, R11	2	CR5025-2010	46.4K, 1W	01H0485	Newark
46	R10, R13, R45, R112, R114, R118, R119, R120, R176, R186, R187, R190	12	0805	10K	P10KACT-ND	Digikey
47	R12, R25, R139, R140, R141, R142	6	1206	2.2K	P2.2KECT-ND	Digikey
48	R15, R17, R50, R52, R67, R82, R84, R107, R111, R121, R129, R154, R163, R172, R179, R205	16	0805	100R	P100ACT-ND	Digikey
49	R16, R18, R21, R22, R23, R24, R51, R53, R56, R57, R58, R59, R83, R85, R88, R89, R90, R91, R122, R123, R125, R126, R136, R137	24	0805	4.7R	P4.7ACT-ND	Digikey
50	R19, R20, R54, R55, R86, R87	6	POT_SRM	1K	3361P-102GCT-ND	Digikey

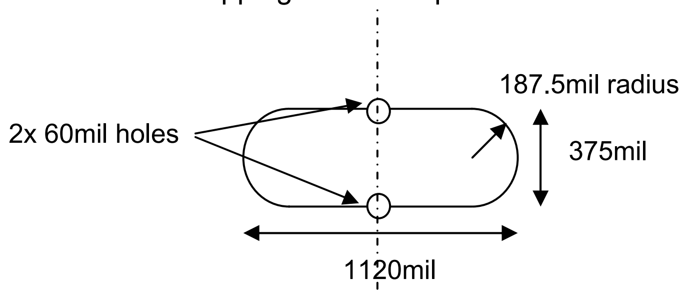
51	R26, R27, R31, R65, R66, R113, R150, R151, R152, R181, R182, R183, R184	13	0805	100K	P100KACT-ND	Digikey
52	R28, R29, R60, R61, R92, R93	6	1206	3.3K	P3.3KECT-ND	Digikey
53	R30, R62, R79, R81, R97, R98, R130, R131, R133, R145, R153, R164, R165, R169, R170, R177, R189, R198, R199, R200	20	0805	47R	P47ACT-ND	Digikey
54	R33, R44, R46, R76, R78, R100, R101, R102, R103, R104, R105, R146, R197	13	0805	47K	P47KACT-ND	Digikey
55	R34, R35, R193, R194, R195, R196	6	2512	10, 1W	PT10XCT	Digikey
56	R94, R109, R127, R132, R135, R166, R216	7	0805	10R	P10ACT-ND	Digikey
57	R95, R99, R134, R155, R167, R171	6	1206	4.7R	P4.7ECT-ND	Digikey
58	R106	1	1206	47K	P47KECT-ND	Digikey
59	R108, R110, R218, R219	4	2512	47R, 1W	PT47XCT-ND	Digikey
60	R115, R147	2	0805	4.7K	P4.7KACT-ND	Digikey
61	R116	1	1206	10K	P10KECT-ND	Digikey
62	R156	1	V_CONTROL	CT2265-ND	CT2265-ND	Digikey
63	R178	1	1206	100R	P100ECT-ND	Digikey
64	R180	1	POT	5K POT	3362H-502-ND	Digikey
65	R188	1	0805	390R	P390ACT-ND	Digikey
66	R206, R207, R210, R211, R214, R215	6	0805	OPEN	OPEN	
67	R217	1	1206	0R	P0.0ECT-ND	Digikey
68	S1	1	SWITCH	SW-PB	P8010S-ND	Digikey
69	S2	1	SW-EG1908	SW_H-L	EG1908-ND	Digikey
70	S3	1	SW-EG1944	SW-3WAY_AB	EG1944-ND	Digikey
71	TP	1	OPEN	OPEN	OPEN	
72	U1, U4, U7, U10, U11, U12	6	SO-8	TLC081	299-7264-1-ND	Digikey
73	U2, U3, U5, U6, U8, U9, U17, U18, U19, U20, U21, U22	12	SOT25	74AHC1G04	296-1089-1-ND	Digikey
74	U13	1	TO-220 FULLPAK	MC78M12	MC78M12CTOS-ND	Digikey
75	U14	1	TO-220 FULLPAK	MC78M05	MC78M05CTOS-ND	Digikey
76	U15	1	TO-220 F	MC79M05	MC79M05CTOS-ND	Digikey
77	U16	1	SOT23-123	MN13821TP	MN13821TPCT-ND	Digikey
78	U_1	1	N8A	3310IR01	3310IR01	Japan*
79	U_2, U_3, U_4	3	SOIC16	CS3310	73C8016	Newark
80	U_5	1	M14A	74HC04	296-1189-1-ND	Digikey
81	W43, W51, W52, W53, W67, W68, W77, W78, W96, W97, W101, W102, W104	27	J1-750	Jumper	ZO-1/8W-T	Digikey
82	W2, W3, W4, W6, W7, W8, W10, W11, W12, W30, W54, W57, W91, W92, W93, W98, W99, W100, W106, W109	20	J1-975	Jumper	ZO-1/8W-T	Digikey
83	W41	1	J1-720	Jumper	ZO-1/8W-T	Digikey
84	W14, W23, W34, W39, W40, W42, W59, W103, W107	9	J1-570	Jumper	ZO-1/8W-T	Digikey
85	W16, W18, W36, W50, W56, W60, W69, W81, W105	9	J1-650	Jumper	ZO-1/8W-T	Digikey
86	W45, W46, W62, W72	4	J1-350	Jumper	ZO-1/8W-T	Digikey
87	W22, W25, W27, W55, W85, W90, W95	7	J1-200	Jumper	ZO-1/8W-T	Digikey
88	W24, W47, W49, W63, W65, W66, W73, W75, W76, W84	10	J1-300	Jumper	ZO-1/8W-T	Digikey
89	W44, W61, W71, W74, W94, W108	6	J1-430	Jumper	ZO-1/8W-T	Digikey
90	W20, W58, W79, W87, W88, W89	6	J1-500	Jumper	ZO-1/8W-T	Digikey
91	Z1	1	SOD-123	18V	BZT52C18-FDICT-ND	Digikey
92	Z7, Z9	2	DL-41	4.7V	ZM4732ADICT-ND	Digikey
93	Z8	1	SOD-123	15V	BZT52C15-FDICT-ND	Digikey
94	Z11	1	SOD-123	39V	BZT52C39-13-FDITR-ND	Digikey
95	Z12	1	SOD-123	24V	BZT52C24-FDICT-ND	Digikey
96	Volume control knob	1			MCCPMB1	Newark
97	Thermalloy with screw	3			46F4081	Newark
98	Standoffs	5			2210K-ND	Digikey
99	screw	5			H354-ND	Digikey
100	Washer Lock	5			H244-ND	Digikey

*Tachyonix Corporation,
14 Gonaka Jimokuji Jimokuji-cho,
Ama-gun Aichi, JAPAN 490-1111

http://www.tachyonix.co.jp
info@tachyonix.co.jp

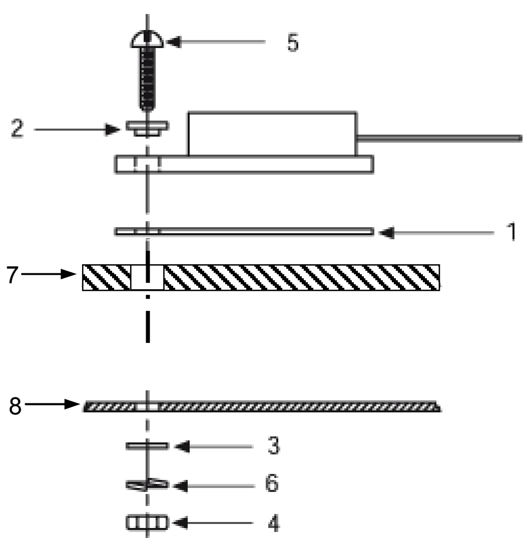
Output Inductor Specification:

Core:	T94-2 from Micrometals
Wire:	22 AWG
# Turns:	48
Nominal Inductance:	18uH
Finish:	No varnish or dipping of core required



Suggested PCB footprint for custom output inductor

Voltage Regulator Mounting:



Item	Description
1	Insulator Thermalfilm
2	Shoulder Washer
3	Flat Washer #4
4	No. 4-40 UNC-2B Hex Nut
5	No. 4-40 UNC-2A X 1/2 Long Phillips Pan Head Screw
6	Lockwasher, No.4
7	Heatsink
8	PCB

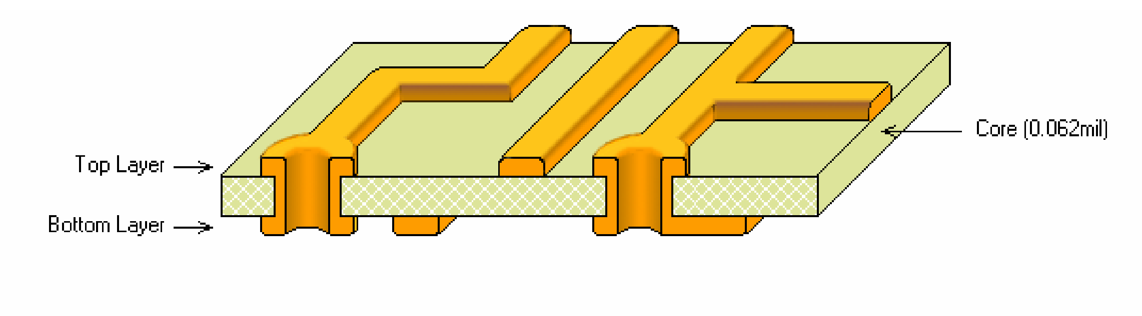
Daughter Board:

IRAUDAMP3 DAUTHER-BOARD BILL OF MATERIAL						
NO	Designator	#	Footprint	Part Type	Part No	Vendor
1	C1, C2	2	0805	100pF	PCC101CGCT-ND	Digikey
2	C3, C4	2	1206	2.2uF, 16V	PCC1898CT-ND	Digikey
3	C5, C6	2	1206	0.33uF, 25V	PCC1889CT-ND	Digikey
4	C7, C8, C20, R15, R16	5	0805	OPEN	OPEN	
5	C16, C17, C18, C19	5	0805	10nF	PCC103BNCT-ND	Digikey
6	C9, C21, C22	3	0805	47nF	PCC1836CT-ND	Digikey
7	C10, C12, C14, C15	4	1206	0.1uF	PCC2239CT-ND	Digikey
8	C11, C13	2	0805	0.1uF	PCC1840CT-ND	Digikey
9	D1, D2, D3, D4	4	SOD-123	1N4148	1N4148WDICT-ND	Digikey
10	D5, D6	2	SMB	MURA120T30SCT	MURA120T3OSCT-ND	Digikey
11	DS2	1	LED	160-1414-1	160-1414-1-ND	Digikey
12	J1	2	CON EISA31	CON EISA31	A26568-ND	Digikey
13	J2	2	CON_POWER	CON_POWER	A26570-ND	Digikey
14	Q1	1	SOT23-BCE	MMBT3904	MMBT3904DICT-ND	Digikey
15	Q2, Q7	2	SOT23-BCE	MMBT5401	MMBT5401DICT-ND	Digikey
16	Q3, Q4, Q5, Q6	4	DirectFet	IRF6645	IRF6645	IR
17	R1, R2	2	0805	0R	P0.0ACT-ND	Digikey
18	R3, R4	2	0805	100R	P100ACT-ND	Digikey
19	R5, R6	2	0805	3.3K	P3.3KACT-ND	Digikey
20	R7, R8	2	0805	10.0K ,1%	P10.0KCCT-ND	Digikey
21	R9, R10	2	0805	10R	P10ACT-ND	Digikey
22	R11, R31, R33, R35, R40, R41	6	0805	100K	P100KACT-ND	Digikey
23	R12	1	0805	4.7K	P4.7KACT-ND	Digikey
24	R13, R14	2	0805	8.2K	P8.2KACT-ND	Digikey
25	R17, R18	2	0805	1.74K,1%	P1.74KCCT-ND	Digikey
26	R19, R20	2	0805	1.30K, 1%	P1.30KCCT-ND	Digikey
27	R21, R22, R24, R39	4	0805	1K	P1.0KACT-ND	Digikey
28	R23, R26, R27, R28, R29, R30	6	0805	4.7R	P4.7ACT-ND	Digikey
29	R25, R32	2	0805	47K	P47KACT-ND	Digikey
30	R36	1	0805	10K	P10KACT-ND	Digikey
31	R37, R38	2	0805	1R	P1.0ACT-ND	Digikey
32	Rp1, Rp2	2	0805	100C	594-2322-675-21007	MOUSER
33	TP1, TP2	2	TP	TP	OPEN	
34	U1, U2	2	SO-14	IRS20124S	IRS20124S	IR

IRAUDAMP3 PCB Specifications

Motherboard:

Material:	FR4, UL 125°C
Layer Stack:	1 Layer, 2 oz. Cu
Dimensions:	5.014” x 13.685” x 0.062”
Solder Mask:	LPI Solder mask, SMOBC on top and bottom layers
Plating:	Open copper solder finish
Silkscreen:	On top and bottom layers



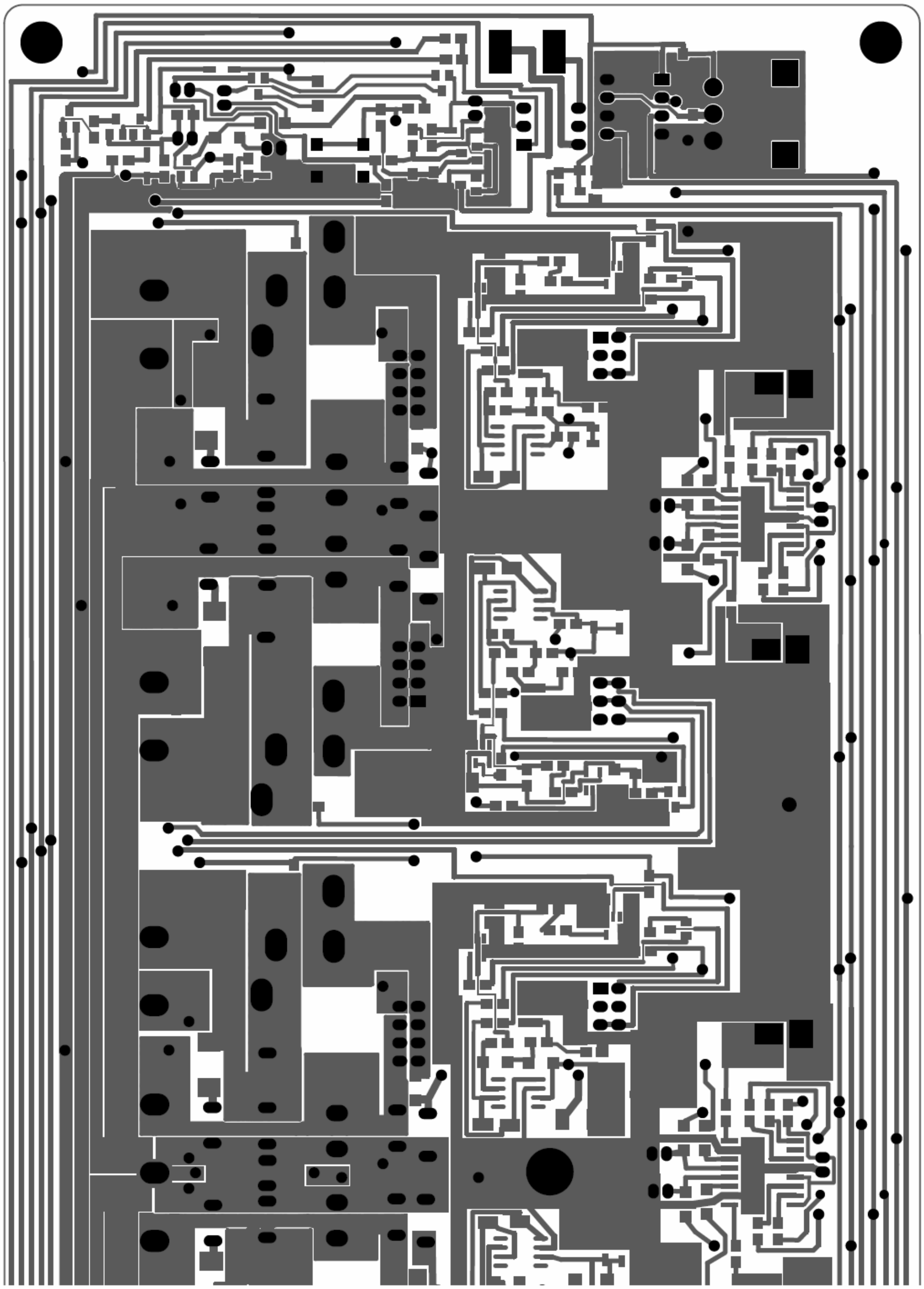
Daughter-board layer stack

Daughter-board:

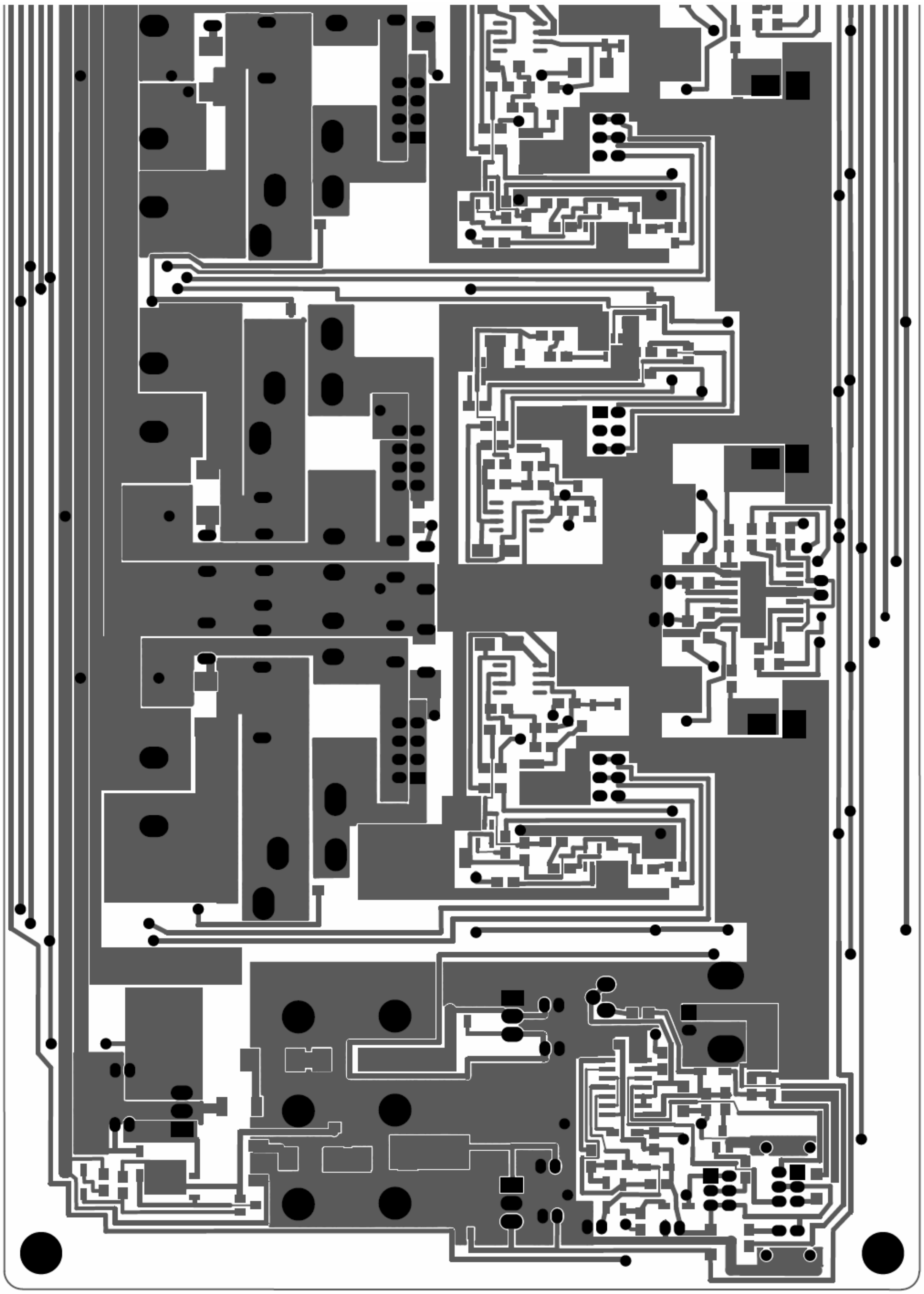
Material:	FR4, UL 125°C
Layer Stack:	2 Layers, 2 oz. Cu each, through-hole plated
Dimensions:	3.127” x 1.492” x 0.062”
Solder Mask:	LPI Solder mask, SMOBC on top and bottom layers (BLACK)
Plating:	Open copper solder finish
Silkscreen:	On top and bottom layers (RED)

IRAUDAMP3 PCB Layers

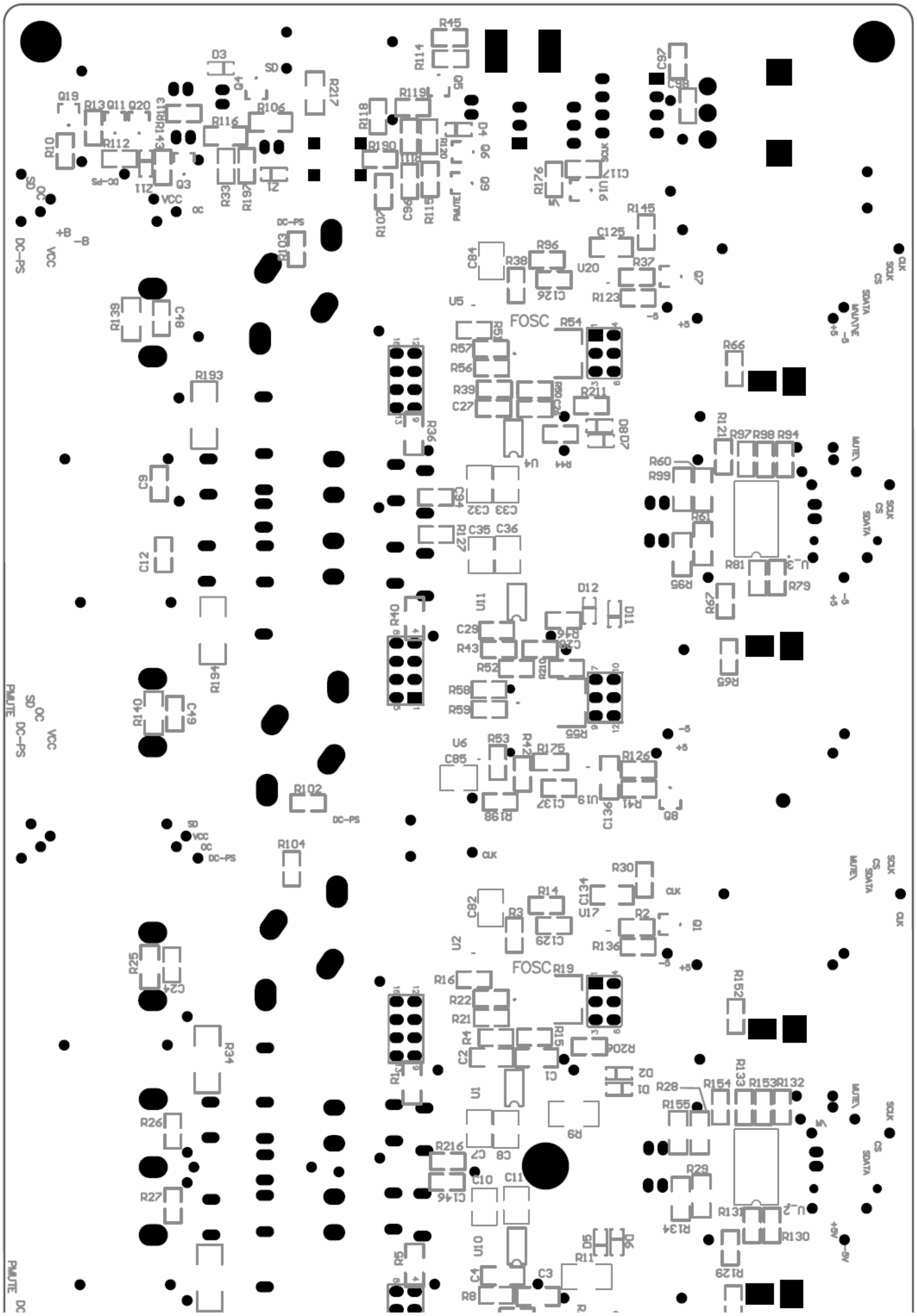
Motherboard:



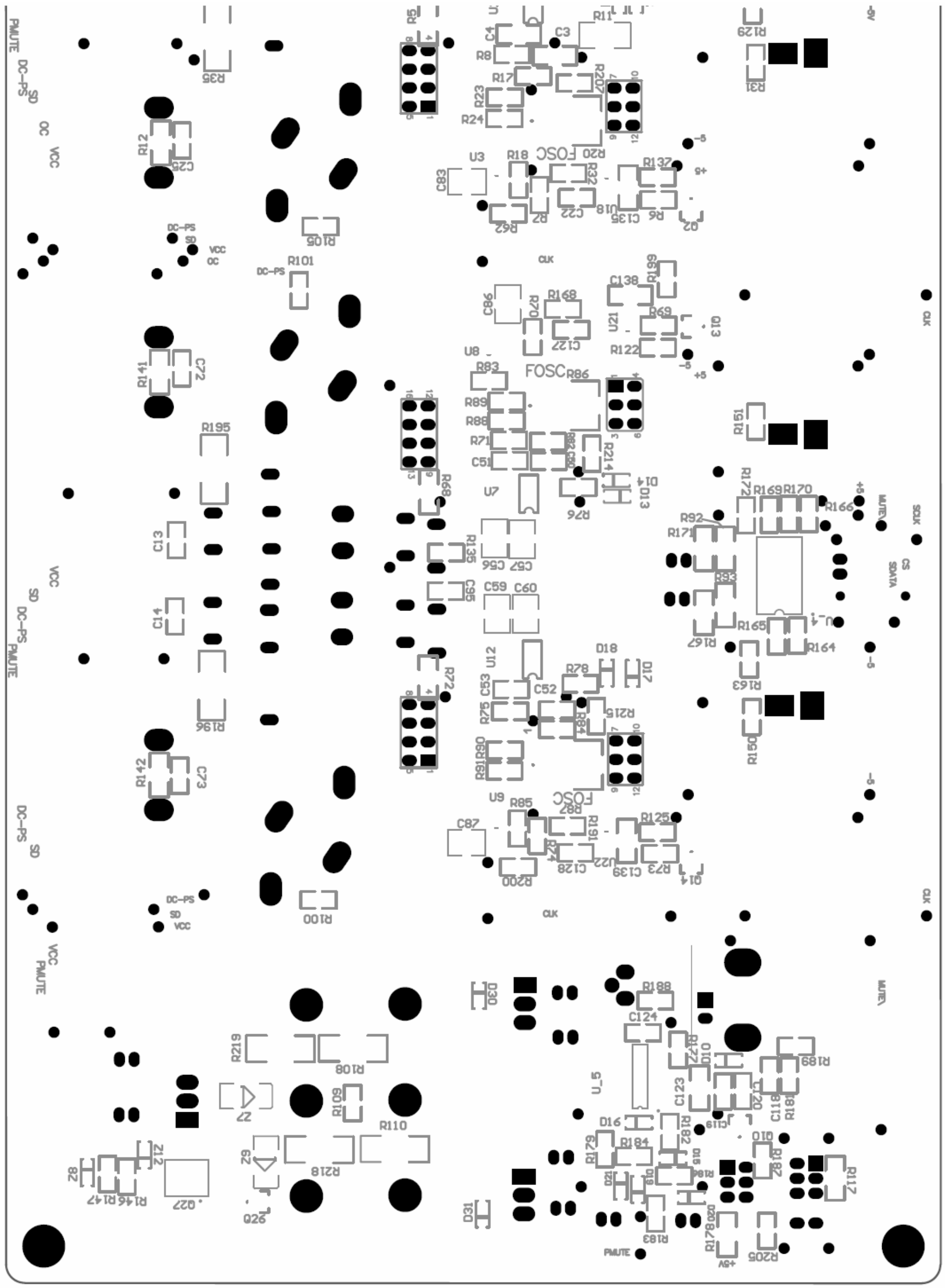
Bottom layer and pads (1 of 2)



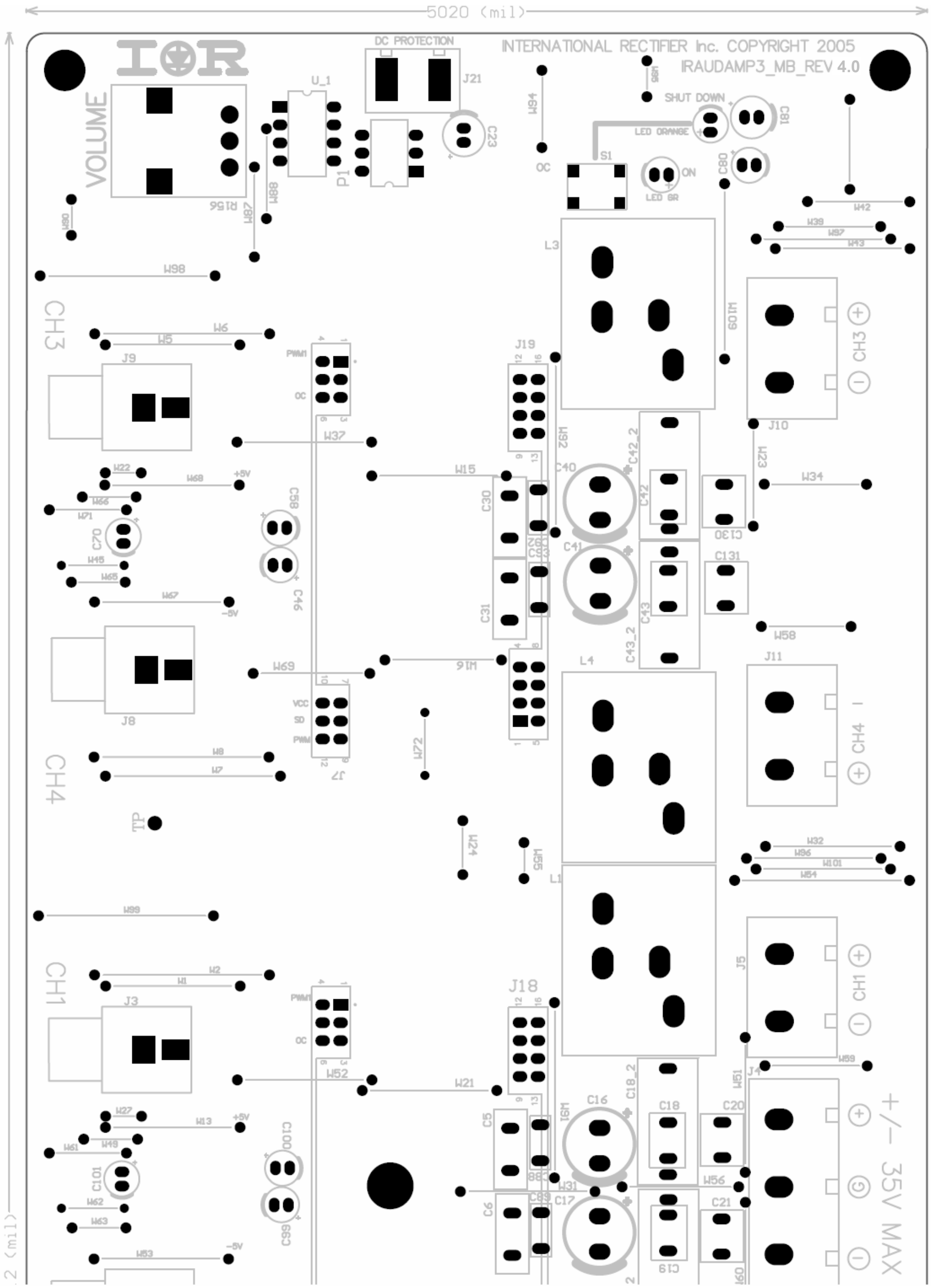
Bottom layer and pads (2 of 2)



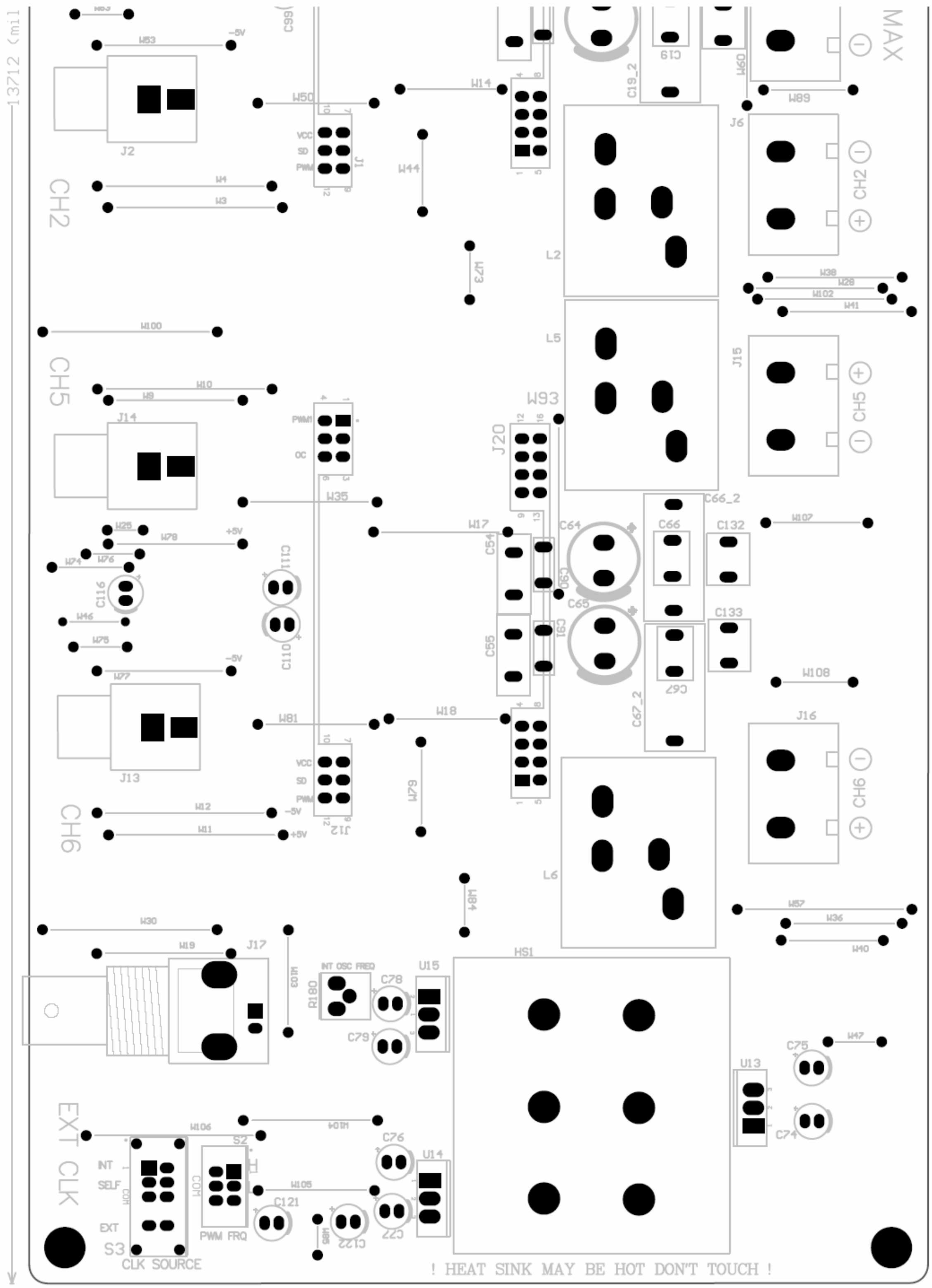
Bottom-side solder-mask and silkscreen (1 of 2)



Bottom-side solder-mask and silkscreen (2 of 2)

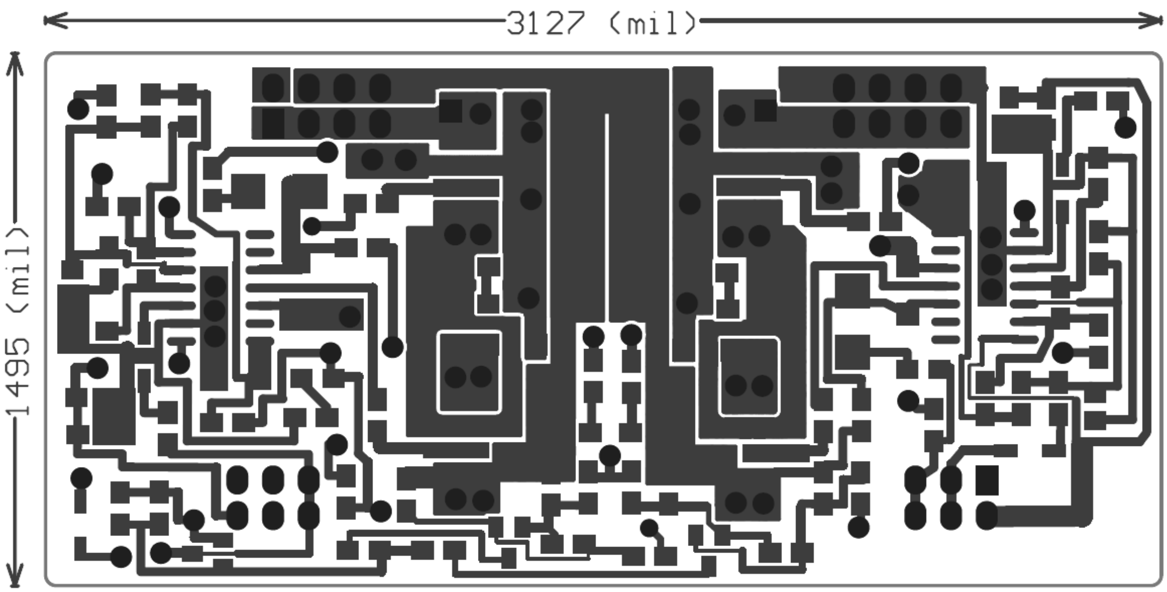


Top-side solder-mask and silkscreen (1 of 2)

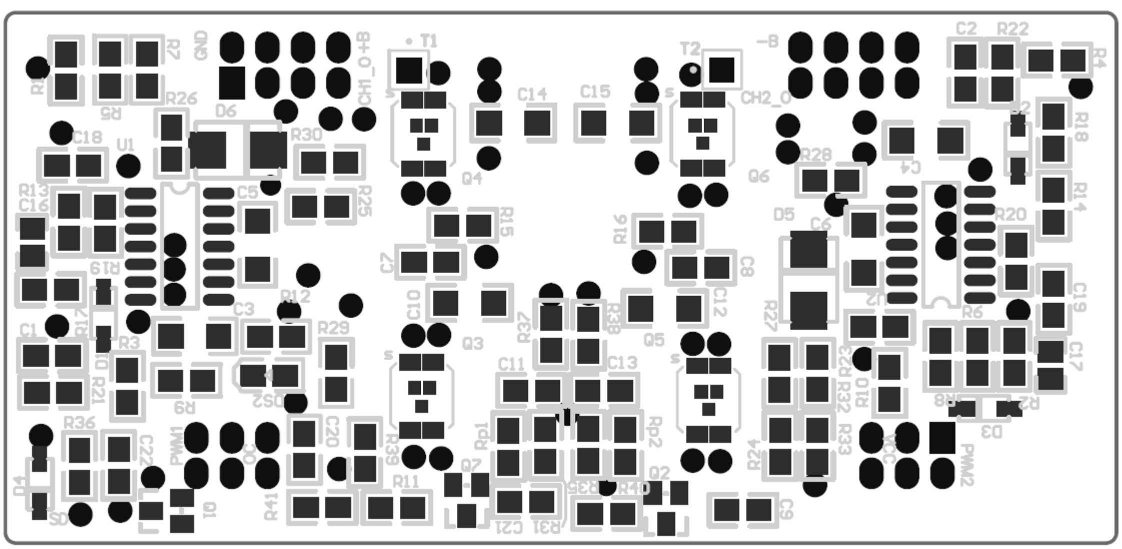

MAX
CH2
CH5
CH6
J2
J14
J13
J6
J15
J16
J17
J20
L2
L5
L6
HS1
U13
U14
U15
EXT CLK
S3
CLK SOURCE
PWM FRQ
INT OSC FREQ
W93
! HEAT SINK MAY BE HOT DON'T TOUCH !

Top-side solder-mask and silkscreen (2 of 2)

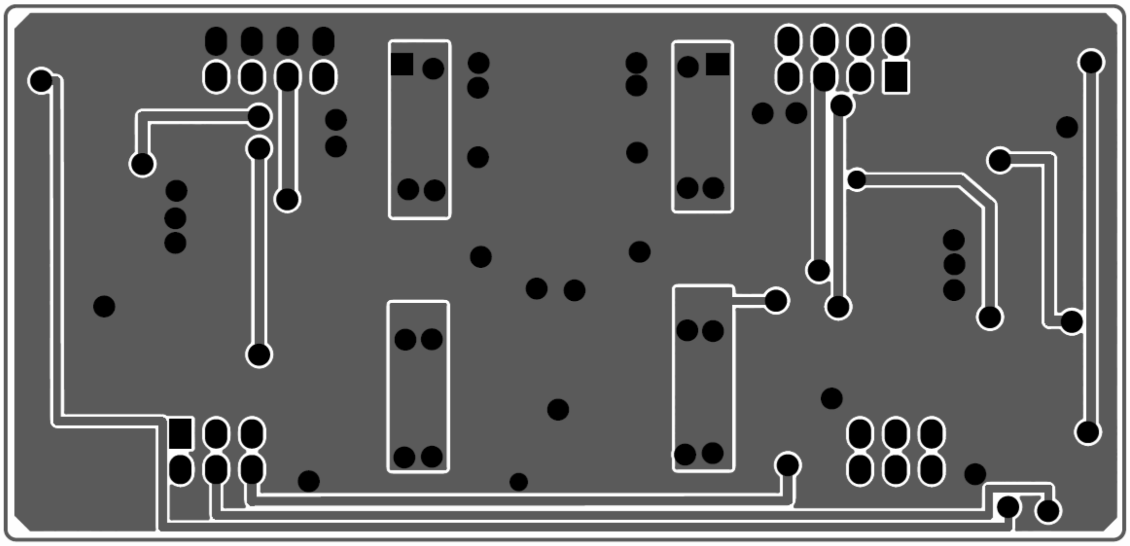
Daughter Board:



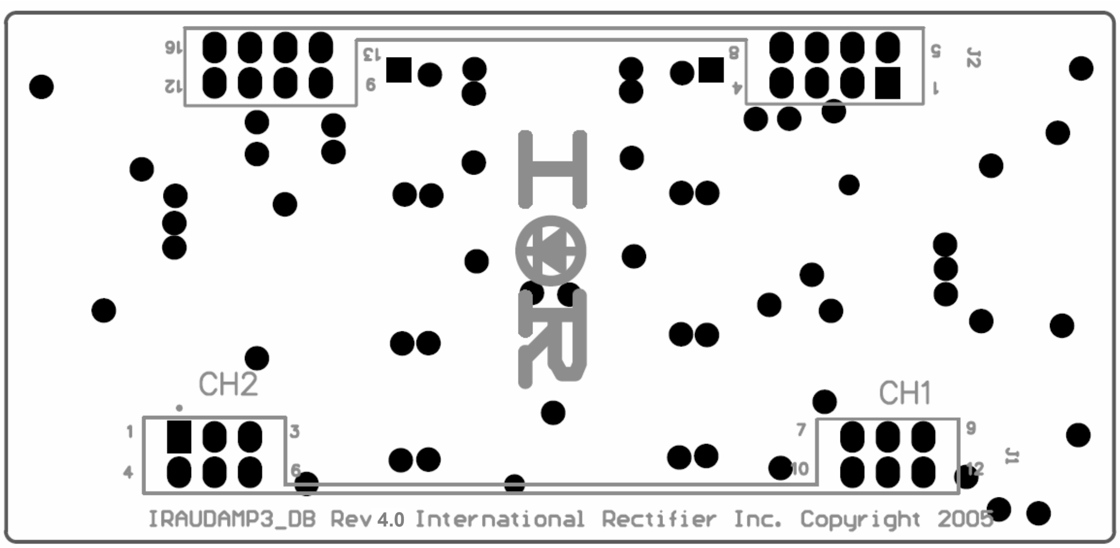
PCB Layout – Top layer and pads



PCB Layout – Top-side solder-mask and silkscreen



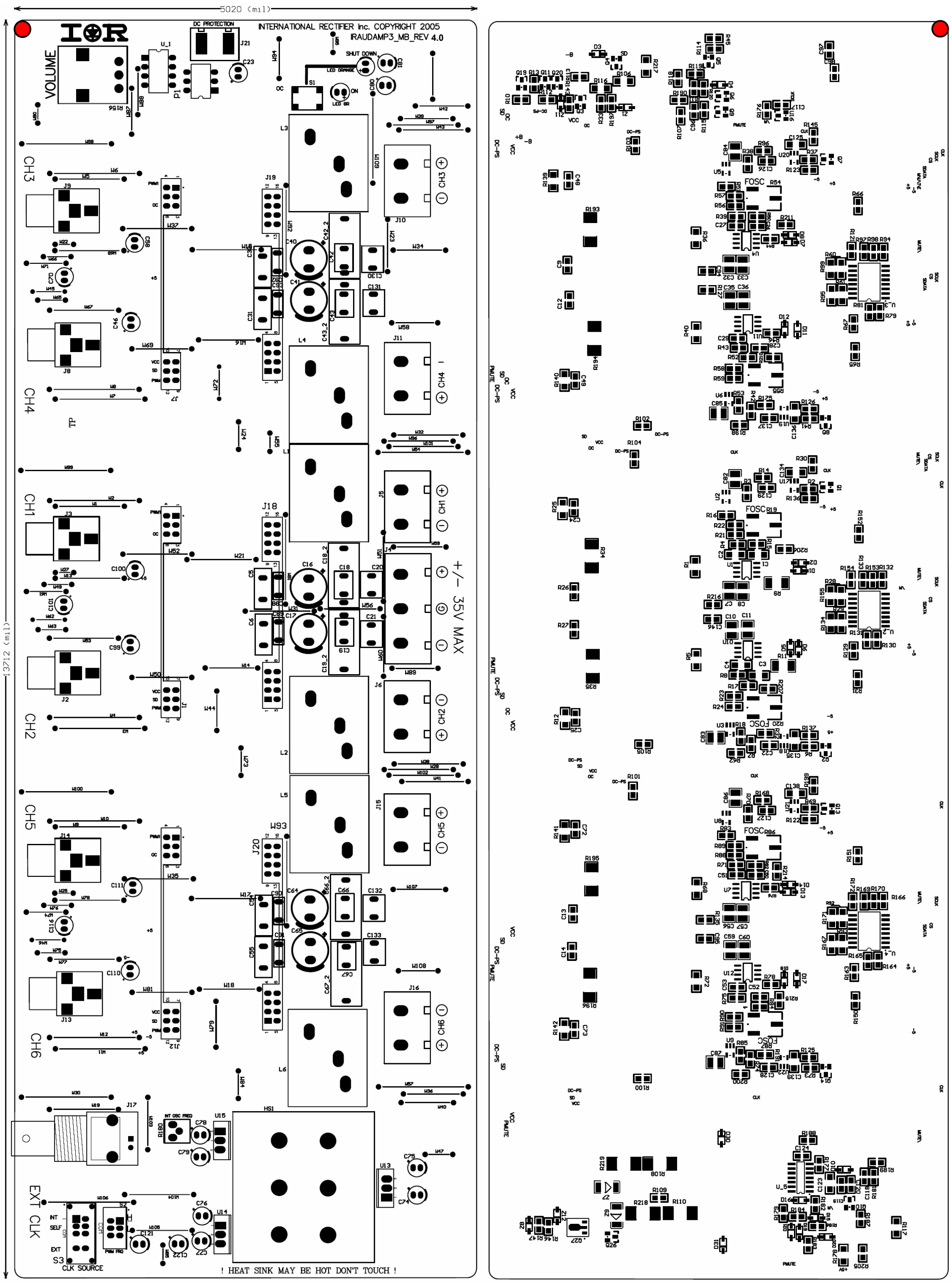
PCB Layout – Bottom layer and pads



PCB Layout – Bottom-side solder-mask and silkscreen

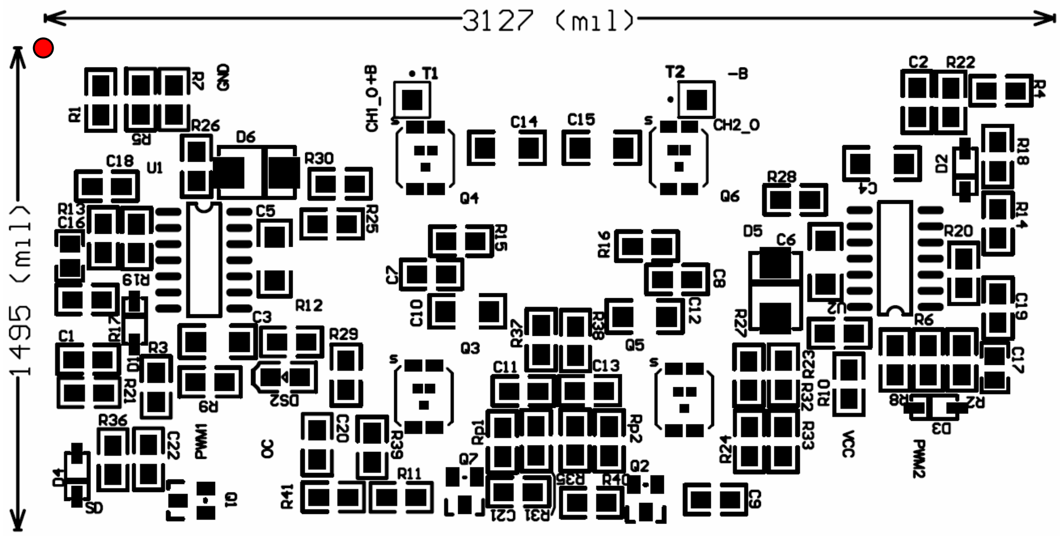
IRAUDAMP3 Mechanical Construction

Motherboard

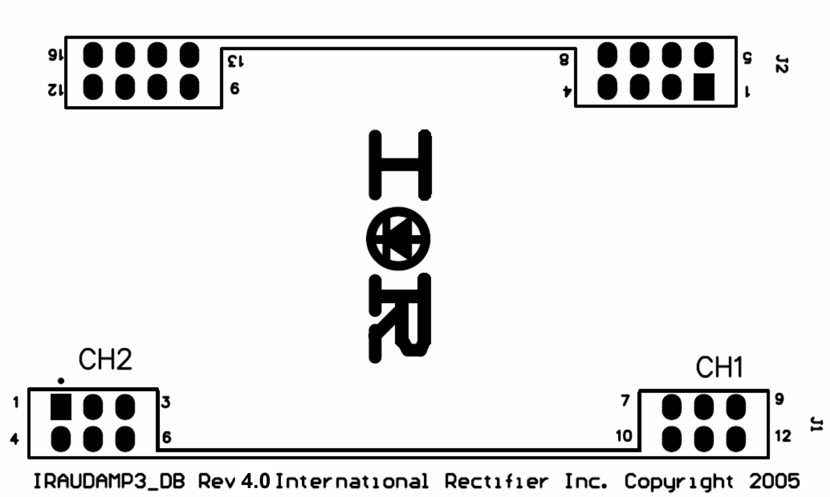


Top and bottom sides of motherboard showing component locations

Daughter Board



Top side showing component locations



Bottom side showing connector locations

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