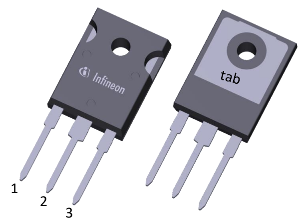
MOSFET

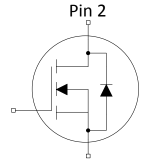
StrongIRFET™ Power MOSFET, 100 V

PG-TO247-3



Features

- Very low on-resistance $R_{ds(on)}$
- Excellent gate charge x $R_{ds(on)}$ (FOM)
- Optimized Q_{rr}
- 175°C operating temperature
- Product validation according to JEDEC standard
- Optimized for broadest availability from distribution partners



Benefits

- Reduced conduction losses
- Ideal for high switching frequency
- Lower overshoot voltage
- Increased reliability versus 150°C rated parts
- Pb-free lead plating; RoHS compliant
- Lead free, Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	1.7	mΩ
I_D	203	A
Q_{oss}	213	nC
Q_G (0V..10V)	168	nC

Type / Ordering code	Package	Marking	Related links
IRF100P219	PG-TO247-3	IRF100P219	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	203 156 33	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{THJA}=40 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	812	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	464	mJ	I_D=100 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	341 3.8	W	T_C=25 °C T_A=25 °C, R_{THJA}=40 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

1) Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

2) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3) See Diagram 3 for more detailed information.

4) See Diagram 13 for more detailed information.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.3	0.44	°C/W	-
Thermal resistance, junction - ambient [5)]	R_{thJA}	-	-	40	°C/W	
Case-to-Sink, Flat Greased Surface	R_{thCS}	-	0.24	-	°C/W	

5) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.3	3.0	3.8	V	V_{DS}=V_{GS}, I_D=278 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.4 1.7	1.7 2.1	mΩ	V_{GS}=10 V, I_D=100 A V_{GS}=6 V, I_D=50 A
Gate resistance	R_G	-	1.2	-	Ω	-
Transconductance [6]	g_{fs}	135	270	-	S	$\|V_{DS}\|≥2\|I_D\|R_{DS(on)max}$, I_D=100 A

[6] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [7]	C_{iss}	-	12000	16000	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance [7]	C_{oss}	-	1800	2300	pF	
Reverse transfer capacitance [7]	C_{rss}	-	80	140	pF	
Turn-on delay time	$t_{d(on)}$	-	67	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	106	-	ns	
Turn-off delay time	$t_{d(off)}$	-	132	-	ns	
Fall time	t_f	-	47	-	ns	

[7] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [8)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	53	-	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	36	-	nC	
Gate to drain charge [9)]	Q_{gd}	-	34	51	nC	
Switching charge	Q_{sw}	-	51	-	nC	
Gate charge total [9)]	Q_g	-	168	210	nC	
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	146	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge [9)]	Q_{oss}	-	213	320	nC	V_{DS}=50 V, V_{GS}=0 V

8) See figure 16 for gate charge parameter definition·

9) Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	173	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	812	A	
Diode forward voltage	V_{SD}	-	0.86	1.0	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	63	-	ns	V_R=50 V, I_F=100 A, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	111	-	nC	

4 Electrical characteristics diagrams

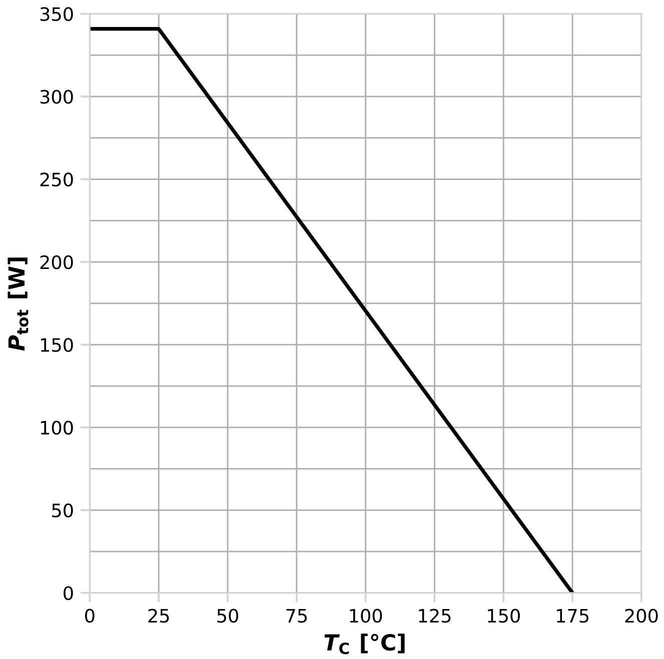
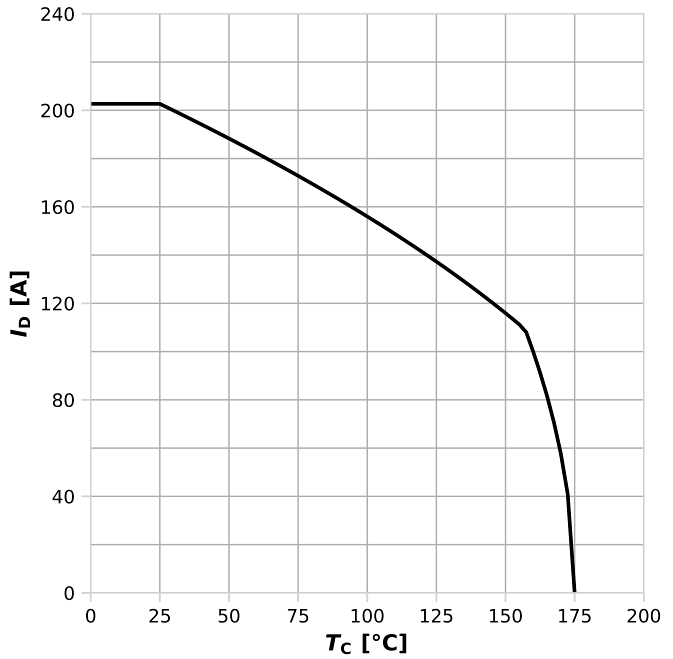
Diagram 1: Power dissipation	Diagram 2: Drain current
	
P_{tot}=f(T_C)	I_D=f(T_C); V_{GS}≥10 V

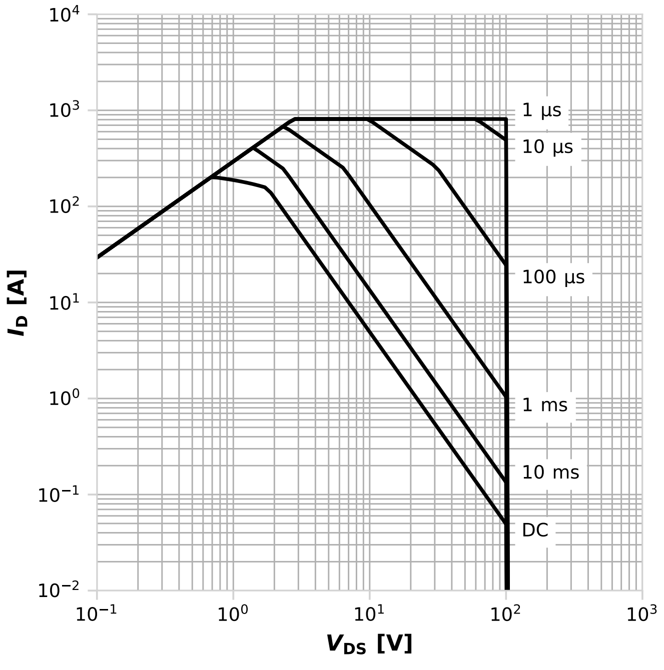
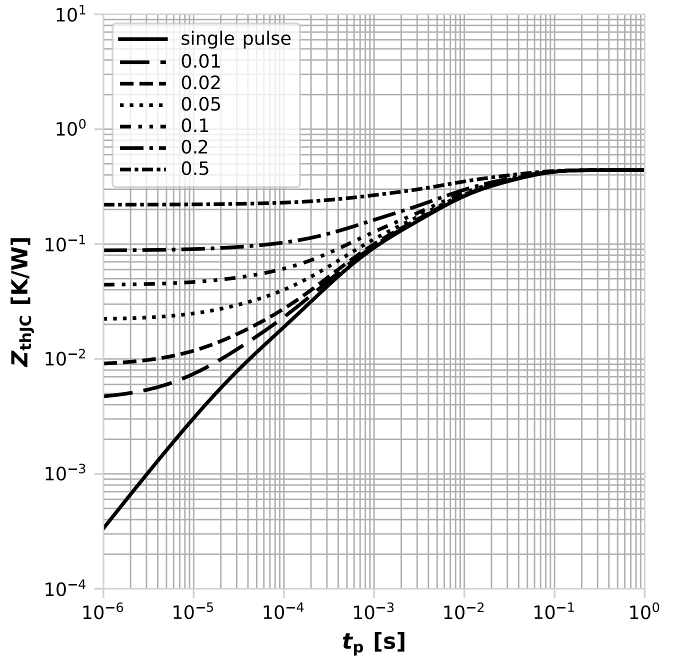
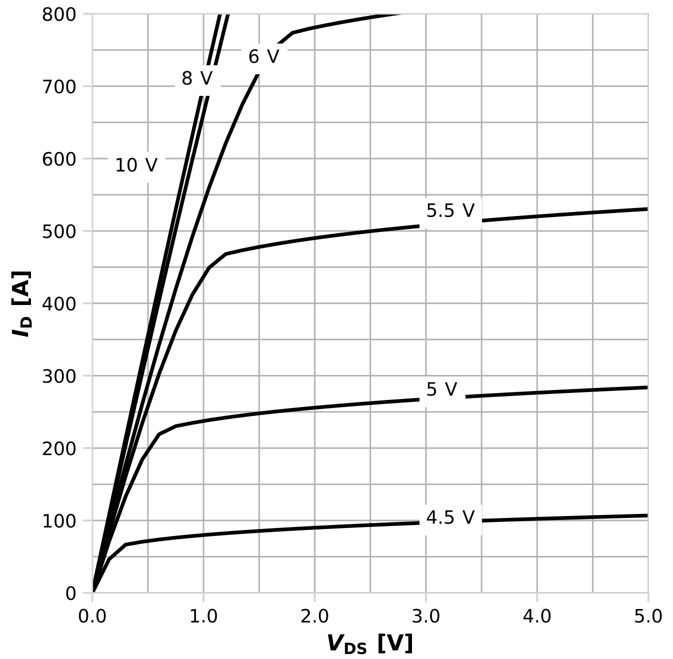
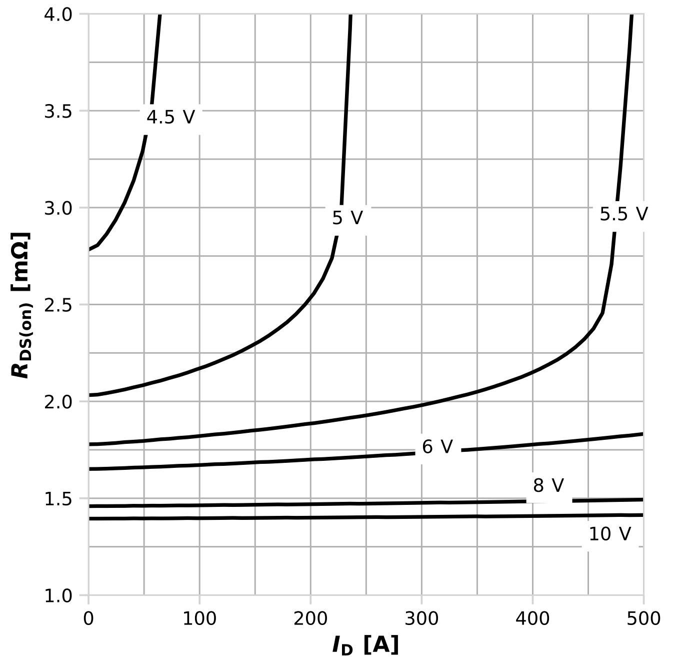
Diagram 3: Safe operating area	Diagram 4: Max. transient thermal impedance
	
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p	Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



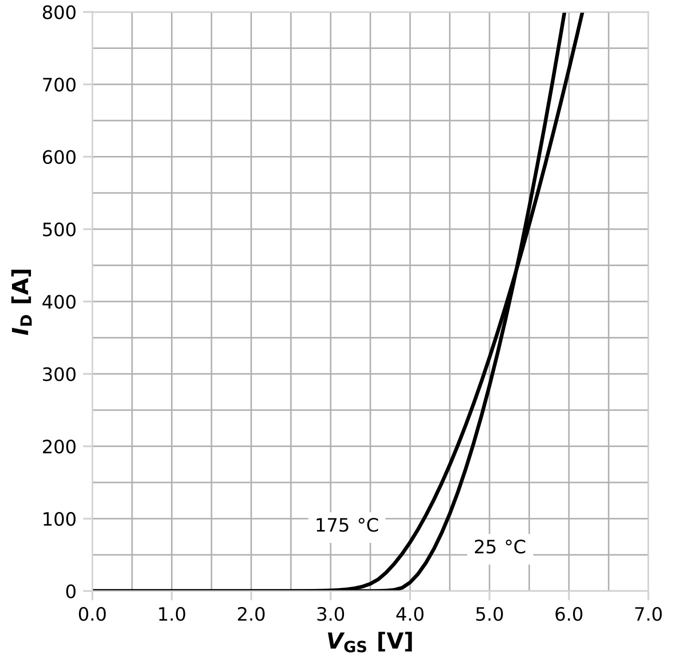
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



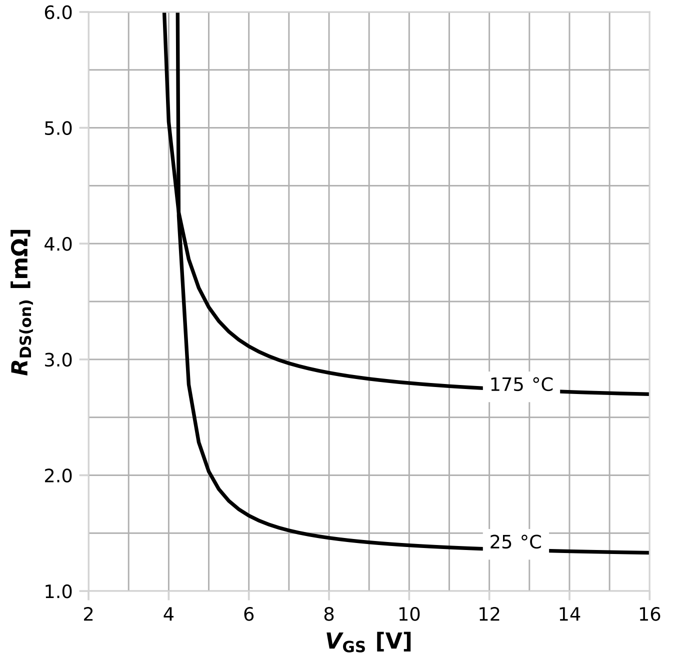
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}), $|V_{DS}|$>2$|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}$=f(V_{GS}), I_D=0 A; parameter: T_j

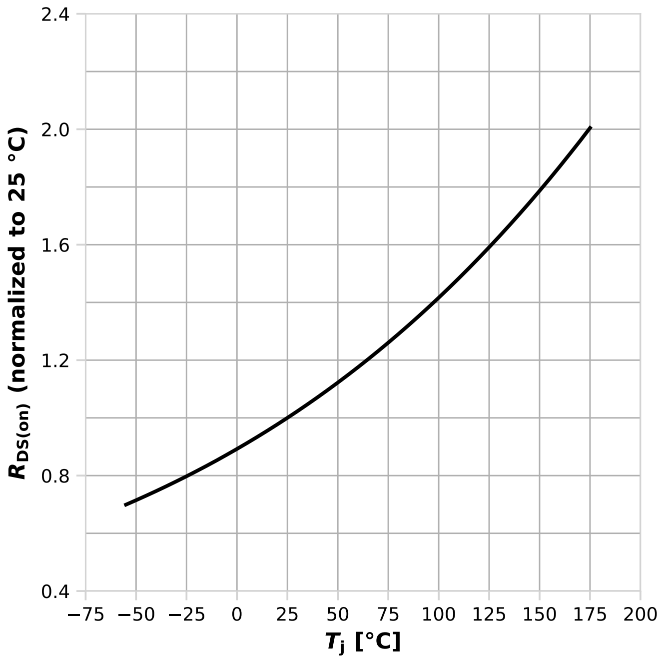
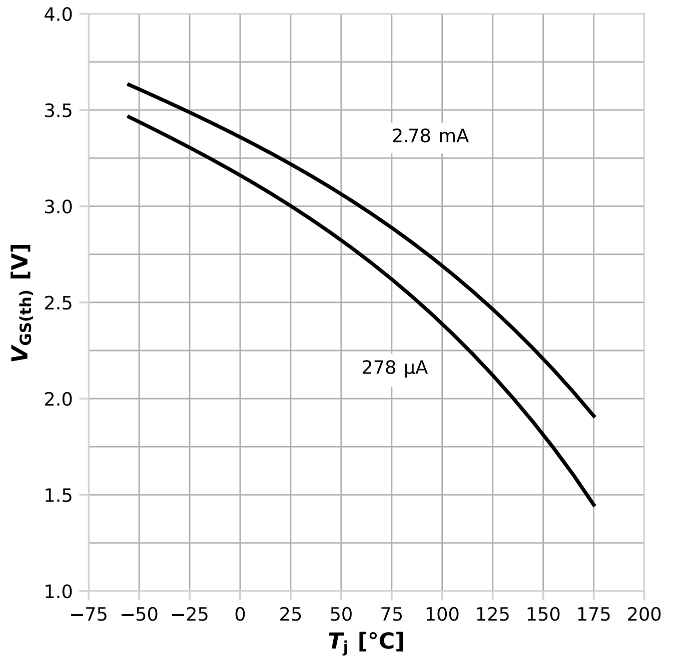
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=0 A, V_{GS}=10 V	$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

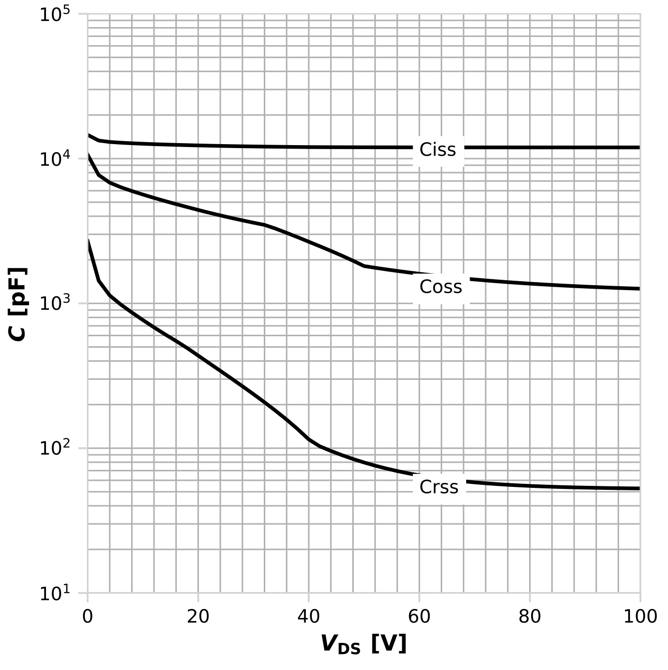
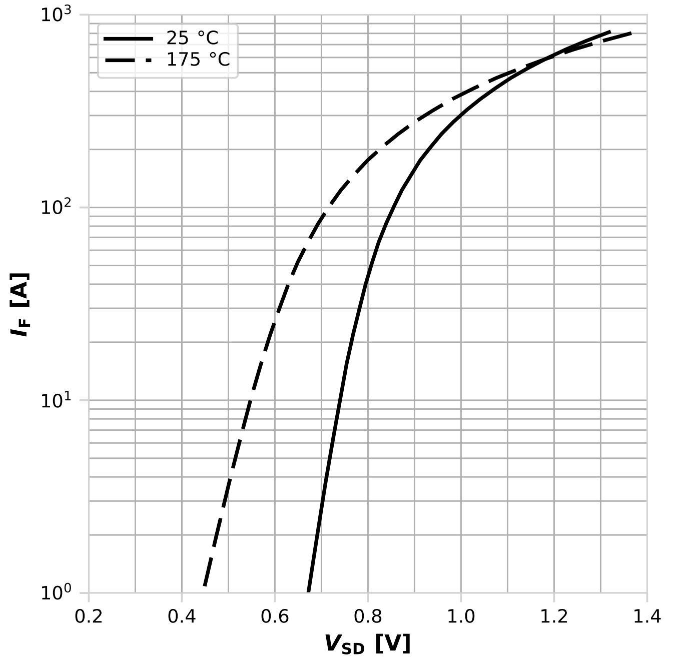
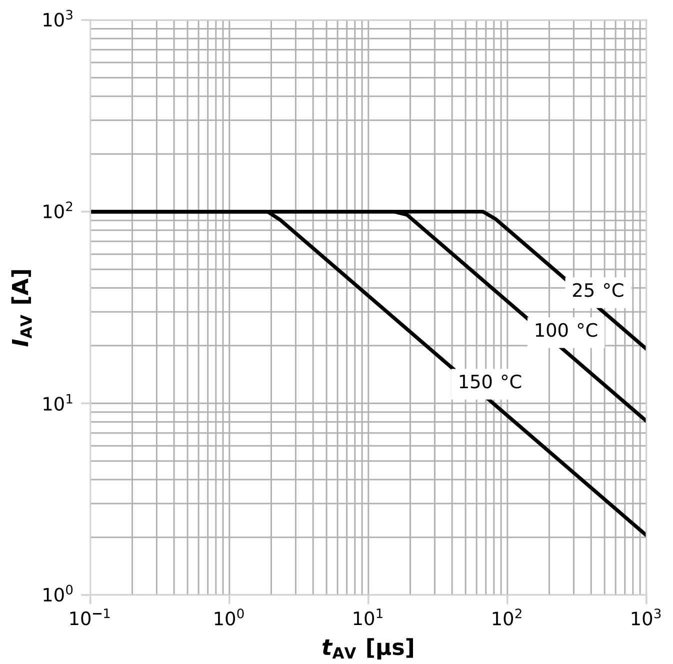
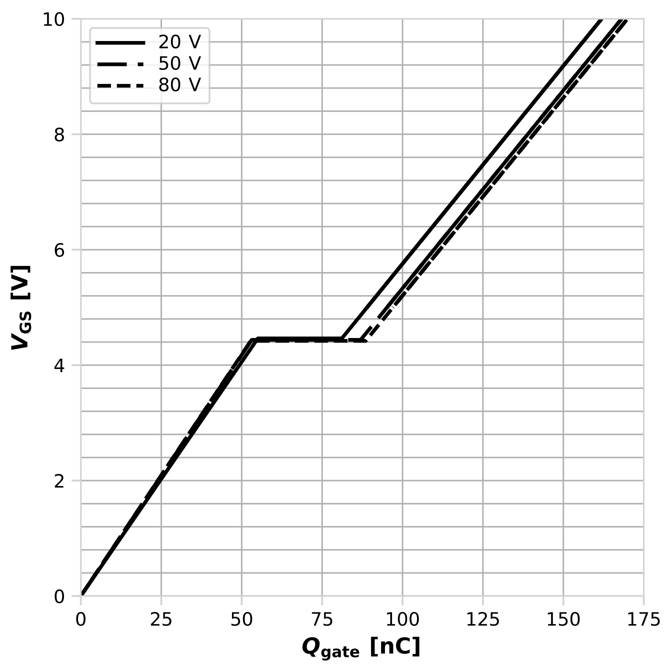
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



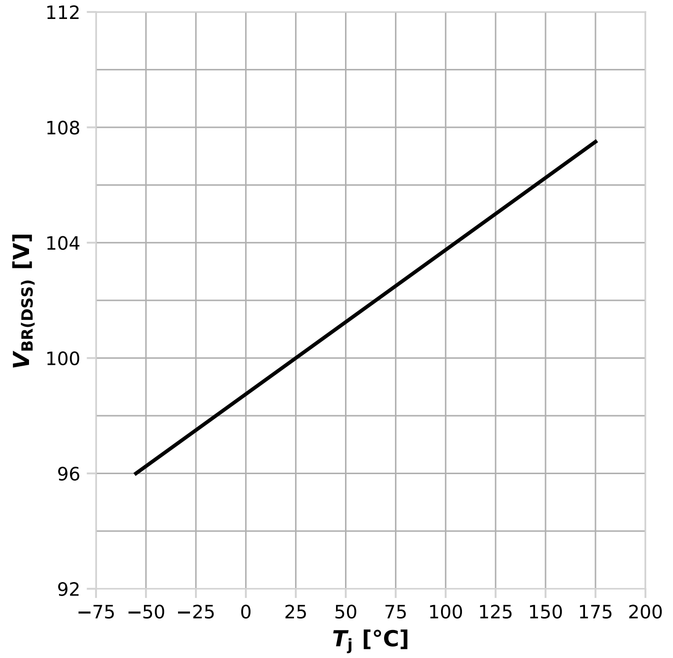
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



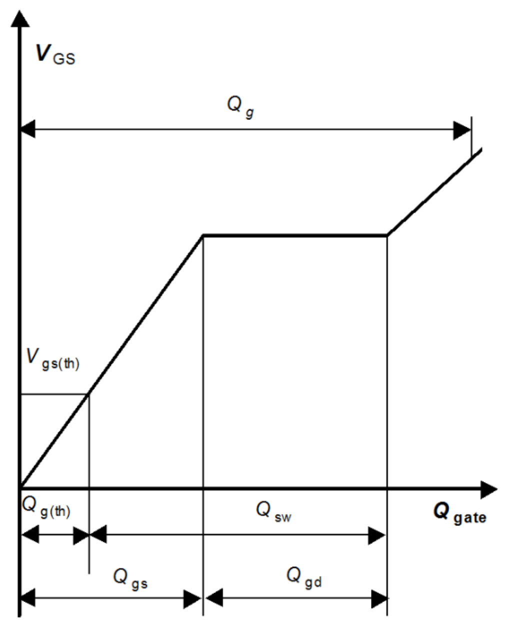
V_{GS}=f(Q_{gate}), I_D=100 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Gate charge waveforms



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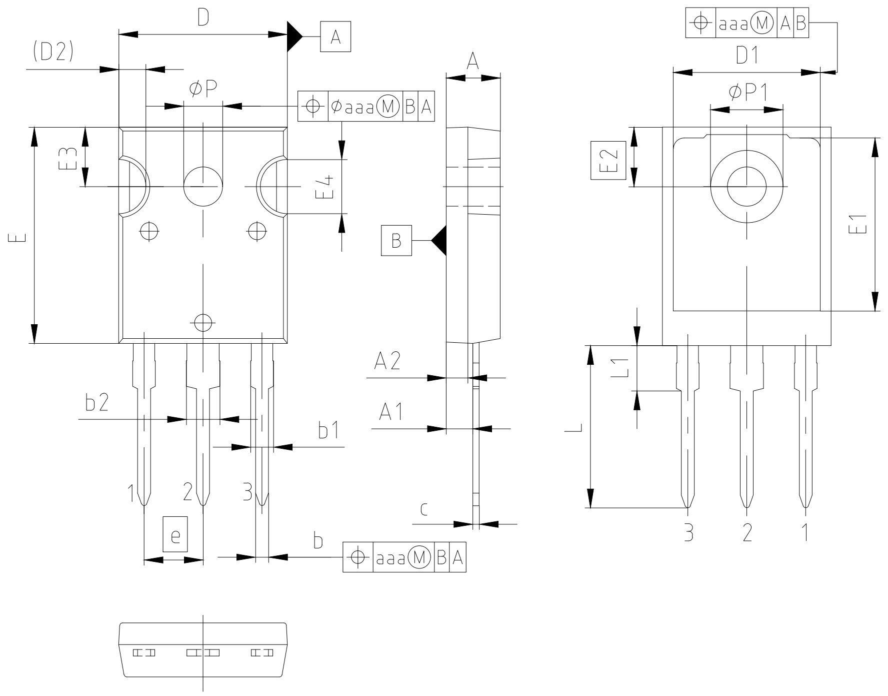
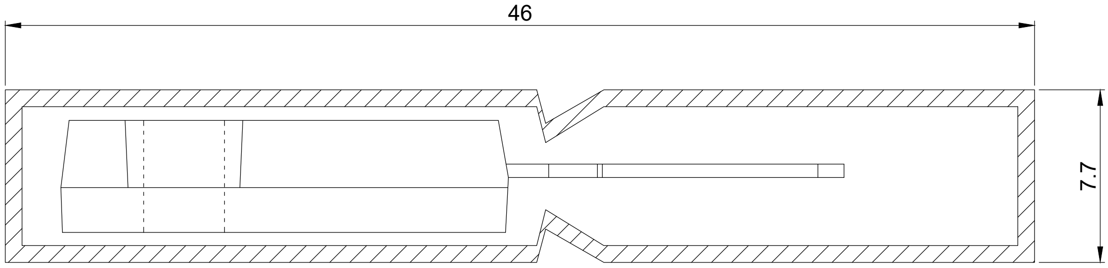
5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TO247-3-U03				
DIMENSIONS	**MILLIMETERS**		**DIMENSIONS**	**MILLIMETERS**	
	MIN.	MAX.		MIN.	MAX.
A	4.83	5.13	**E2**	5.51	
A1	2.21	2.59	**E3**	5.31	5.69
A2	1.50	2.50	**E4**	4.50	5.50
b	0.99	1.41	**e**	5.46	
b1	1.65	2.39	**L**	14.20	16.10
b2	2.59	3.43	**L1**	3.71	4.29
c	0.38	0.89	**N**	3	
D	15.29	15.87	**ØP**	3.56	3.66
D1	13.46	13.66	**ØP1**	7.19	7.39
D2	2.50		**aaa**	0.25	
E	19.70	20.70			
E1	13.08	13.28			

NOTES: (1) DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
(2) N IS THE NUMBER OF LEADS

Figure 1 Outline PG-TO247-3, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 2 **Packaging variant PG-TO247-3, dimensions in mm**

Revision history

IRF100P219

Revision 2025-01-09, Rev. 2.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2018-10-16	Release of final version
2.1	2020-01-20	Update from IR MOSFT/StrongIRFET™ to StrongIRFET™
2.2	2025-01-09	updated switch time and trr

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