

## N-Channel Power MOSFET (14A, 500Volts)

### DESCRIPTION

The Nell **IRF13N50** are N-channel enhancement mode silicon gate power field effect transistors.

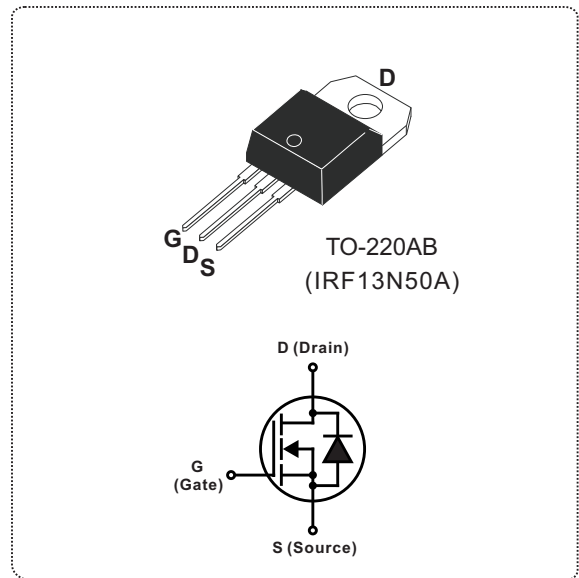
They are designed, tested and guaranteed to withstand level of energy in breakdown avalanche mode of operation.

They are designed as an extremely efficient and reliable device for use in a wide variety of applications such as SMPS, UPS, converters, motor drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power.

These transistors can be operated directly from integrated circuits.

### FEATURES

- $R_{DS(ON)} = 0.45\Omega @ V_{GS} = 10V$
- Ultra low gate charge(81nC max.)
- Low reverse transfer capacitance ( $C_{RSS} = 11pF$  typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature



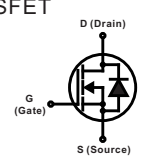
PRODUCT SUMMARY	
$I_D$ (A)	14
$V_{DSS}$ (V)	500
$R_{DS(ON)}$ ( $\Omega$ )	0.45 @ $V_{GS} = 10V$
$Q_G$ (nC) max.	81

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ C$ unless otherwise specified)				
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
$V_{DSS}$	Drain to Source voltage(Note 1)	$T_J=25^\circ C$ to $150^\circ C$	500	V
$V_{DGR}$	Drain to Gate voltage	$R_{GS}=20K\Omega$	500	
$V_{GS}$	Gate to Source voltage		$\pm 30$	
$I_D$	Continuous Drain Current	$V_{GS}=10V, T_C=25^\circ C$	14	A
		$V_{GS}=10V, T_C=100^\circ C$	9.1	
$I_{DM}$	Pulsed Drain current (Note 1)		56	
$I_{AR}$	Repetitive avalanche current (Note 1)		14	
$E_{AR}$	Repetitive avalanche energy(Note 1)	$I_{AR}=14A, R_{GS}=50\Omega, V_{GS}=10V$	25	mJ
$E_{AS}$	Single pulse avalanche energy (Note 2)	$I_{AS}=14A, L=5.7mH$	560	mJ
dv/dt	Peak diode recovery dv/dt(Note 3)		9.2	V/ns
$P_D$	Total power dissipation	$T_C=25^\circ C$	250	W
	Derating factor above $25^\circ C$		1.9	W/ $^\circ C$
$T_J$	Operation junction temperature		-55 to 150	$^\circ C$
$T_{STG}$	Storage temperature		-55 to 150	
$T_L$	Maximum soldering temperature, for 10 seconds	1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf-in (N-m)

Note: 1.Repetitive rating: pulse width limited by junction temperature.  
 2.  $V_{DD}=50V, L=5.7mH, I_{AS}=14A, R_G=25\Omega, dV/dt=7.6 V/ns$ , starting  $T_J=25^\circ C$   
 3.  $I_{SD} \leq 14A, di/dt \leq 250A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ C$ .

THERMAL RESISTANCE						
SYMBOL	PARAMETER	Min.	Typ.	Max.	UNIT	
$R_{th(j-c)}$	Thermal resistance, junction to case			0.50	°C/W	
$R_{th(c-s)}$	Thermal resistance, case to heatsink		0.5			
$R_{th(j-a)}$	Thermal resistance, junction to ambient			62		

ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
⊙ STATIC						
$V_{(BR)DSS}$	Drain to source breakdown voltage	$V_{GS} = 0V, I_D = 250\mu A$	500			V
$V_{(BR)DSS}/T_J$	Breakdown voltage temperature coefficient	$I_D = 1mA$ , referenced to $25^\circ\text{C}$		0.55		V/°C
$I_{DSS}$	Drain to source leakage current	$V_{DS}=500V, V_{GS}=0V$ $T_C = 25^\circ\text{C}$			25	$\mu A$
		$V_{DS}=400V, V_{GS}=0V$ $T_C = 125^\circ\text{C}$			250	
$I_{GSS}$	Gate to source forward leakage current	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
	Gate to source reverse leakage current	$V_{GS} = -30V, V_{DS} = 0V$			-100	
$R_{DS(ON)}$	Static drain to source on-state resistance	$V_{GS} = 10V, I_D = 8.4A$ (Note 1)			0.45	$\Omega$
$V_{GS(TH)}$	Gate threshold voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	2		4	V
$g_{fs}$	Forward transconductance	$V_{DS}=50V, I_D=8.4A$	8.1			S
⊙ DYNAMIC						
$C_{ISS}$	Input capacitance	$V_{DS} = 25V, V_{GS} = 0V, f = 1MHz$		1910		pF
$C_{OSS}$	Output capacitance			290		
$C_{RSS}$	Reverse transfer capacitance			11		
$C_{OSS}$	Output capacitance	$V_{GS} = 0V$	$V_{DS} = 1.0V, f = 1.0MHz$	2730		pF
			$V_{DS} = 400V, f = 1.0MHz$	82		
$C_{OSS\ eff.}$	Effective output capacitance (Note 2)	$V_{DS} = 0$ to $400V$		160		pF
$t_{d(ON)}$	Turn-on delay time	$V_{DD} = 250V, I_D = 14A, R_G = 7.5\Omega, V_{GS} = 10V, (Note\ 1)$		15		ns
$t_r$	Rise time			39		
$t_{d(OFF)}$	Turn-off delay time			39		
$t_f$	Fall time			31		
$Q_G$	Total gate charge	$V_{DS} = 400V, V_{GS} = 10V, I_D = 14A$			81	nC
$Q_{GS}$	Gate to source charge				20	
$Q_{GD}$	Gate to drain charge (Miller charge)				36	

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
$V_{SD}$	Diode forward voltage	$I_{SD} = 14A, V_{GS} = 0V$			1.5	V
$I_S(I_{SD})$	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET 			14	A
$I_{SM}$	Pulsed source current				56	
$t_{rr}$	Reverse recovery time	$I_{SD} = 14A, V_{GS} = 0V, di_F/dt = 100A/\mu s$		370	550	ns
$Q_{rr}$	Reverse recovery charge			4.4	6.5	$\mu C$
$I_{RRM}$	Reverse recovery current			21	31	A
$t_{ON}$	Forward turn-on time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Note: 1. Pulse test: Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .

2.  $C_{OSS\ eff.}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DS}$

## ORDERING INFORMATION SCHEME

**IRF 13N50 A**

**MOSFET series**

N-Channel, IR series

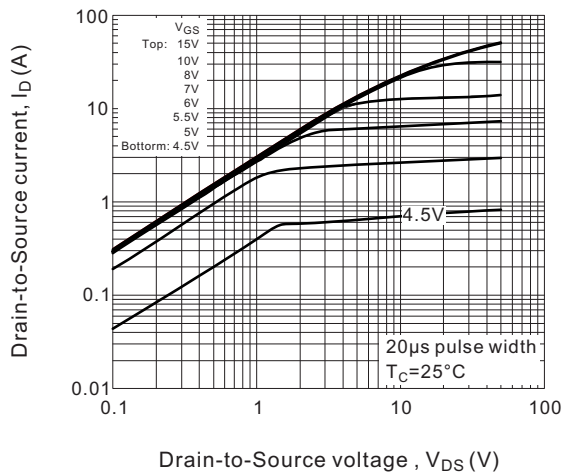
**Current & Voltage rating,  $I_D$  &  $V_{DS}$**

14A / 500V

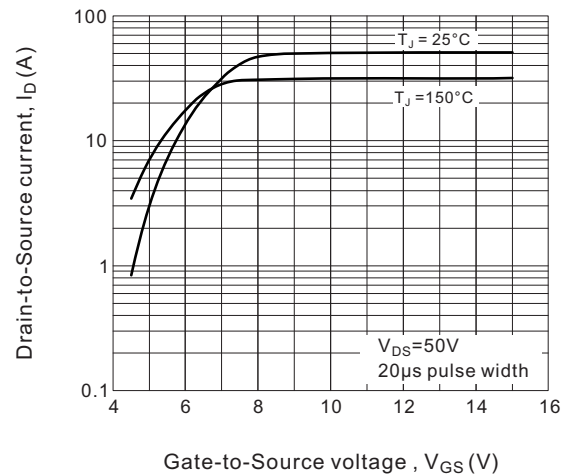
**Package type**

A = TO-220AB

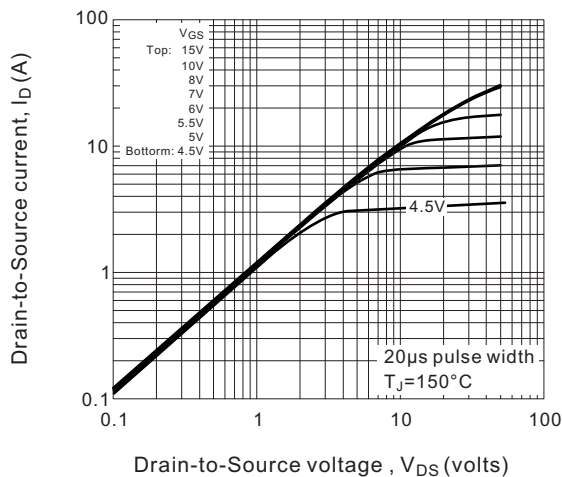
**Fig.1 Typical output characteristics,  $T_C=25^\circ\text{C}$**



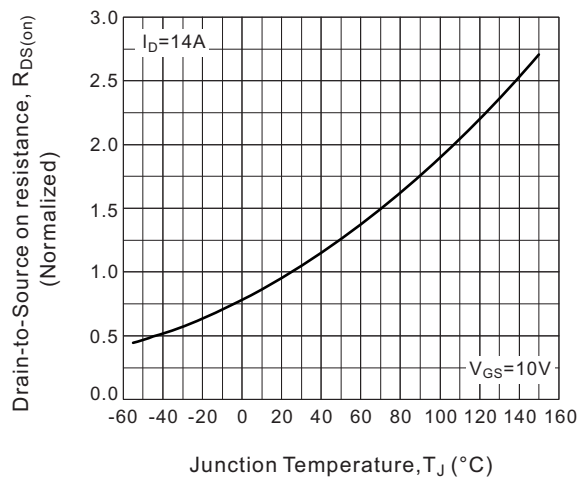
**Fig.2 Typical transfer characteristics**



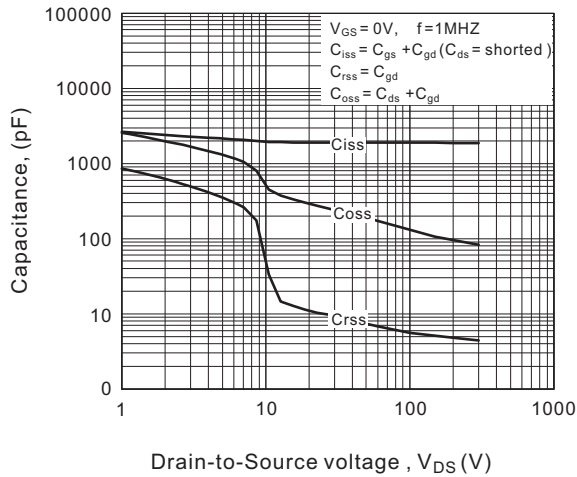
**Fig.3 Typical output characteristics,  $T_C=150^\circ\text{C}$**



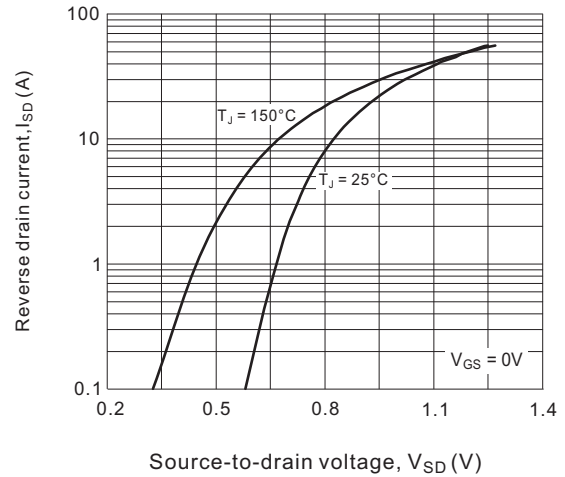
**Fig.4 Normalized On-Resistance vs. Temperature**



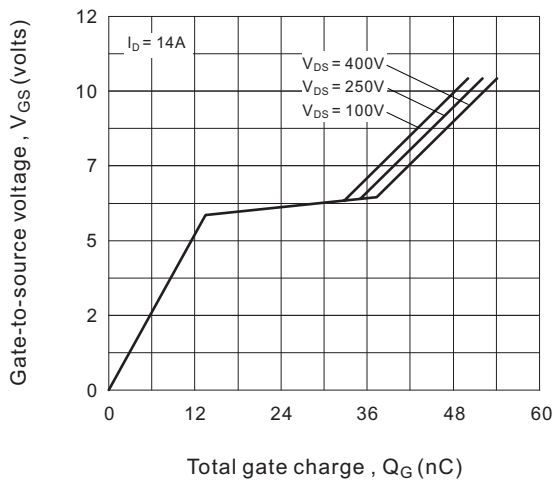
**Fig.5 Typical capacitance vs. Drain-to-Source voltage**



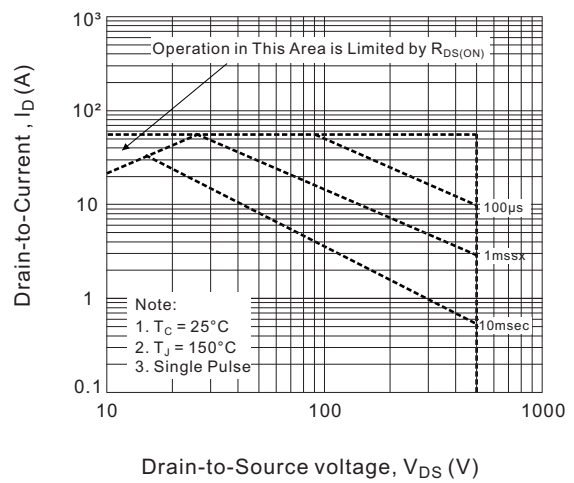
**Fig.6 Typical source-drain diode forward voltage**



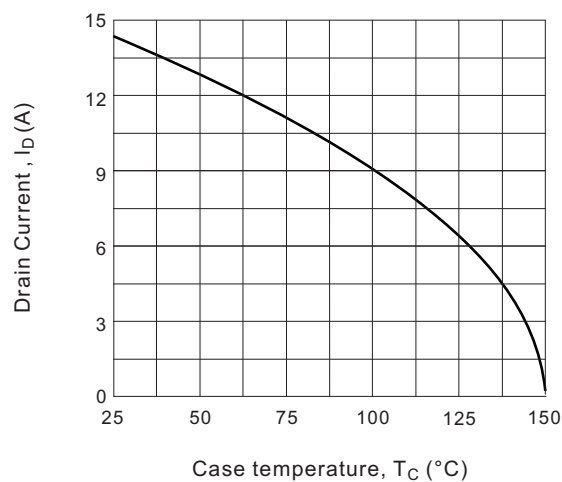
**Fig.7 Typical gate charge vs. gate-to-source voltage**



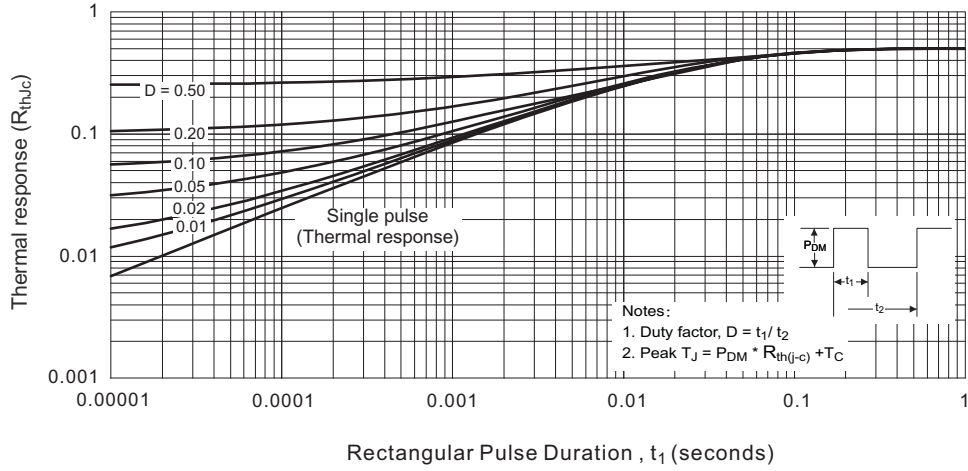
**Fig.8 Maximum safe operating area**



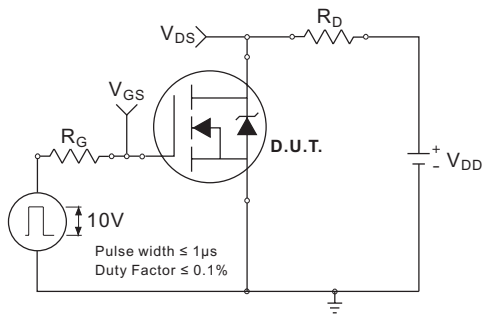
**Fig.9 Maximum drain current vs. Case temperature**



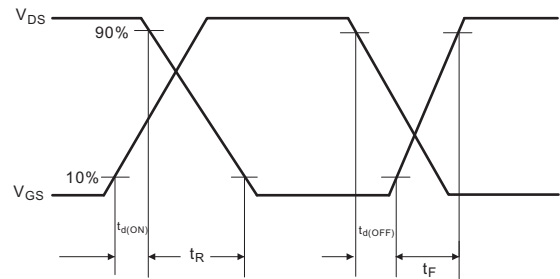
**Fig.10 Maximum effective transient thermal impedance, Junction-to-Case**



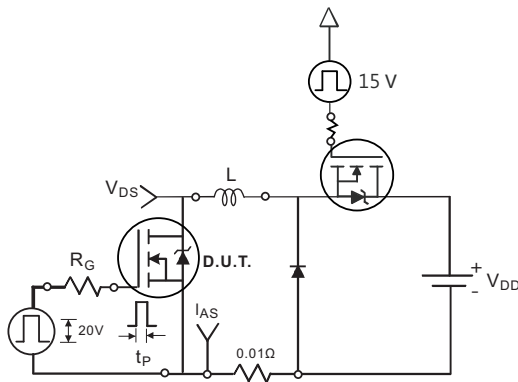
**Fig.11a. Switching time test circuit**



**Fig.11b. Switching time waveforms**

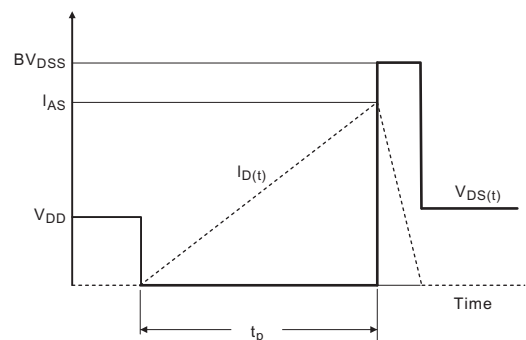


**Fig.12a. Unclamped Inductive test circuit**

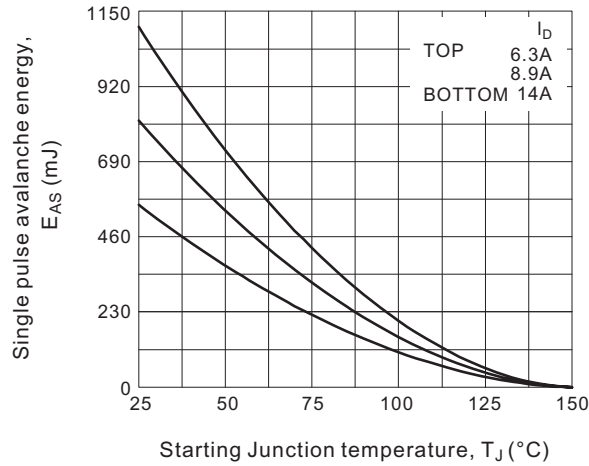


Vary  $t_p$  to obtain required  $I_{AS}$

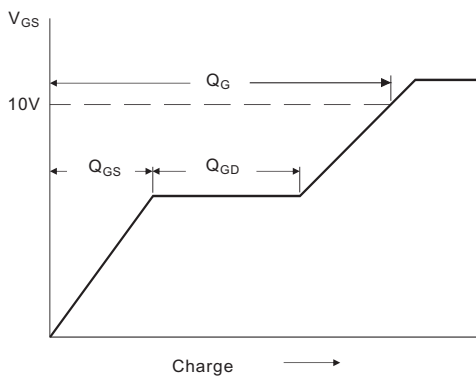
**Fig.12b. Unclamped Inductive waveforms**



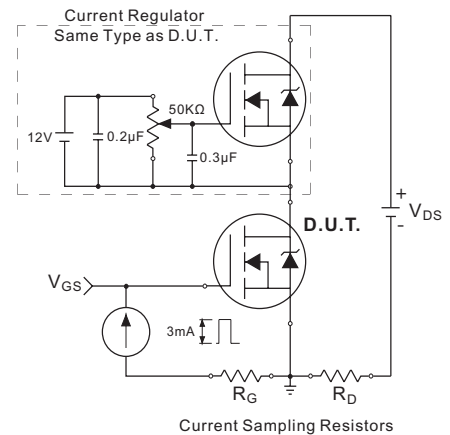
**Fig.12c. Maximum avalanche energy vs. Drain current**



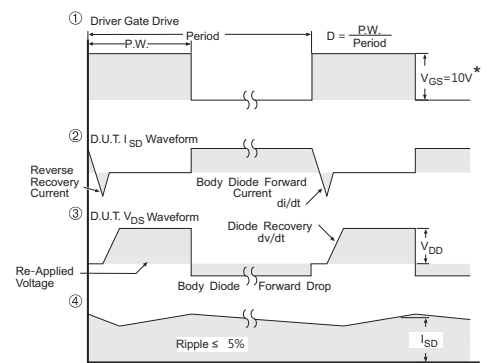
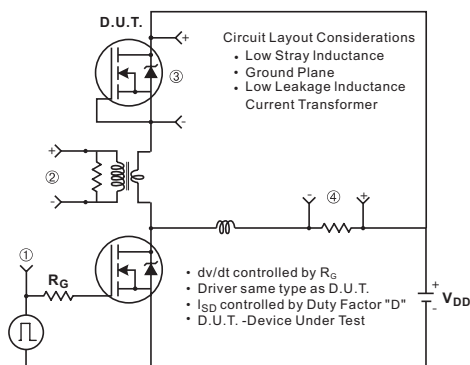
**Fig.13a. Basic gate charge waveform**



**Fig.13b. Gate charge test circuit**

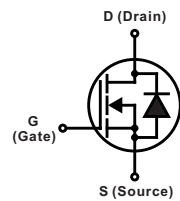
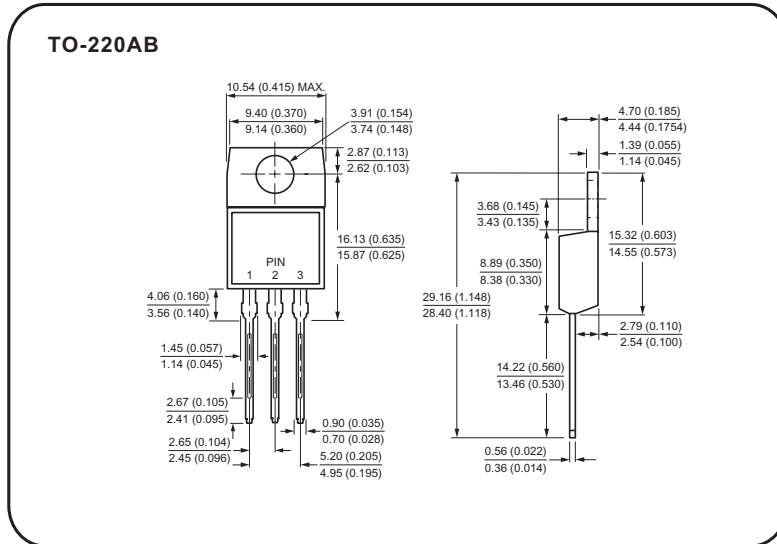


**Fig.14 Peak diode recovery dv/dt test circuit for N-Channel MOSFET**



\* $V_{GS} = 5V$  for Logic Level Devices and  $3V$  for drive devices

## Case Style



All dimensions in millimeters(inches)