

IRF2807SPbF

IRF2807LPbF

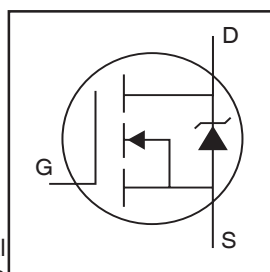
HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications. The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

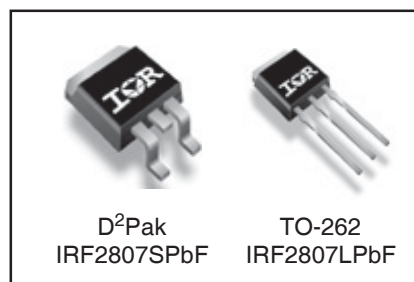
The through-hole version (IRF2807L) is available for low-profile applications.



$$V_{DS} = 75V$$

$$R_{DS(on)} = 13m\Omega$$

$$I_D = 82A \textcircled{7}$$



D²Pak
IRF2807SPbF

TO-262
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Absolute Maximum Ratings

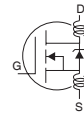
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	82 $\textcircled{7}$	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	58	
I_{DM}	Pulsed Drain Current $\textcircled{1}$	280	
$P_D @ T_C = 25^\circ C$	Power Dissipation	230	W
	Linear Derating Factor	1.5	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current $\textcircled{1}$	43	A
E_{AR}	Repetitive Avalanche Energy $\textcircled{1}$	23	mJ
dv/dt	Peak Diode Recovery dv/dt $\textcircled{3}$	5.9	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	40	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.074	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	13	m Ω	$V_{GS} = 10V, I_D = 43A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	38	—	—	S	$V_{DS} = 50V, I_D = 43A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 75V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 60V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	160	nC	$I_D = 43A$
Q_{gs}	Gate-to-Source Charge	—	—	29		$V_{DS} = 60V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	55		$V_{GS} = 10V$, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = 38V$
t_r	Rise Time	—	64	—		$I_D = 43A$
$t_{d(off)}$	Turn-Off Delay Time	—	49	—		$R_G = 2.5\Omega$
t_f	Fall Time	—	48	—		$V_{GS} = 10V$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3820	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	610	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	130	—		$f = 1.0\text{MHz}$, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy②	—	1280③	340⑥		$I_{AS} = 50A, L = 370\mu H$



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	82⑦	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	—	—	280		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 43A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	100	150	ns	$T_J = 25^\circ\text{C}, I_F = 43A$
Q_{rr}	Reverse Recovery Charge	—	410	610	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 370\mu H$
 $R_G = 25\Omega$, $I_{AS} = 43A$, $V_{GS} = 10V$ (See Figure 12)
- ③ $I_{SD} \leq 43A$, $di/dt \leq 300A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

⑤ This is a typical value at device destruction and represents operation outside rated limits.

⑥ This is a calculated value limited to $T_J = 175^\circ\text{C}$.

⑦ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

**When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

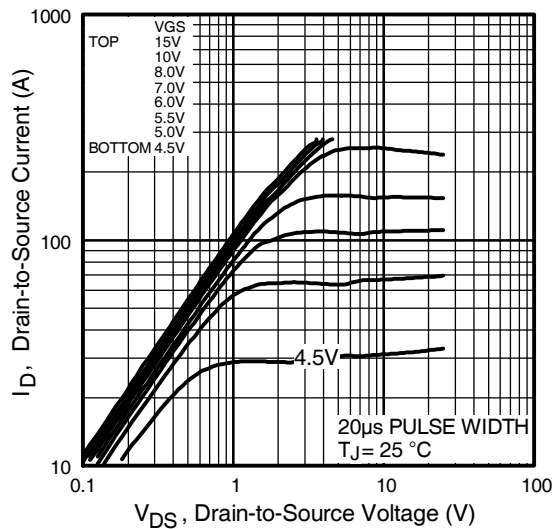


Fig 1. Typical Output Characteristics

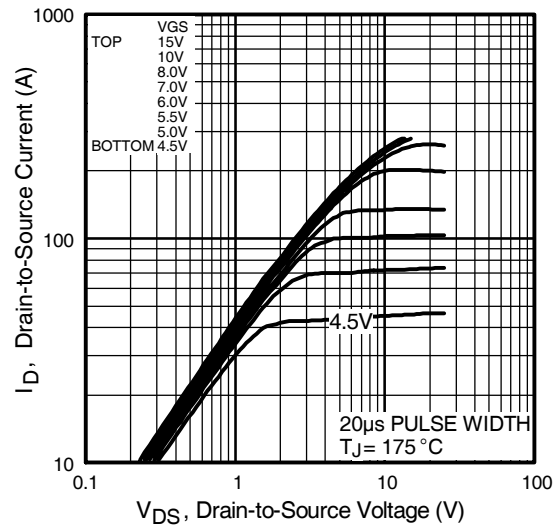


Fig 2. Typical Output Characteristics

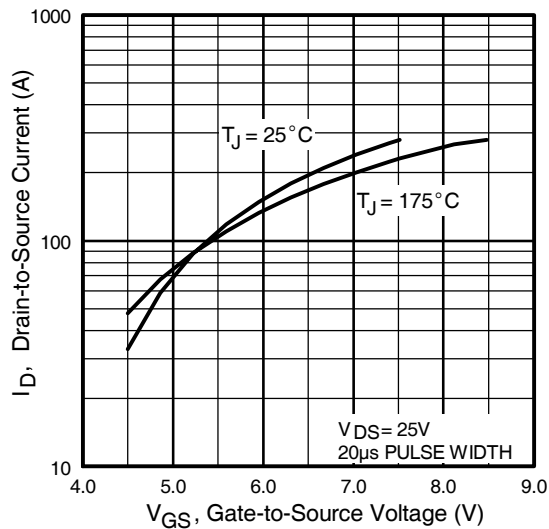


Fig 3. Typical Transfer Characteristics

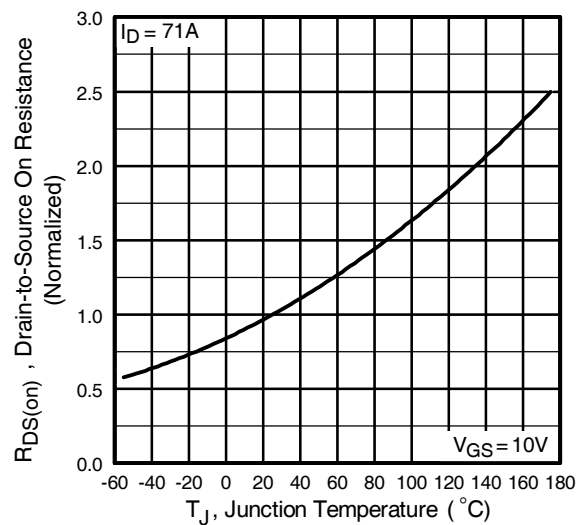


Fig 4. Normalized On-Resistance Vs. Temperature

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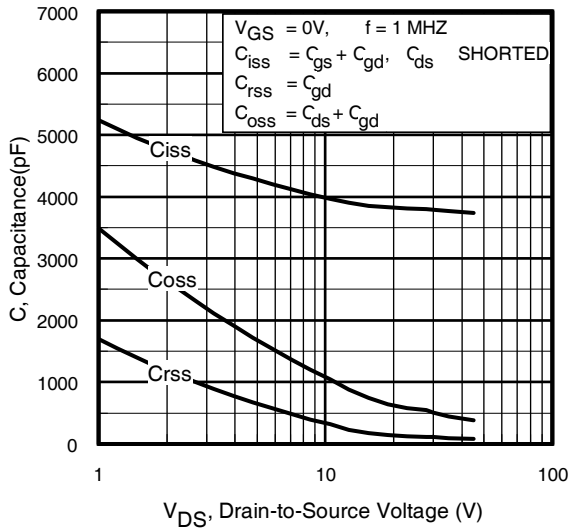


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

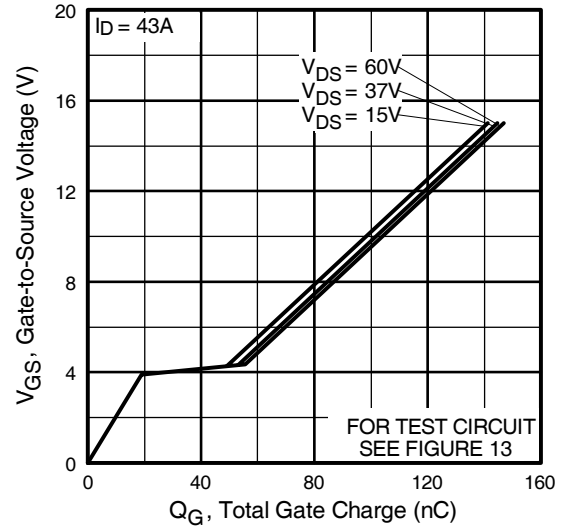


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

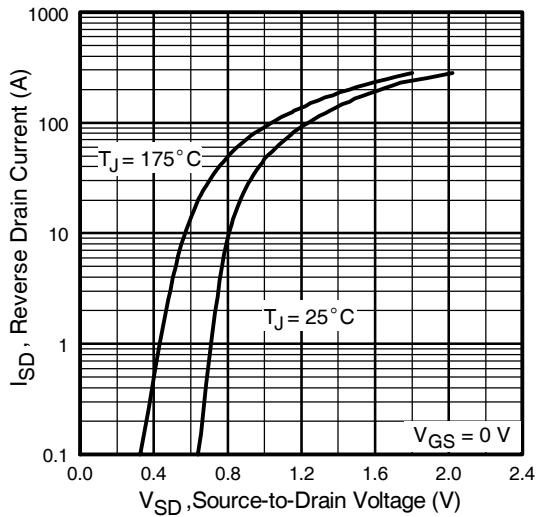


Fig 7. Typical Source-Drain Diode Forward Voltage

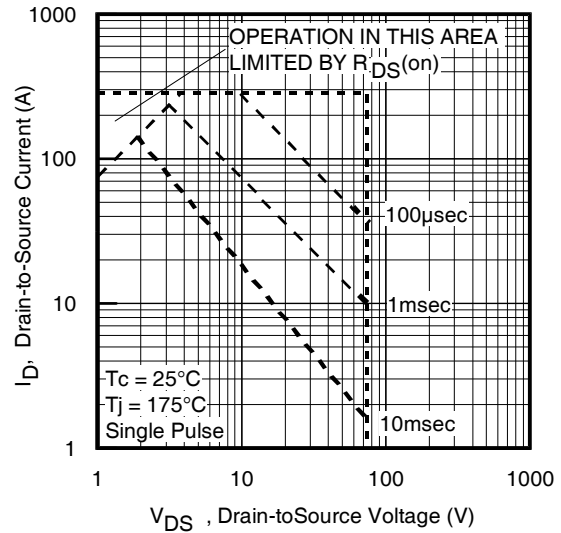


Fig 8. Maximum Safe Operating Area

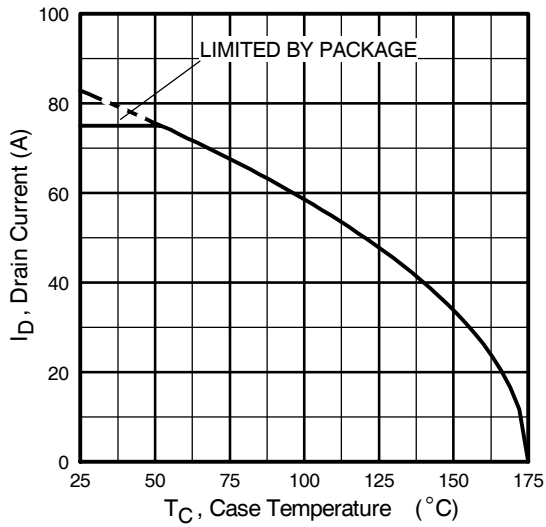


Fig 9. Maximum Drain Current Vs. Case Temperature

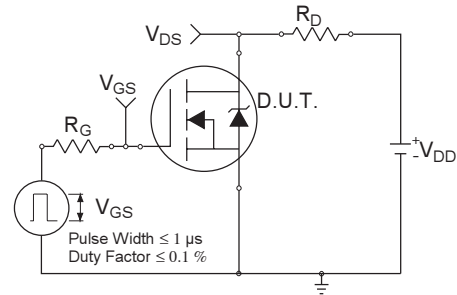


Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

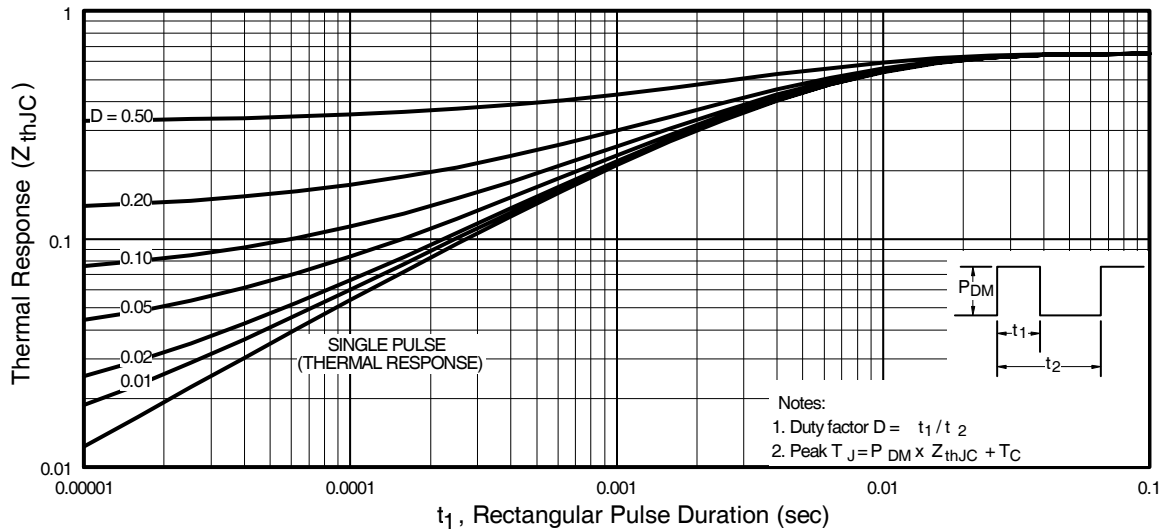


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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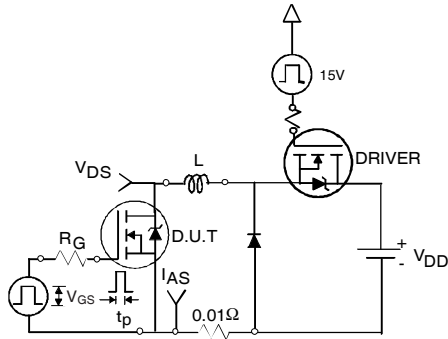


Fig 12a. Unclamped Inductive Test Circuit

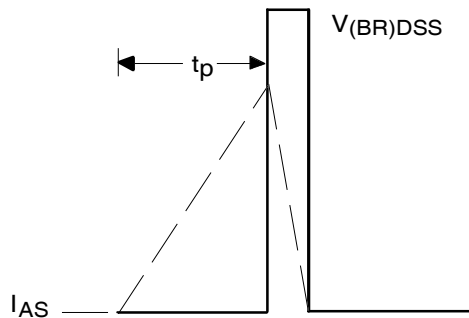


Fig 12b. Unclamped Inductive Waveforms



Fig 13a. Basic Gate Charge Waveform

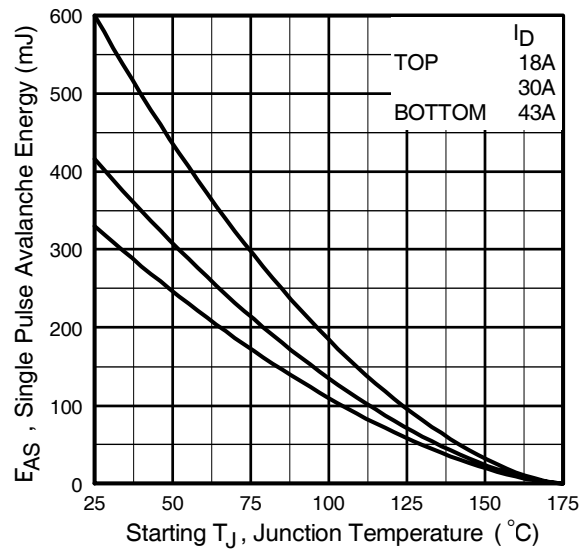


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

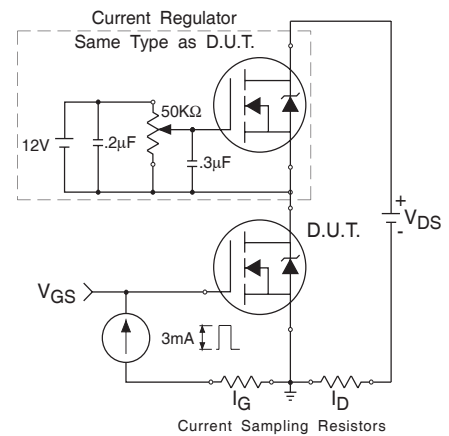
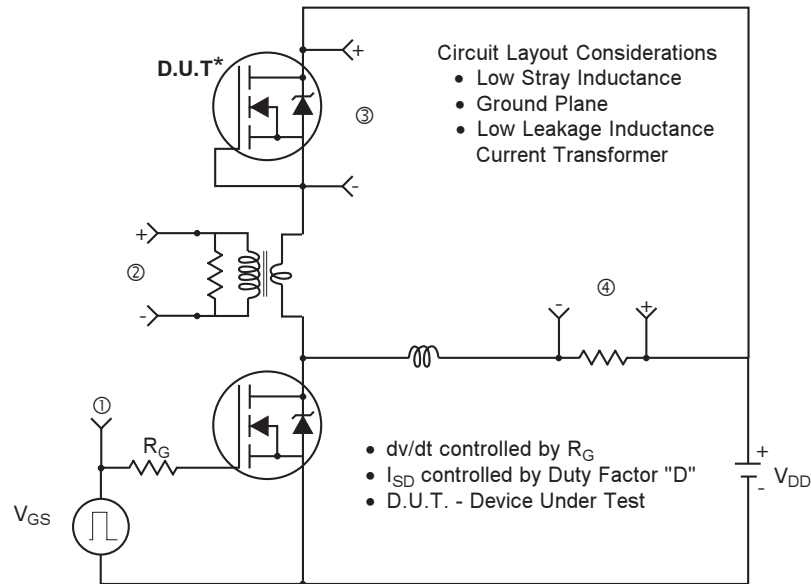
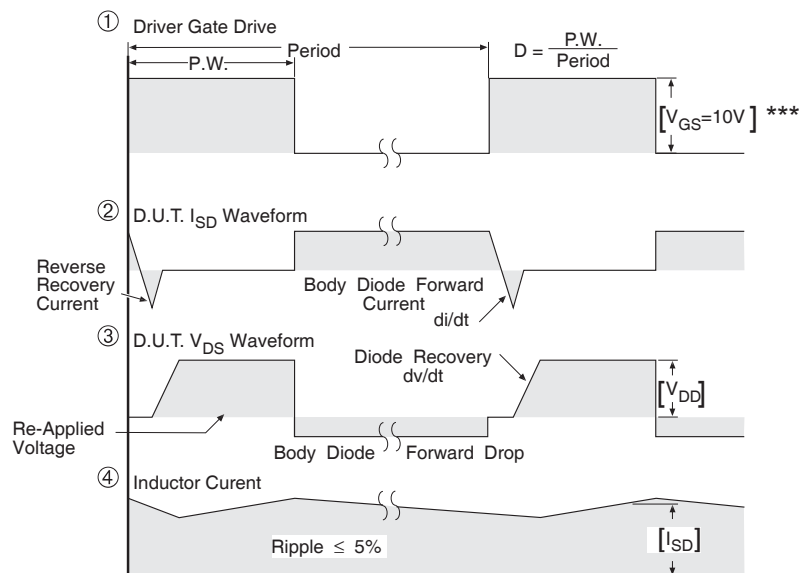


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

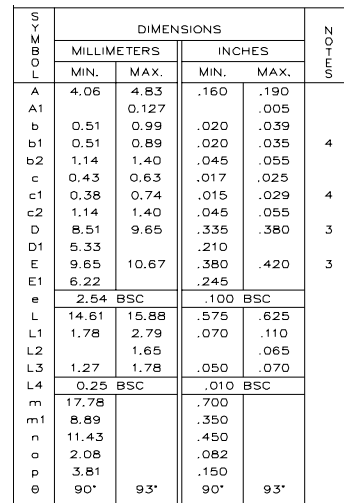


*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

International
IOR Rectifier

Dimensions are shown in millimeters (inches)



<u>HEXFET</u>	<u>IGBTs, CoPACK</u>	<u>DIODES</u>
1.- GATE	1.- GATE	1.- ANODE
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

• PART DEPENDENT.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead-Free"

Diagram illustrating the markings on the F530S MOSFET package:

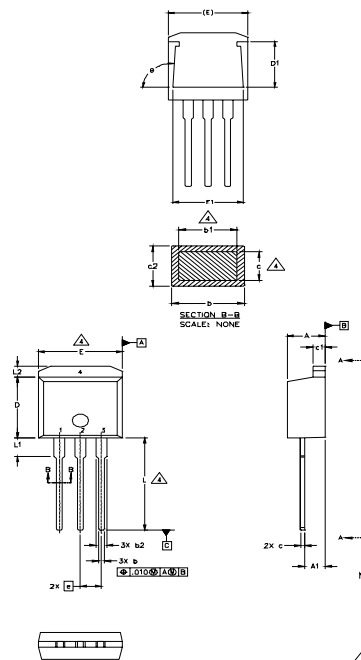
- INTERNATIONAL RECTIFIER LOGO**: Points to the IR logo on the package.
- PART NUMBER**: Points to the F530S marking.
- DATE CODE**: Points to the 002L marking.
 - YEAR 0 = 2000
 - WEEK 02
 - LINE L
- ASSEMBLY LOT CODE**: Points to the 80 and 24 markings.

OR

Diagram illustrating the marking on a component, showing the following codes and their meanings:

- INTERNATIONAL RECTIFIER LOGO**: Points to the logo on the component marking.
- PART NUMBER**: Points to the text **F 530S** on the component marking.
- DATE CODE**: Points to the text **P002A** on the component marking.
- ASSEMBLY LOT CODE**: Points to the text **80** and **24** on the component marking.
- P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)**
- YEAR 0 = 2000**
- WEEK 02**
- A = ASSEMBLY SITE CODE**

TO-262 Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET	IGBT
1. - GATE	1 - GATE
2. - DRAIN	2 - COLLECTOR
3. - SOURCE	3 - EMITTER
4. - DRAIN	

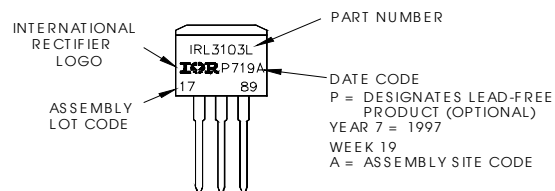
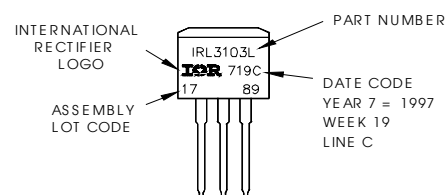
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 4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 5. CONTROLLING DIMENSION: INCH.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"

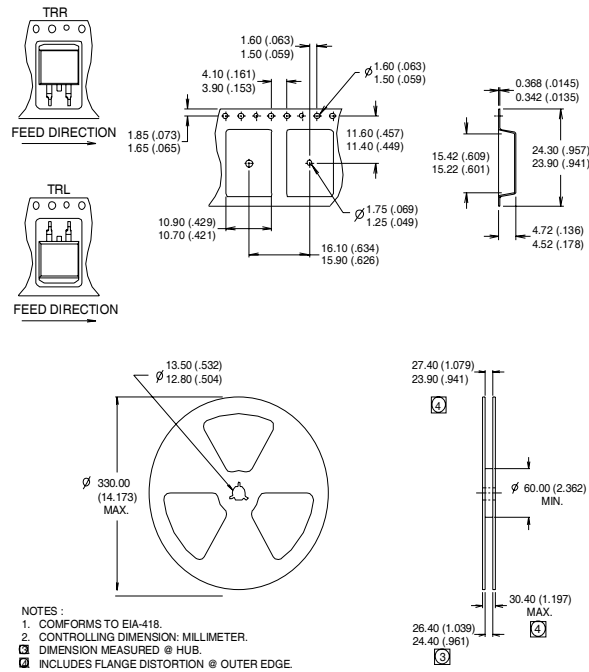
OR



IRF2807S/LPbF

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D²Pak Tape & Reel Information



Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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TAC Fax: (310) 252-7903

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