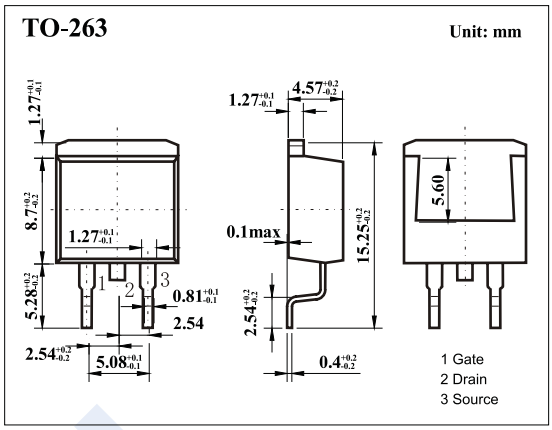
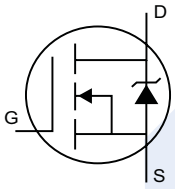
N-Channel MOSFET

IRF3808S (KRF3808S)

■ Features

- V_{DSS} = 75V
- $R_{DS(ON)}$ = 0.007Ω
- I_D = 106A ⑥
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax





■ Absolute Maximum Ratings Ta = 25℃

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	75	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current, V_{GS} @ 10V	Tc=25℃	I_D	106 ⑥	A
	Tc=100℃		75 ⑥	
Pulsed Drain Current ①		I_{DM}	550	
Power Dissipation	Tc=25℃	P_D	200	W
Single Pulse Avalanche Energy ②		E_{AS}	430	mJ
Avalanche Current ①		I_{AR}	82	A
Repetitive Avalanche Energy ⑦		E_{AR}	See Fig.12a, 12b, 15, 16	mJ
Peak Diode Recovery dv/dt ③		dv/dt	5.5	V/ns
Thermal Resistance Junction-to-Case		R_{thJC}	0.75	℃/W
Thermal Resistance.Junction- to-Ambient (PCB Mounted, Steady State) **		R_{thJA}	40	
Junction Temperature		T_J	175	℃
Storage Temperature Range		T_{stg}	-55 to 175	

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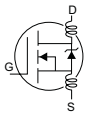
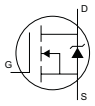
■ Electrical Characteristics @ T_J = 25℃(unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	I_D = 250 μA, V_{GS} = 0 V	75			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 75 V, V_{GS} = 0 V			20	μA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 150 ℃			250	
Gate-Body Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±200	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = 10 V , I_D = 250 μA	2.0		4.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 82 A			7.0	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 25 V, I_D = 82 A	100			S
Total Gate Charge	Q_g	I_D = 82 A V_{DS} = 60 V V_{GS} = 10 V ④		150	220	nC
Gate Source Charge	Q_{gs}			31	47	
Gate Drain Charge	Q_{gd}			50	76	
Turn-On DelayTime	$t_{d(on)}$	V_{DD} = 38 V I_D = 82 A R_G = 2.5 Ω V_{GS} = 10 V ④		16		ns
Turn-On Rise Time	t_r			140		
Turn-Off DelayTime	$t_{d(off)}$			68		
Turn-Off Fall Time	t_f			120		
Internal Drain Inductance	L_D	Between lead, 6mm (0.25in.) from package and center of die contact 		4.5		nH
Internal Source Inductance	L_S			7.5		
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1.0 MHz. See Fig. 5		5310		pF
Output Capacitance	C_{oss}			890		
Reverse Transfer Capacitance	C_{rss}			130		
Output Capacitance	C_{oss}	V_{GS} = 0 V, V_{DS} = 1.0 V, f = 1.0 MHz		6010		
Output Capacitance	C_{oss}	V_{GS} = 0 V, V_{DS} = 60 V, f = 1.0 MHz		570		
Effective Output Capacitance ⑤	$C_{oss\ eff.}$	V_{GS} = 0 V, V_{DS} = 0V to 60V		1140		
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 ℃, I_F = 82 A di/dt = 100 A/μs ④			140	ns
Body Diode Reverse Recovery Charge	Q_{rr}				510	nC
Maximum Body-Diode Continuous Current	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 			106	A
Body-Diode Pulsed Source Current ①	I_{SM}				550	
Diode Forward Voltage	V_{SD}	T_J = 25 ℃, I_S = 82A, V_{GS} = 0V ④			1.3	V
Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)					

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.130mH, R_G = 25Ω , I_{AS} = 82A. (See Figure 12).

③ I_{SD} ≤ 82A, di/dt ≤ 310A/μs, V_{DD} ≤ $V_{(BR)DSS}$,T_J ≤ 175°C

④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

** When mounted on 1" square PCB (FR-4 or G-10 Material).

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■ Typical Characterisitics

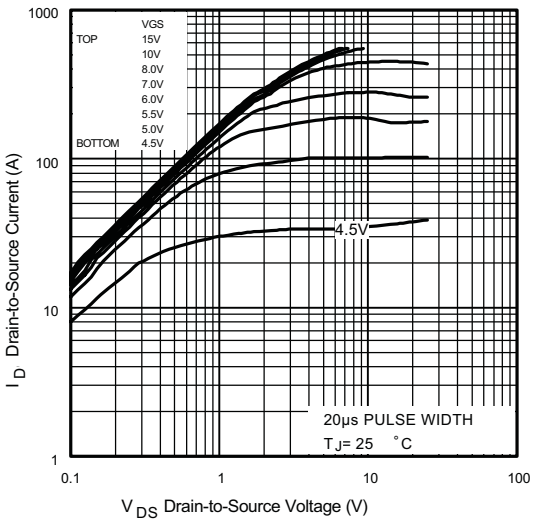

Fig 1. Typical Output Characteristics

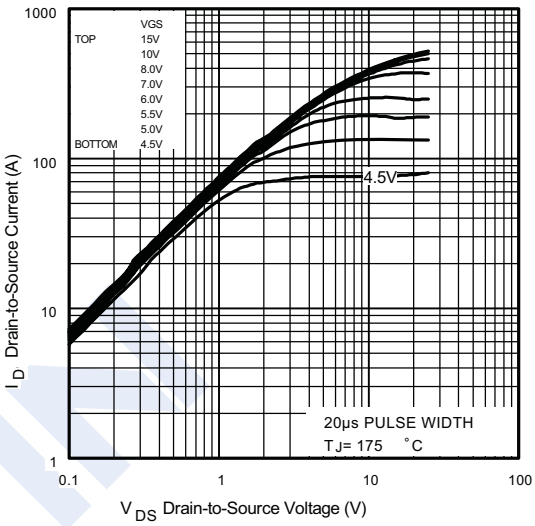

Fig 2. Typical Output Characteristics

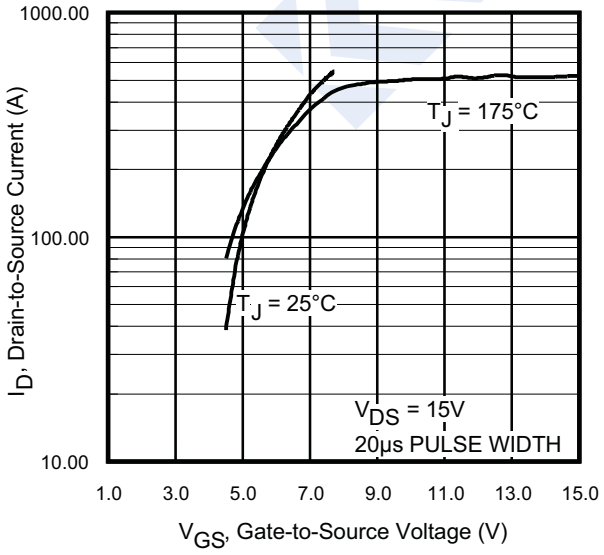

Fig 3. Typical Transfer Characteristics

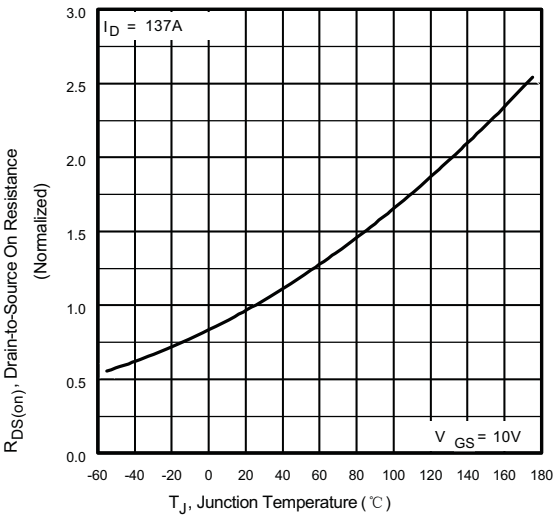

Fig 4. Normalized On-Resistance Vs. Temperature

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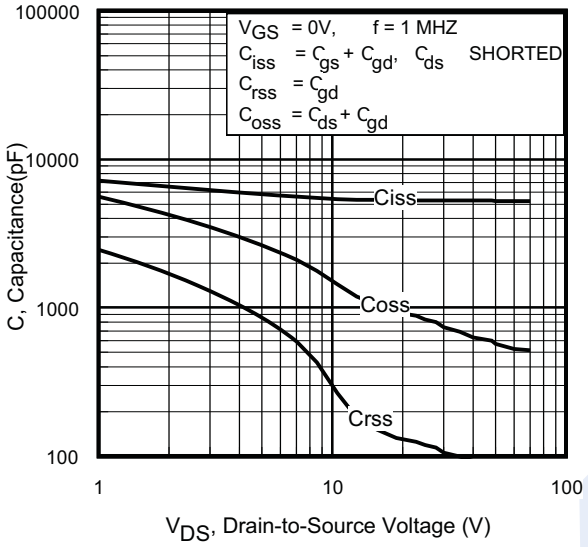

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

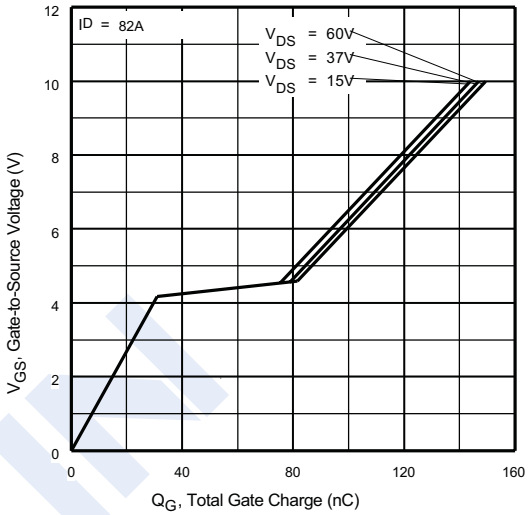

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

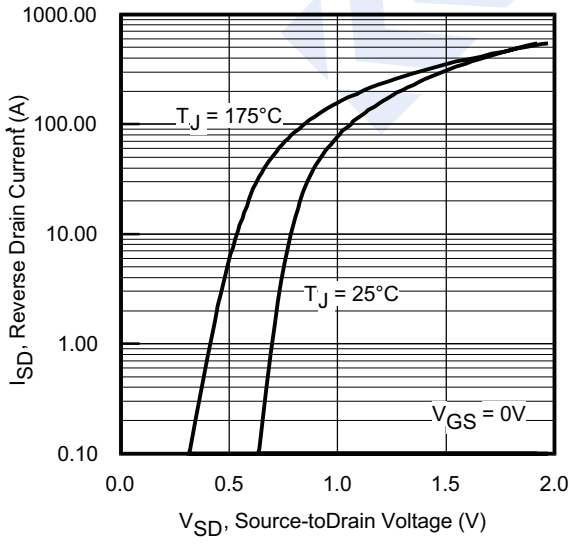

Fig 7. Typical Source-Drain Diode Forward Voltage

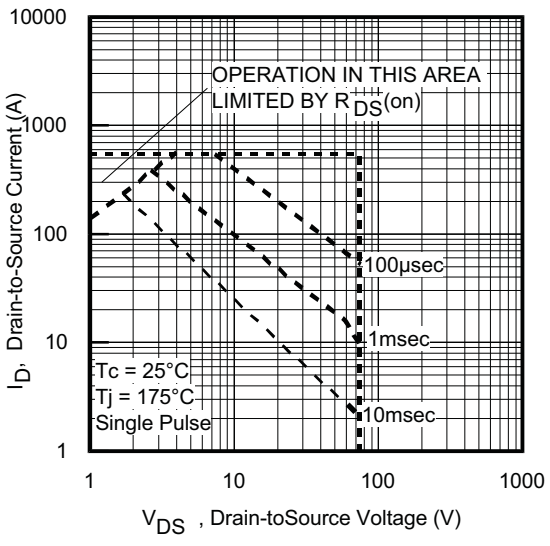

Fig 8. Maximum Safe Operating Area

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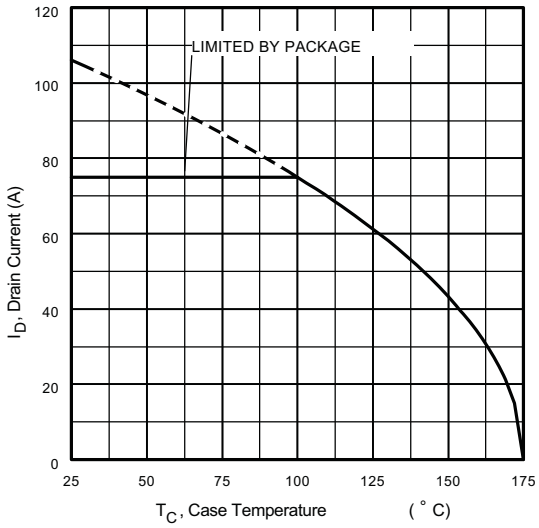

Fig 9. Maximum Drain Current Vs. Case Temperature

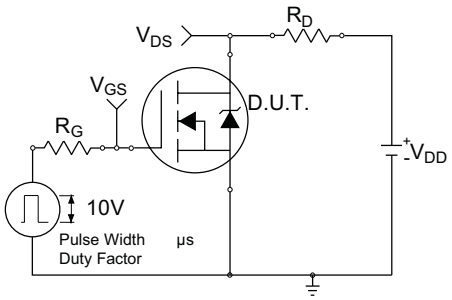

Fig 10a. Switching Time Test Circuit

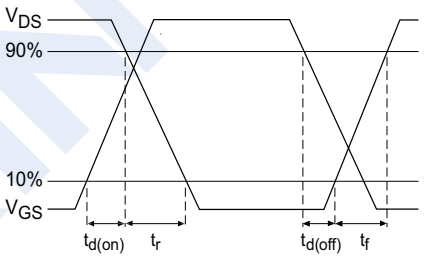

Fig 10b. Switching Time Waveforms

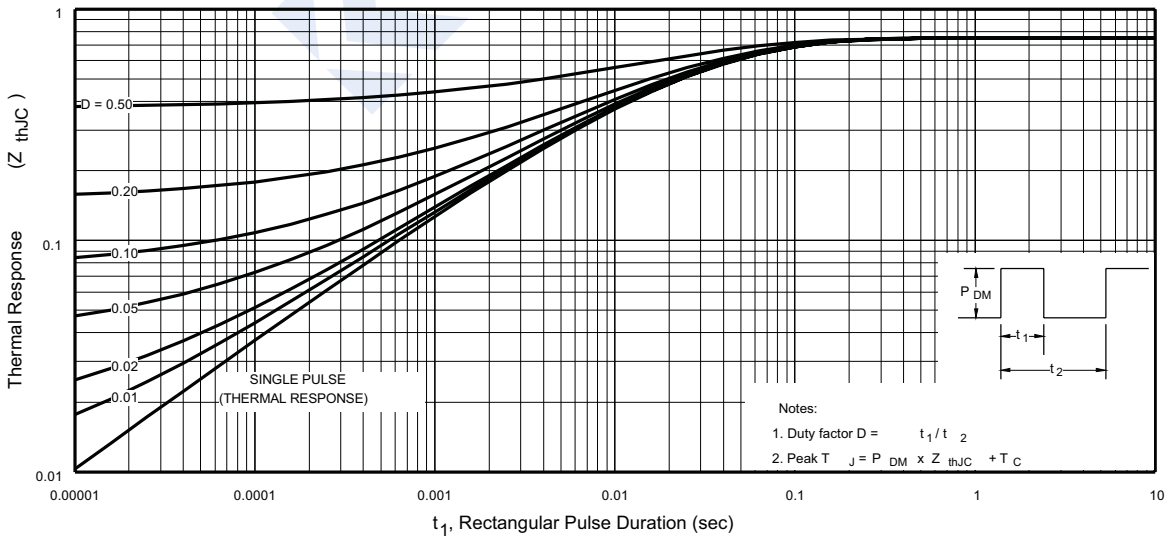

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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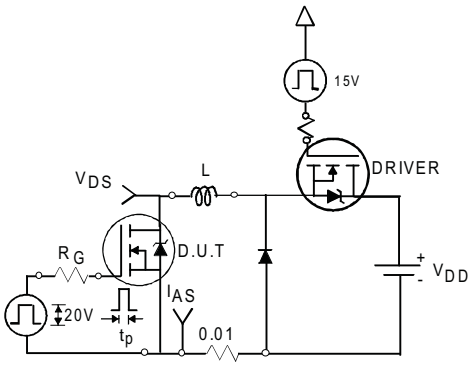

Fig 12a. Unclamped Inductive Test Circuit

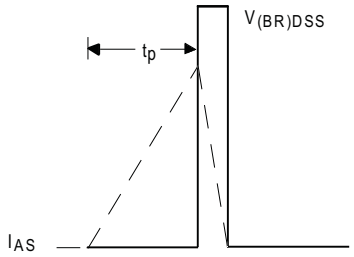

Fig 12b. Unclamped Inductive Waveforms

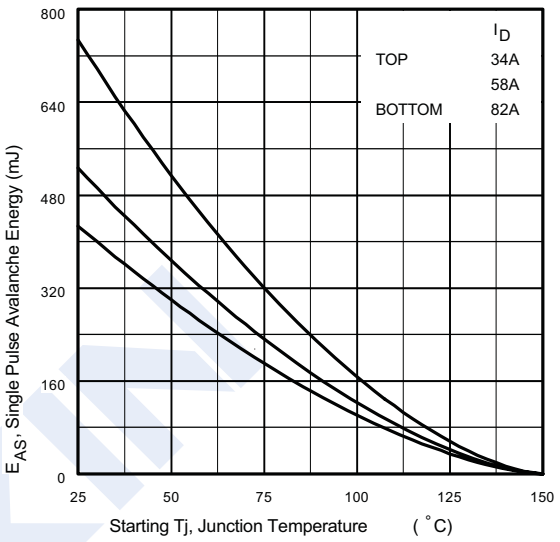

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

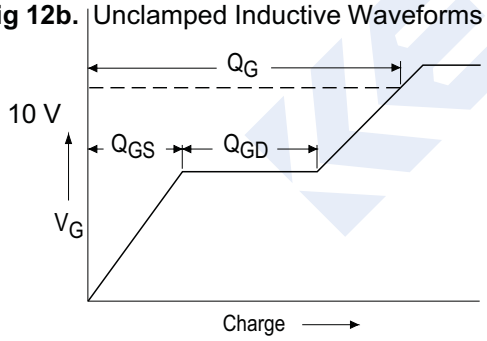

Fig 13a. Basic Gate Charge Waveform

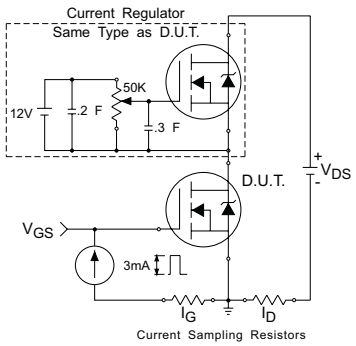

Fig 13b. Gate Charge Test Circuit

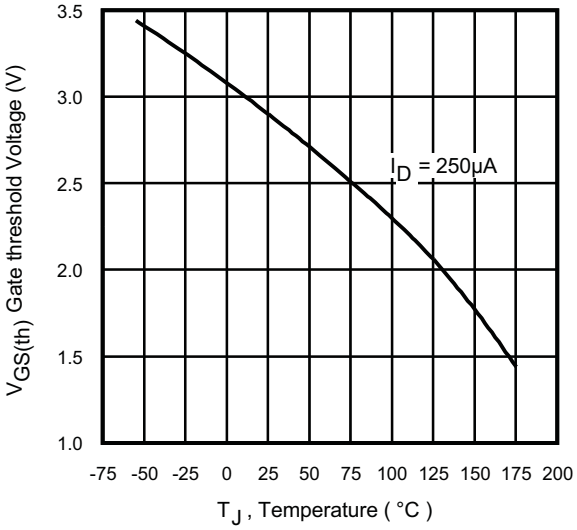

Fig 14. Threshold Voltage Vs. Temperature

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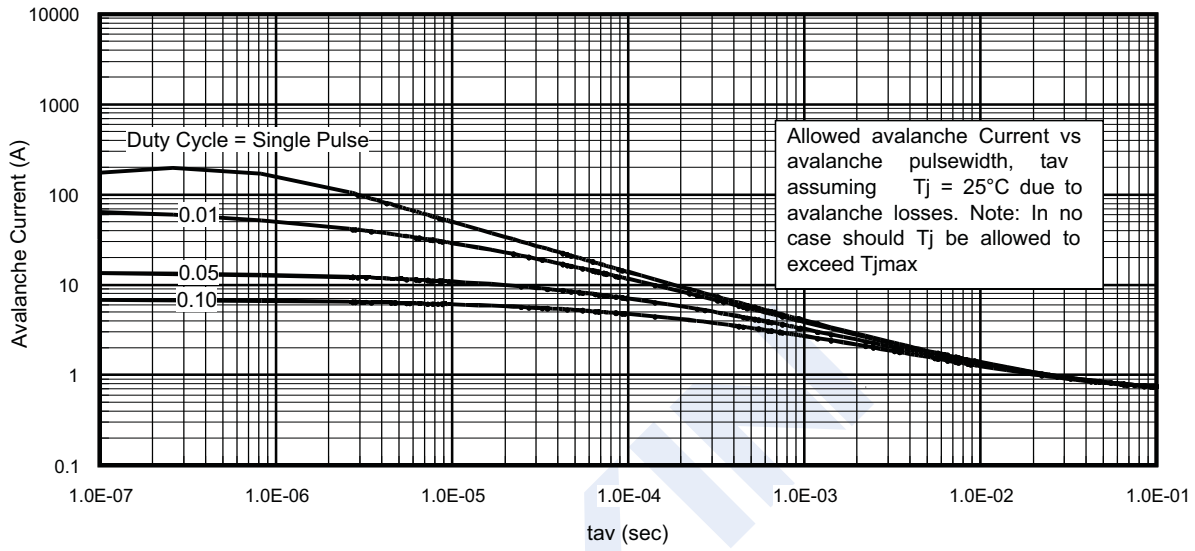

Fig 15. Typical Avalanche Current Vs.Pulsewidth

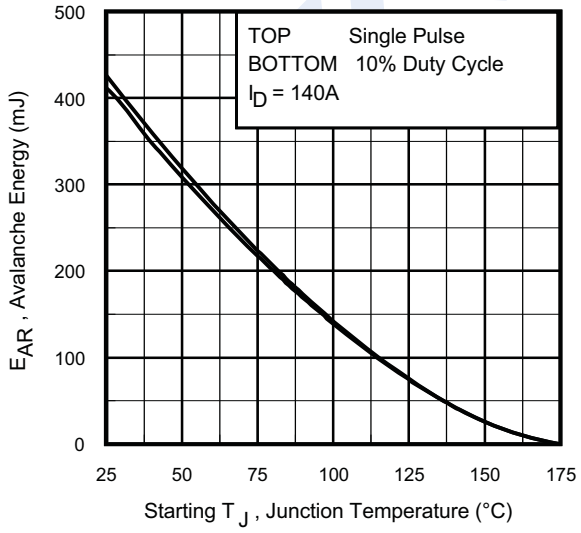

Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. T = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = T/Z_{thJC}$$
$$I_{av} = 2\ T/[1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

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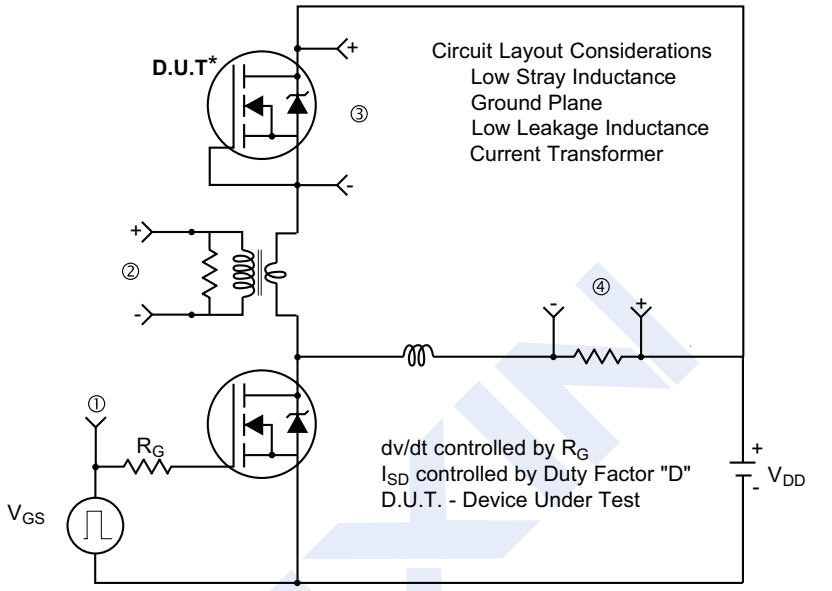
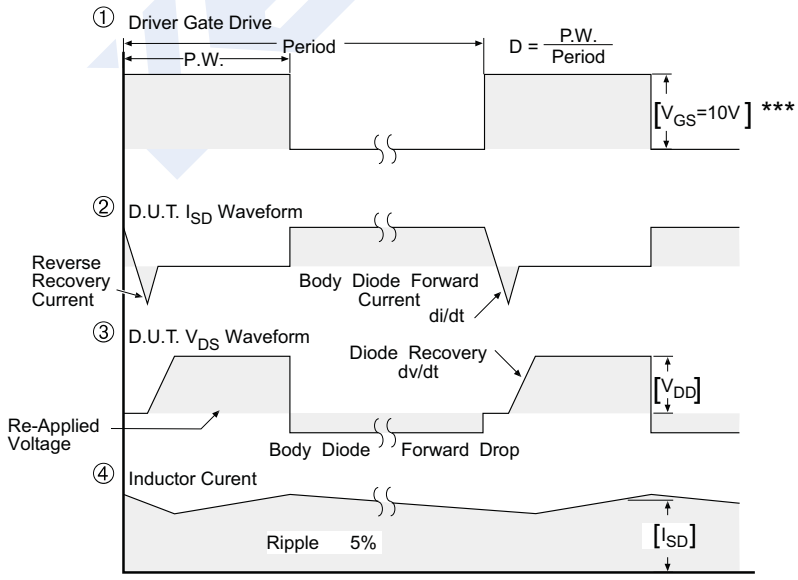
Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 17. For N-channel power MOSFETs