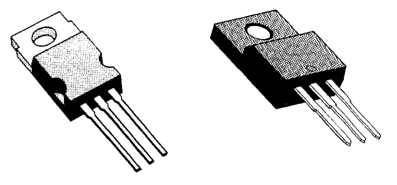
SGS-THOMSON MICROELECTRONICS

IRF 540/FI-541/FI IRF 542/FI-543/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF540	100 V	0.077 Ω	28 A
IRF540FI	100 V	0.077 Ω	15 A
IRF541	80 V	0.077 Ω	28 A
IRF541FI	80 V	0.077 Ω	15 A
IRF542	100 V	0.100 Ω	25 A
IRF542FI	100 V	0.100 Ω	14 A
IRF543	80 V	0.100 Ω	25 A
IRF543FI	80 V	0.100 Ω	14 A



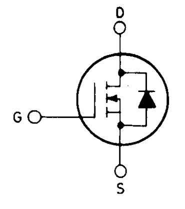
TO-220 ISOWATT220

- 80-100 VOLTS - FOR DC/DC CONVERTERS
- HIGH CURRENT
- ULTRA FAST SWITCHING
- EASY DRIVE- FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:
- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC/DC converters, UPS, battery chargers, secondary regulators, servo control, power-audio amplifiers and robotics.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	TO-220 ISOWATT220	IRF 540 540FI	541 541FI	542 542FI	543 543FI	
V_{DS} *	Drain-source voltage ($V_{GS}=0$)	100	80	100	80	V
V_{DGR} *	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	80	100	80	V
V_{GS}	Gate-source voltage	±20				V
I_{DM} (•)	Drain current (pulsed)	110	110	100	100	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)	110	110	100	100	A
		540	**541**	**542**	**543**	
I_D	Drain current (cont.) at T_c = 25°C	28	28	25	25	A
I_D	Drain current (cont.) at T_c = 100°C	20	20	17	17	A
		540FI	**541FI**	**542FI**	**543FI**	
I_D ■	Drain current (cont.) at T_c = 25°C	15	15	14	14	A
I_D ■	Drain current (cont.) at T_c = 100°C	9	9	8	8	A
		TO-220		**ISOWATT220**		
P_{tot} ■	Total dissipation at T_c < 25°C	125		40		W
■	Derating factor	1		0.32		W/°C
T_{stg}	Storage temperature	−55 to 150				°C
T_j	Max. operating junction temperature	150				°C

* T_j = 25°C to 125°C
(•) Repetitive Rating: Pulse width limited by max junction temperature.
■ See note on ISOWATT220 on this datasheet.

June 1988

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj-case}$	Thermal resistance junction-case	max	1	3.12	°C/W
R_{thc-s}	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25°C$ unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit

OFF

$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF540/542/540FI/542FI** for **IRF541/543/541FI/543FI**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	V_{GS} = ±20 V			±500	nA

ON **

$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ V_{GS} = 10 V for **IRF540/541/540FI/541FI** for **IRF542/543/542FI/543FI**	 28 25			 A A
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 17 A for **IRF540/541/540FI/541FI** for **IRF542/543/542FI/543FI**			 0.077 0.100	 Ω Ω

DYNAMIC

g_{fs} **	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ I_D = 17 A	8.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			1600 800 300	pF pF pF

SWITCHING

$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V I_D = 15 A R_i = 4.7 Ω (see test circuit)			30 60 80 30	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 28 A V_{DS} = Max Rating × 0.8 (see test circuit)			59	nC

ELECTRICAL CHARACTERISTICS (Continued)

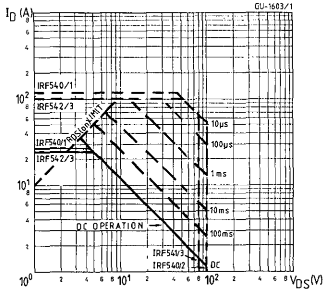
Parameters		Test Conditions		Min.	Typ.	Max.	Unit

SOURCE DRAIN DIODE

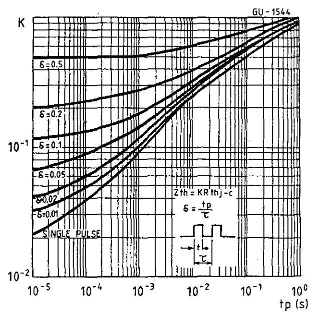
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)					28 110	A A
V_{SD}**	Forward on voltage	I_{SD} = 28 A	V_{GS} = 0			2.5	V
t_{rr}	Reverse recovery time	T_j = 150°C			500		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 28 A	di/dt = 100 A/μs		2.9		μC

** Pulsed: Pulse duration ⩽ 300 μs, duty cycle ⩽ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

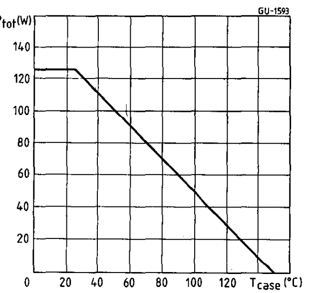
Safe operating areas (standard package)



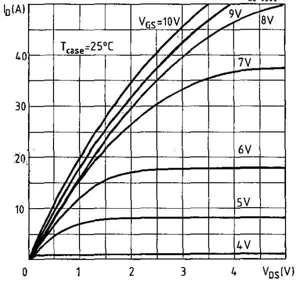
Thermal impedance (standard package)



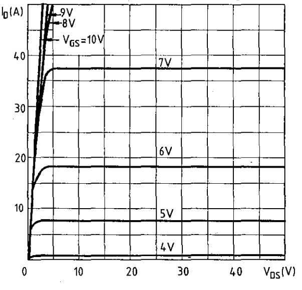
Derating curve (standard package)



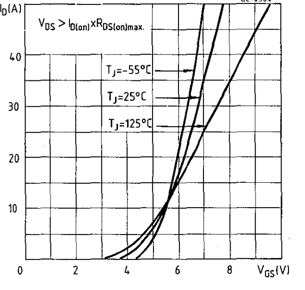
Output characteristics



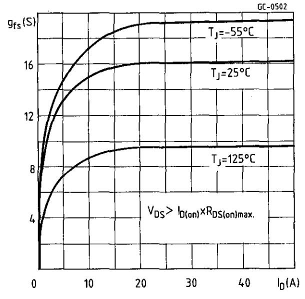
Output characteristics



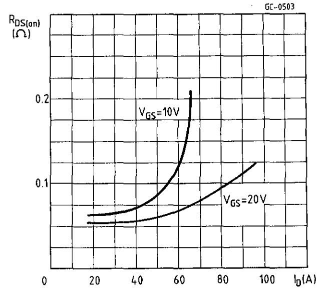
Transfer characteristics



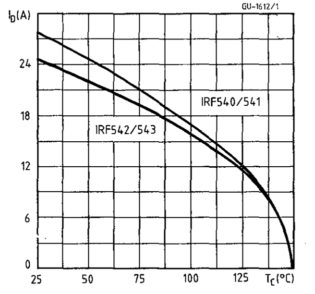
Transconductance



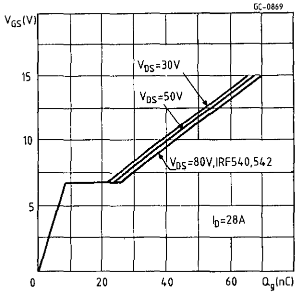
Static drain-source on resistance



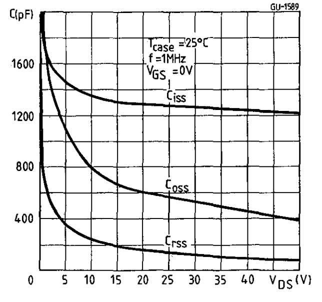
Maximum drain current vs temperature



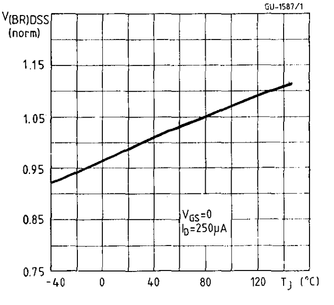
Gate charge vs gate-source voltage



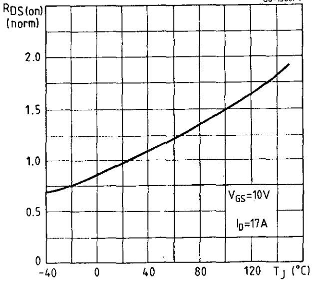
Capacitance variation



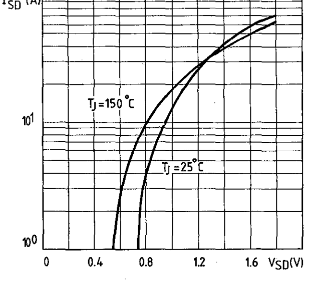
Normalized breakdown voltage vs temperature



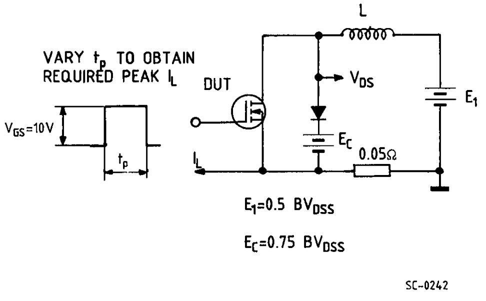
Normalized on resistance vs temperature



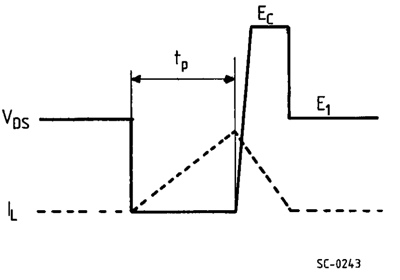
Source-drain diode forward characteristics



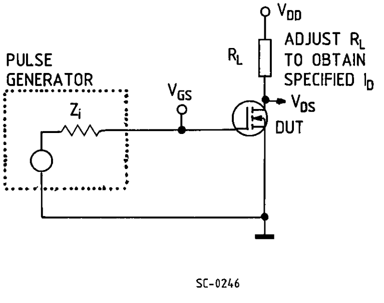
Clamped inductive test circuit



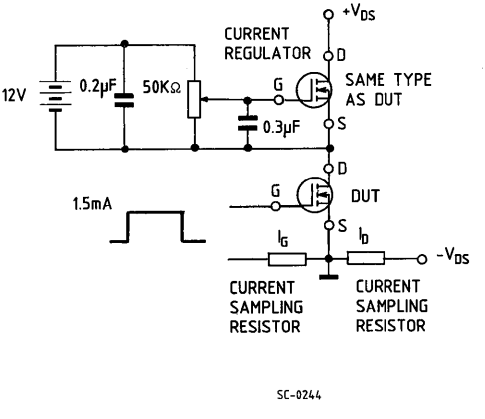
Clamped inductive waveforms



Switching times test circuit



Gate charge test circuit



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)}\ (\text{at } 150°C)}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

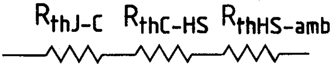
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

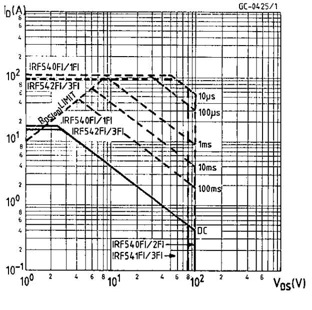
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

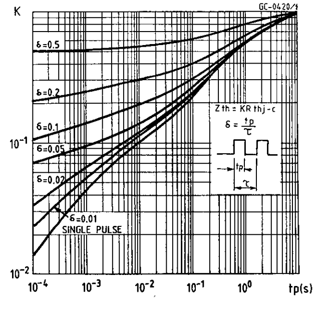


ISOWATT DATA

Safe operating areas



Thermal impedance



Derating curve