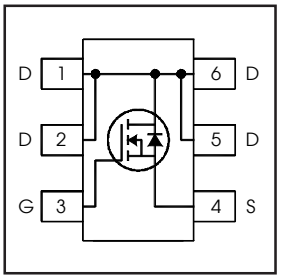
International
IOR Rectifier

IRF5801PbF-1

HEXFET® Power MOSFET

V_{DS}	200	V
$R_{DS(on)\ max}$ ($@V_{GS}$ = 10V)	2.20	Ω
$Q_{g\ (typical)}$	3.9	nC
I_D ($@T_A$ = 25°C)	0.6	A



Features		Benefits
Industry-standard pinout TSOP-6 Package	⇒	Multi-Vendor Compatibility
Compatible with Existing Surface Mount Techniques		Easier Manufacturing
RoHS Compliant, Halogen-Free		Environmentally Friendlier
MSL1, Industrial qualification		Increased Reliability

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF5801TRPbF-1	TSOP-6	Tape and Reel	3000	IRF5801TRPbF-1

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	0.6	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	0.48	
I_{DM}	Pulsed Drain Current ①	4.8	
P_D @T_A = 25°C	Power Dissipation	2.0	W
	Linear Derating Factor	0.016	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ⑥	9.6	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ④	—	62.5	°C/W

Notes ① through ⑥ are on page 8

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/°C	Reference to 25°C, I_D = 1mA ③
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	2.2	Ω	V_{GS} = 10V, I_D = 0.36A ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 200V, V_{GS} = 0V
		—	—	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

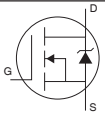
	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	0.44	—	—	S	V_{DS} = 50V, I_D = 0.36A
Q_g	Total Gate Charge	—	3.9	—	nC	I_D = 0.36A
Q_{gs}	Gate-to-Source Charge	—	0.8	—		V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	2.2	—		V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	—	6.5	—	ns	V_{DD} = 100V
t_r	Rise Time	—	8.0	—		I_D = 0.36A
$t_{d(off)}$	Turn-Off Delay Time	—	8.8	—		R_G = 53Ω
t_f	Fall Time	—	19	—		V_{GS} = 10V ③
C_{iss}	Input Capacitance	—	88	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	18	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	6.3	—		f = 1.0MHz
C_{oss}	Output Capacitance	—	102	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	8.4	—		V_{GS} = 0V, V_{DS} = 160V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	26	—		V_{GS} = 0V, V_{DS} = 0V to 160V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	9.9	mJ
I_{AR}	Avalanche Current①	—	0.6	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	1.8	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	4.8		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 0.36A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	45	—	ns	T_J = 25°C, I_F = 0.36A
Q_{rr}	Reverse RecoveryCharge	—	54	—	nC	di/dt = 100A/µs ③



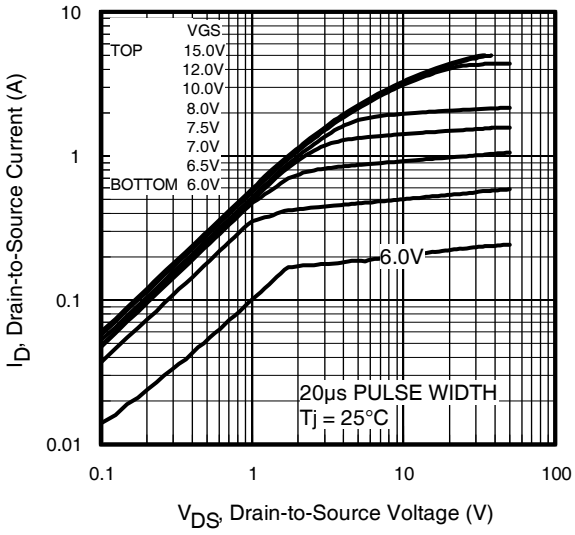


Fig 1. Typical Output Characteristics

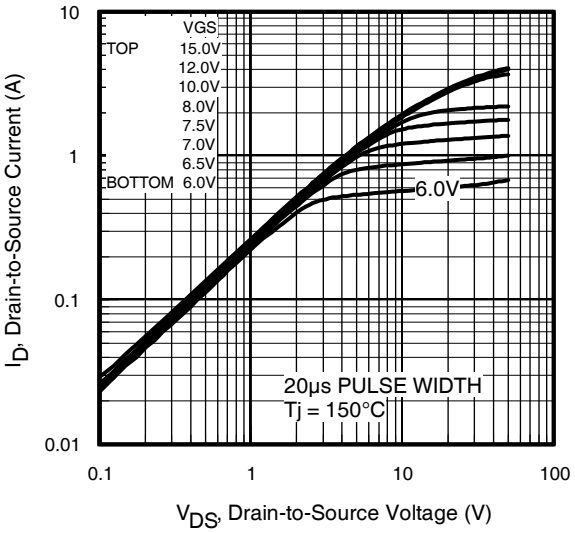


Fig 2. Typical Output Characteristics

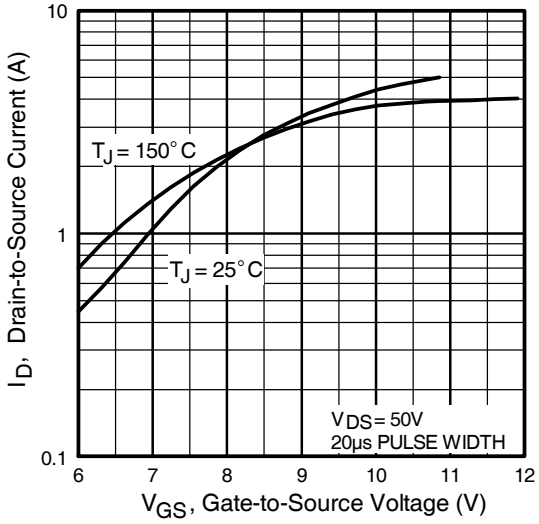


Fig 3. Typical Transfer Characteristics

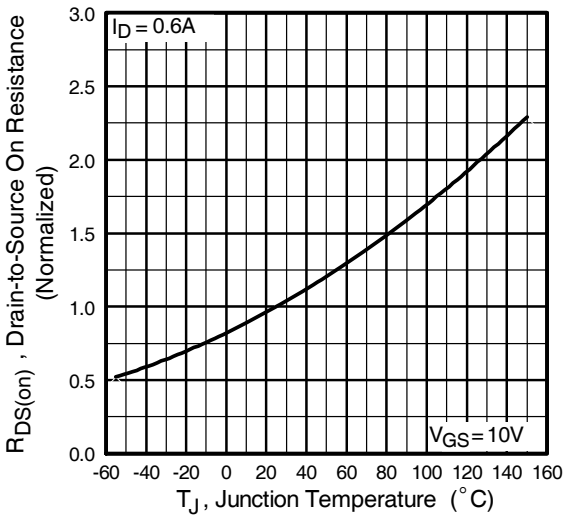


Fig 4. Normalized On-Resistance Vs. Temperature

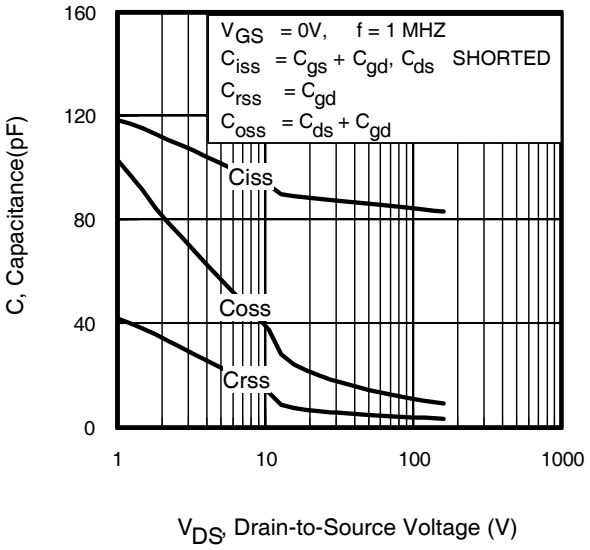


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

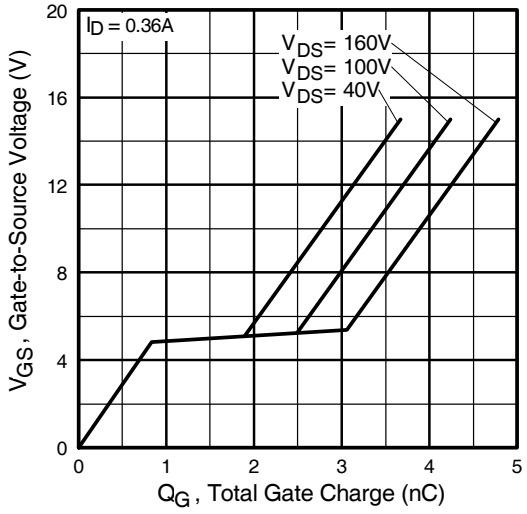


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

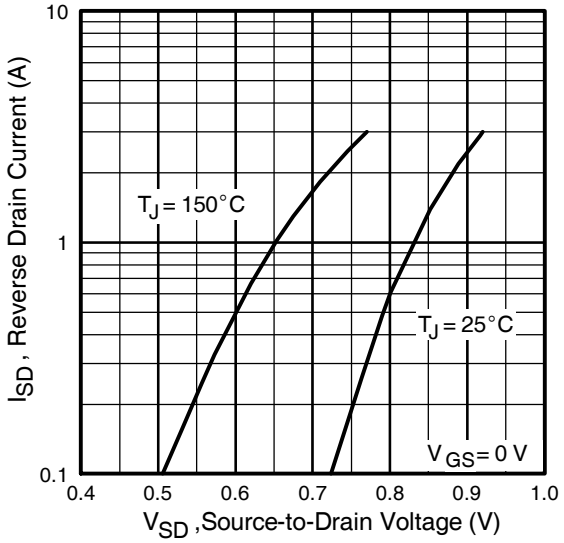


Fig 7. Typical Source-Drain Diode Forward Voltage

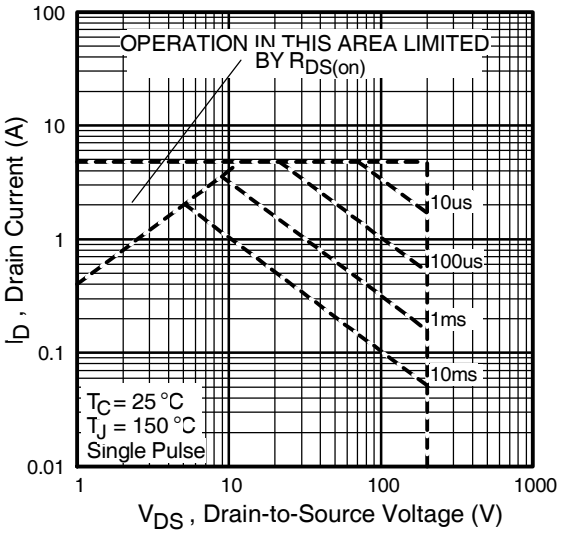


Fig 8. Maximum Safe Operating Area

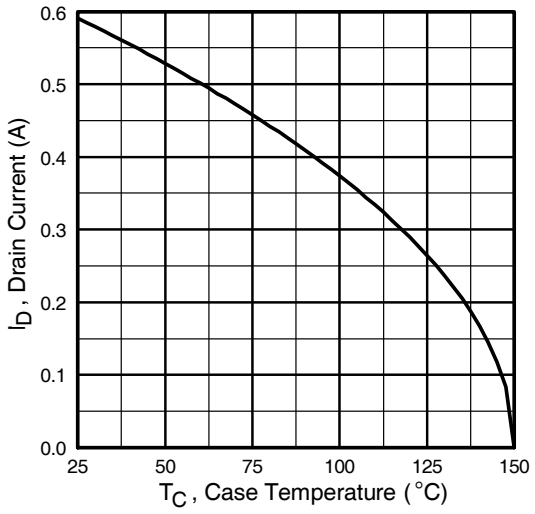


Fig 9. Maximum Drain Current Vs. Case Temperature

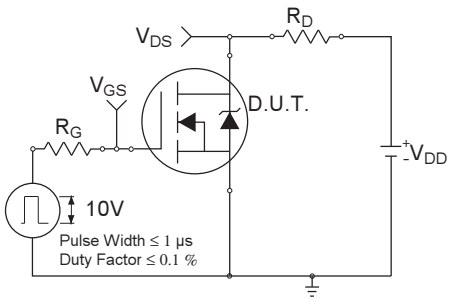


Fig 10a. Switching Time Test Circuit

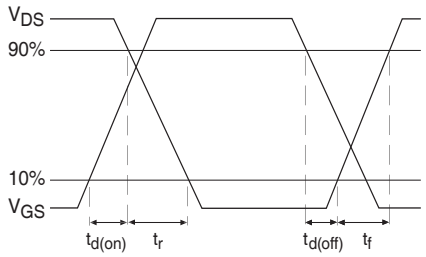


Fig 10b. Switching Time Waveforms

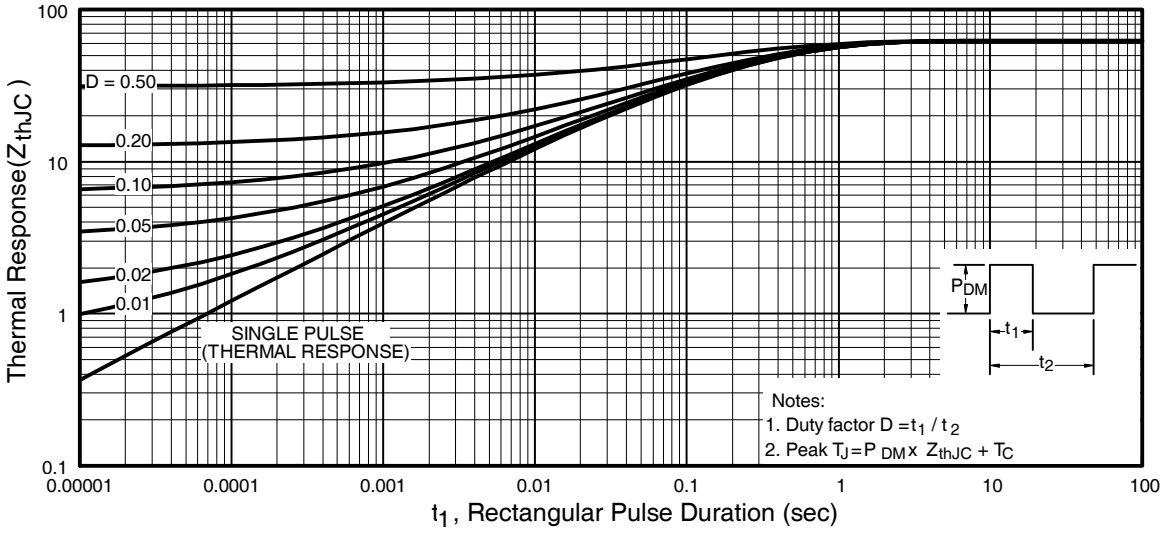


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

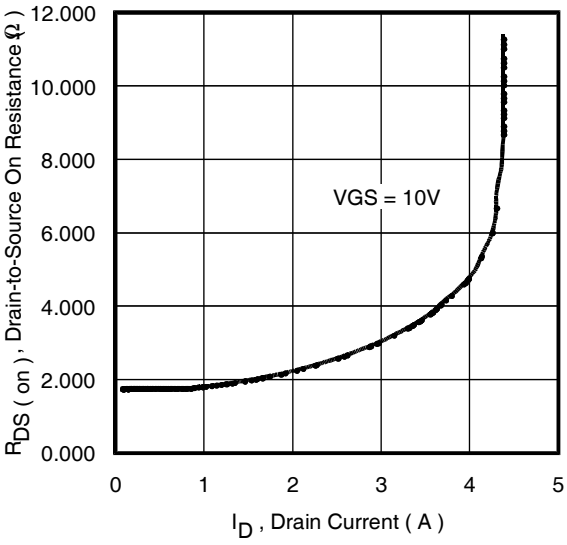


Fig 12. On-Resistance Vs. Drain Current

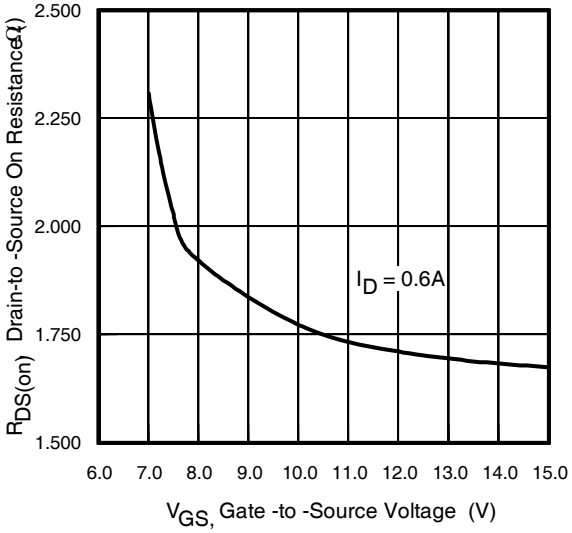


Fig 13. On-Resistance Vs. Gate Voltage

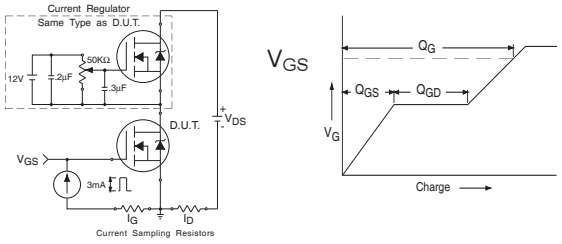


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

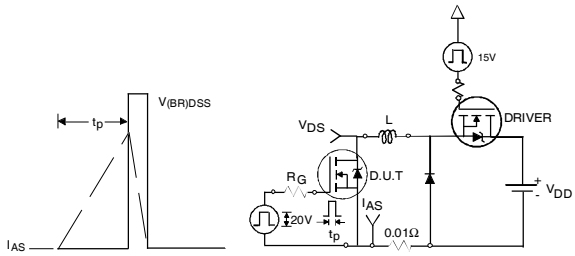


Fig 15a&b. Unclamped Inductive Test circuit and Waveforms

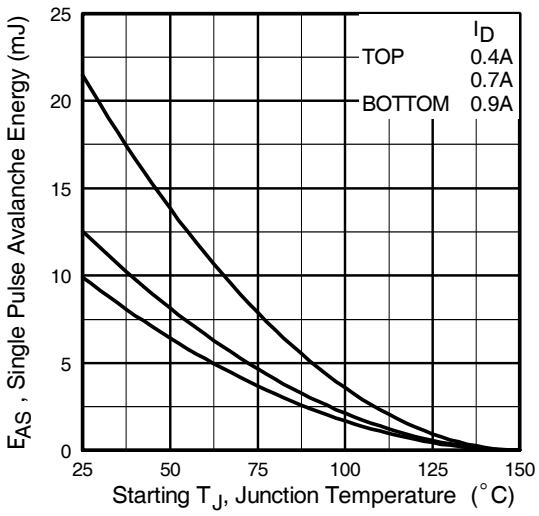
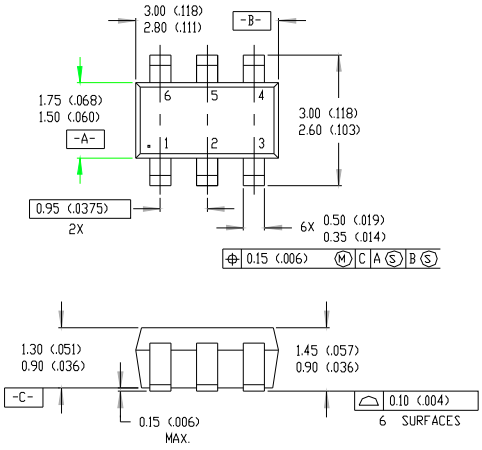
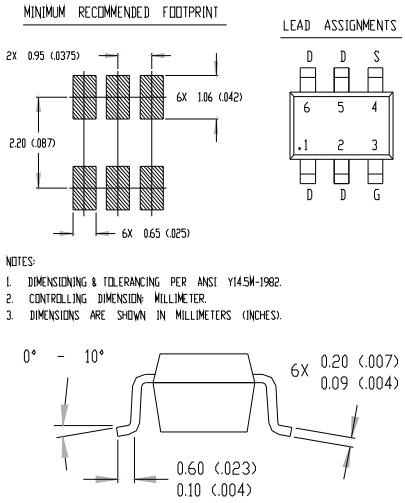


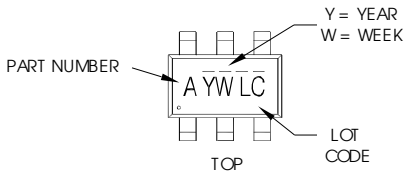
Fig 15c. Maximum Avalanche Energy Vs. Drain Current

TSOP-6 Package Outline





TSOP-6 Part Marking Information



PART NUMBER CODE REFERENCE:

A = SI3443DV	O = IRLTS6342TRPBF
B = IRF5800	P = IRFTS8342TRPBF
C = IRF5850	R = IRFTS9342TRPBF
D = IRF5851	S = Not applicable
E = IRF5852	T = IRLTS2242TRPBF
F = IRF5801	
G = IRF5803	
H = IRF5804	
I = IRF5805	
J = IRF5806	
K = IRF5810	
N = IRF5802	

Note: A line above the work week
(as shown here) indicates Lead-Free.

DATE CODE MARKING INSTRUCTIONS

WW = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

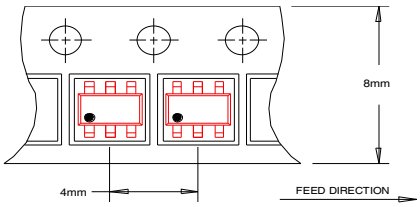
YEAR		Y	WORK WEEK	W
2011	2001	1	01	A
2012	2002	2	02	B
2013	2003	3	03	C
2014	2004	4	04	D
2015	2005	5		
2016	2006	6		
2017	2007	7		
2018	2008	8		
2019	2009	9		
2020	2010	0	24	X
			25	Y
			26	Z

WW = (27-52) IF PRECEDED BY A LETTER

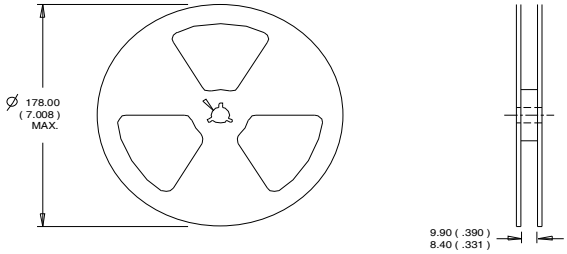
YEAR		Y	WORK WEEK	W
2011	2001	A	27	A
2012	2002	B	28	B
2013	2003	C	29	C
2014	2004	D	30	D
2015	2005	E		
2016	2006	F		
2017	2007	G		
2018	2008	H		
2019	2009	J		
2020	2010	K	50	X
			51	Y
			52	Z

Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

TSOP-6 Tape & Reel Information



NOTES :
1. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 27mH, R_G = 25Ω, I_{AS} = 0.36A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ When mounted on 1 inch square copper board, t < 10sec.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ I_{SD} ≤ 0.36A, di/dt ≤ 93A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C.

Qualification information†

Qualification level	Industrial (per JEDEC JESD47F†† guidelines)	
Moisture Sensitivity Level	TSOP-6	MSL1 (per JEDEC J-STD-020D††)
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability

†† Applicable version of JEDEC standard at the time of product release

International
IOR Rectifier
IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA
To contact International Rectifier, please visit http://www.irf.com/whoto-call/