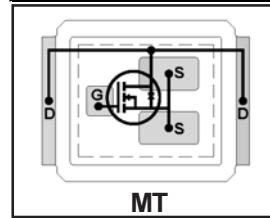


**IRF6609**  
HEXFET® Power MOSFET

- Low Conduction Losses
- Low Switching Losses
- Ideal Synchronous Rectifier MOSFET
- Low Profile (<0.7 mm)
- Dual Sided Cooling Compatible
- Compatible with existing Surface Mount Techniques

$V_{DS}$	$R_{DS(on)}$ max	Qg
20V	2.0mΩ @ $V_{GS} = 10V$	46nC
	2.6mΩ @ $V_{GS} = 4.5V$	



Applicable DirectFET Outline and Substrate Outline (see p.8,9 for details)

SQ	SX	ST		MQ	MX	<b>MT</b>			
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**Description**

The IRF6609 combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of an SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, IMPROVING previous best thermal resistance by 80%.

The IRF6609 balances both low resistance and low charge along with ultra low package inductance to reduce both conduction and switching losses. The reduced total losses make this product ideal for high efficiency DC-DC converters that power the latest generation of processors operating at higher frequencies. The IRF6609 has been optimized for parameters that are critical in synchronous buck operating from 12 volt buss converters including Rds(on), gate charge and Cdv/dt-induced turn on immunity. The IRF6609 offers particularly low Rds(on) and high Cdv/dt immunity for synchronous FET applications.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	20	V
$V_{GS}$	Gate-to-Source Voltage	±20	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	150	A
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	31	
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	25	
$I_{DM}$	Pulsed Drain Current ①	250	
$P_D @ T_A = 25^\circ C$	Power Dissipation ②	2.8	W
$P_D @ T_A = 70^\circ C$	Power Dissipation ②	1.8	
$P_D @ T_C = 25^\circ C$	Power Dissipation	89	
	Linear Derating Factor	0.022	W/°C
$T_J$	Operating Junction and	-40 to + 150	°C
$T_{STG}$	Storage Temperature Range		

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ④⑤	—	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑤⑥	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑥⑦	20	—	
$R_{\theta JC}$	Junction-to-Case ⑦⑧	—	1.4	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	—	

Notes ① through ⑧ are on page 10

## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

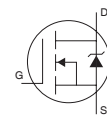
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	20	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	15	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	1.6	2.0	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 31A ③
		—	2.0	2.6		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 25A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.55	—	2.45	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-6.1	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
		—	—	150		V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	91	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 25A
Q <sub>g</sub>	Total Gate Charge	—	46	69	nC	V <sub>DS</sub> = 10V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 17A See Fig. 17
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	15	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	4.7	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	15	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	11	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	20	—		
Q <sub>oss</sub>	Output Charge	—	26	—	nC	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V
t <sub>d(on)</sub>	Turn-On Delay Time	—	24	—	ns	V <sub>DD</sub> = 16V, V <sub>GS</sub> = 4.5V ③ I <sub>D</sub> = 25A Clamped Inductive Load
t <sub>r</sub>	Rise Time	—	95	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	26	—		
t <sub>f</sub>	Fall Time	—	9.8	—		
C <sub>iss</sub>	Input Capacitance	—	6290	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 10V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	1850	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	860	—		

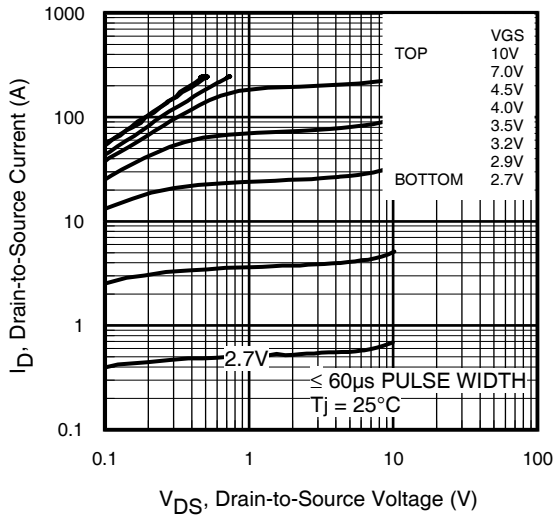
## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>②</sup>	—	230	mJ
I <sub>AR</sub>	Avalanche Current ①	—	25	A

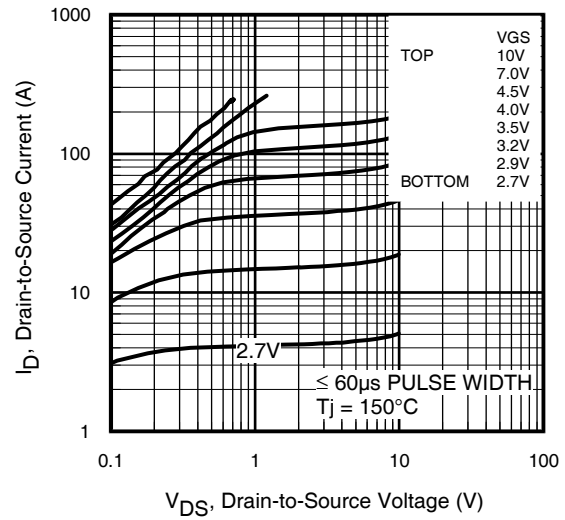
## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	31	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	250		
V <sub>SD</sub>	Diode Forward Voltage	—	0.80	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 25A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	32	48	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 25A
Q <sub>rr</sub>	Reverse Recovery Charge	—	26	39	nC	di/dt = 100A/μs ③

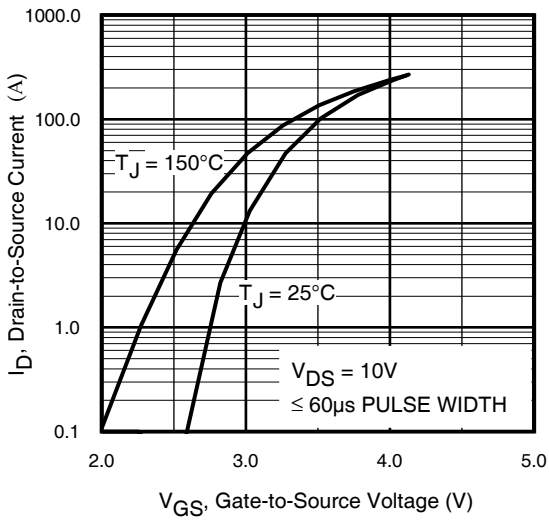




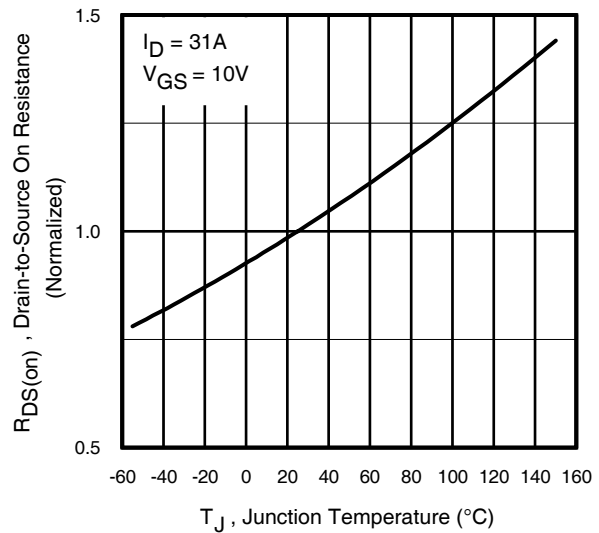
**Fig 1.** Typical Output Characteristics



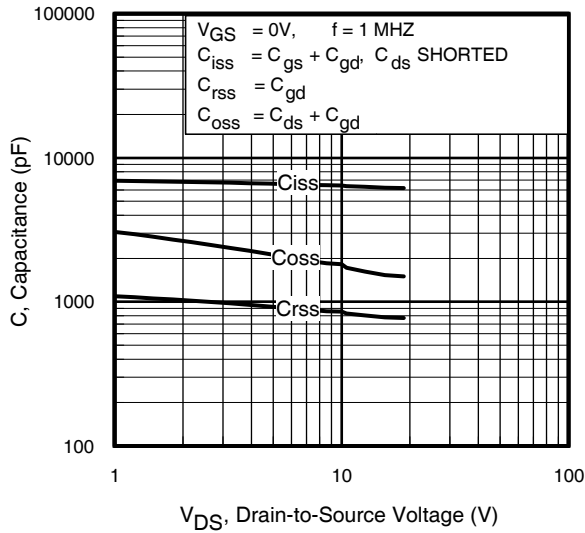
**Fig 2.** Typical Output Characteristics



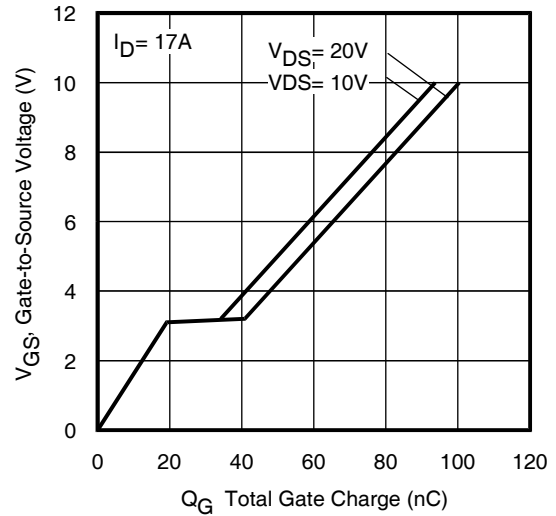
**Fig 3.** Typical Transfer Characteristics



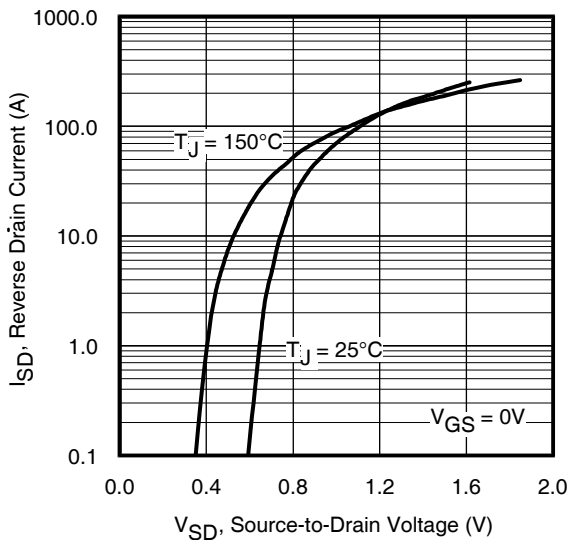
**Fig 4.** Normalized On-Resistance vs. Temperature



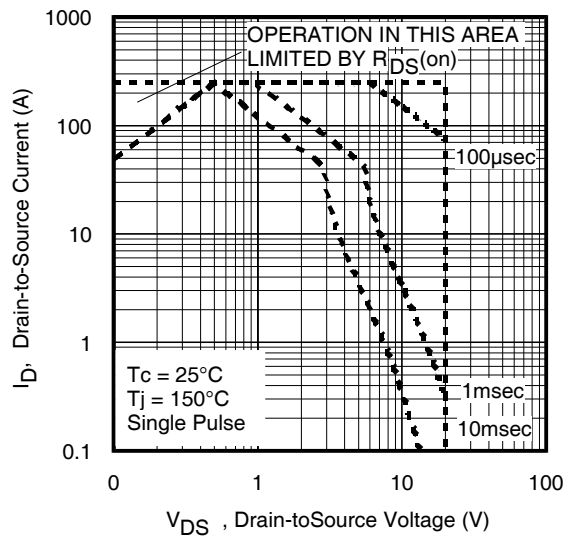
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



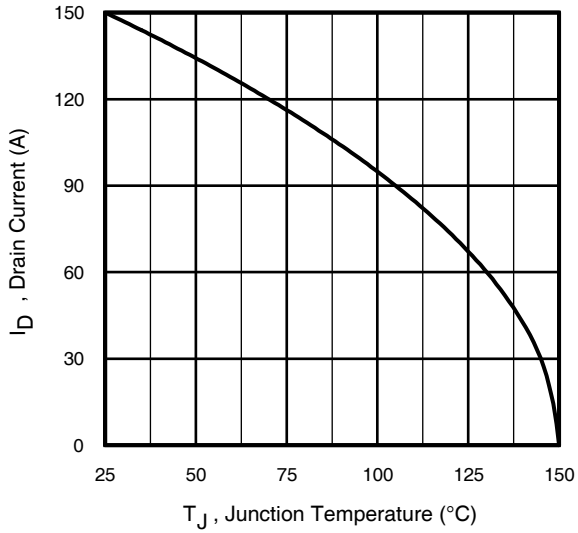
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



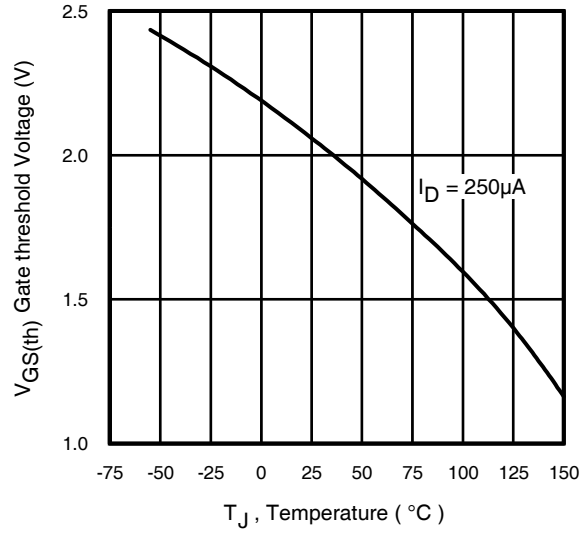
**Fig 7.** Typical Source-Drain Diode Forward Voltage



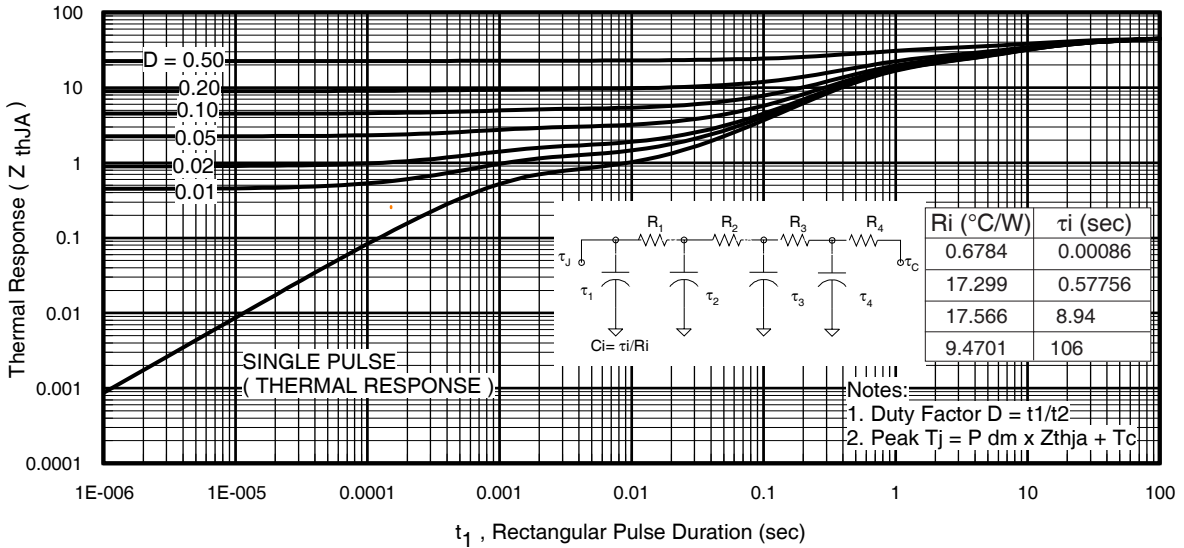
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current vs. Case Temperature



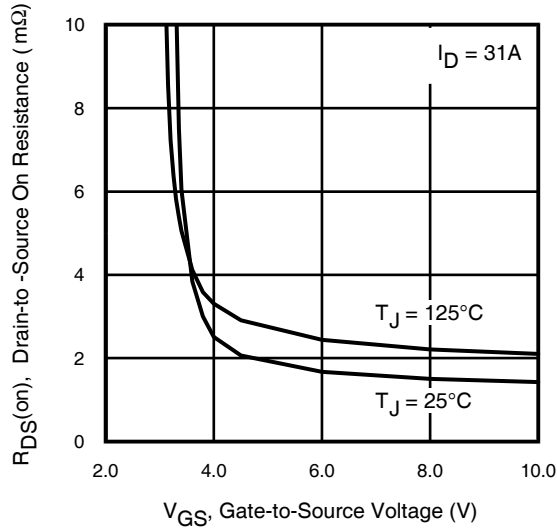
**Fig 10.** Threshold Voltage vs. Temperature



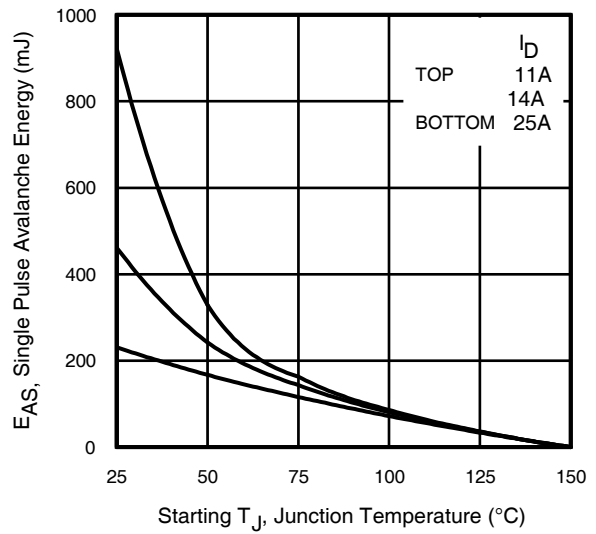
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

# IRF6609

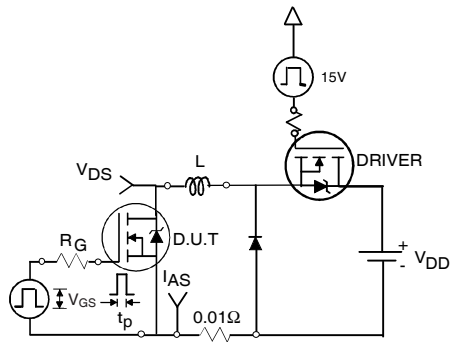
International  
**IR** Rectifier



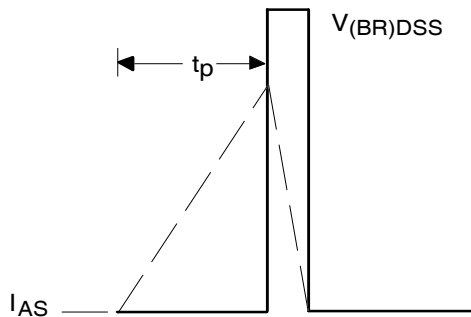
**Fig 12.** On-Resistance Vs. Gate Voltage



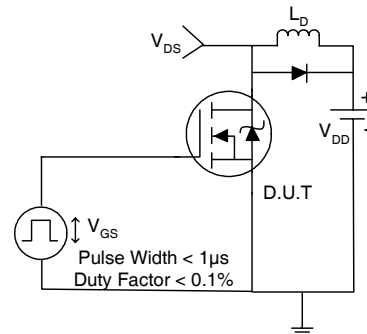
**Fig 13c.** Maximum Avalanche Energy Vs. Drain Current



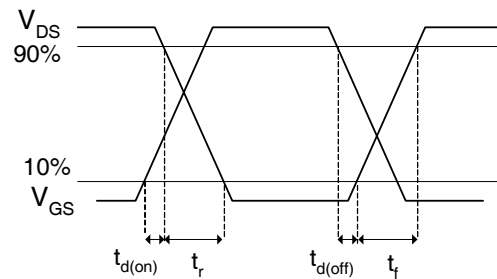
**Fig 13a.** Unclamped Inductive Test Circuit



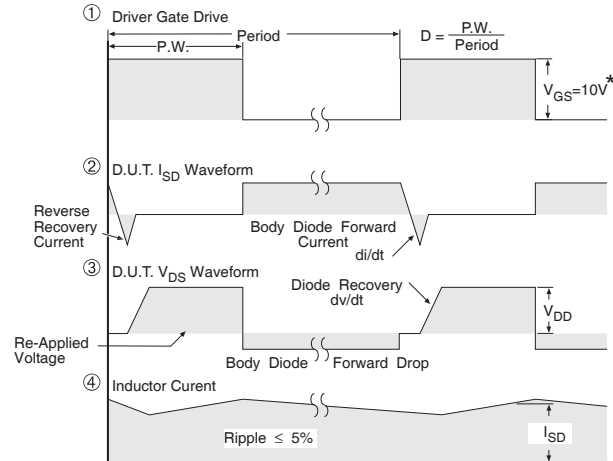
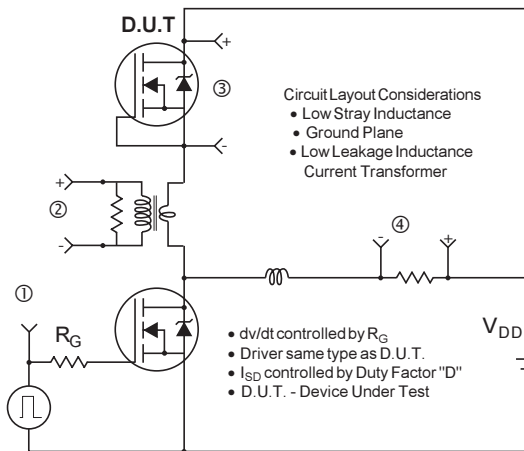
**Fig 13b.** Unclamped Inductive Waveforms



**Fig 14a.** Switching Time Test Circuit

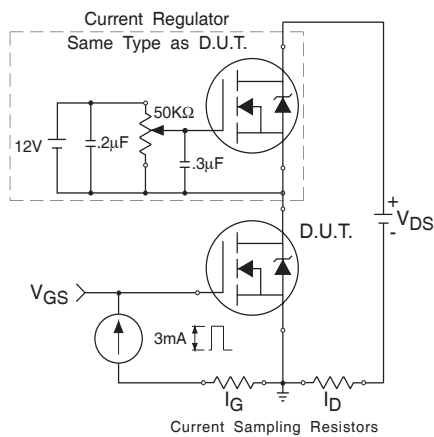


**Fig 14b.** Switching Time Waveforms

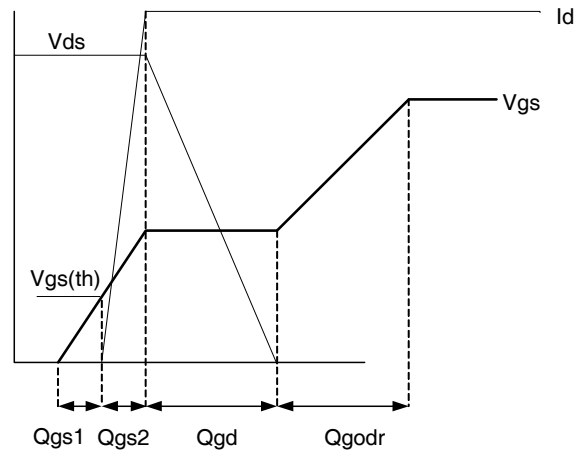


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 15. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



**Fig 16. Gate Charge Test Circuit**



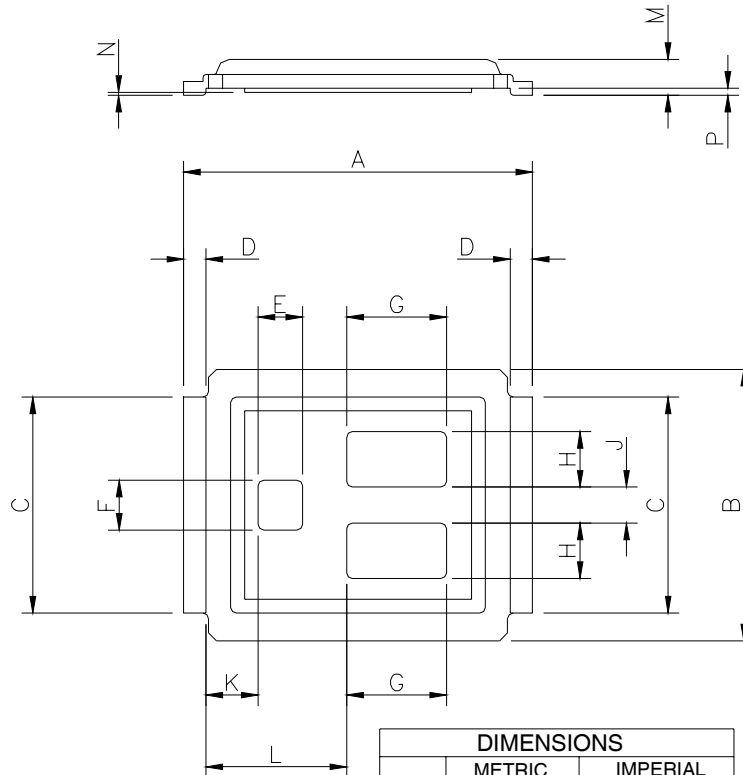
**Fig 17. Gate Charge Waveform**

# IRF6609

International  
**IR** Rectifier

## DirectFET™ Outline Dimension, MT Outline (Medium Size Can, T-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



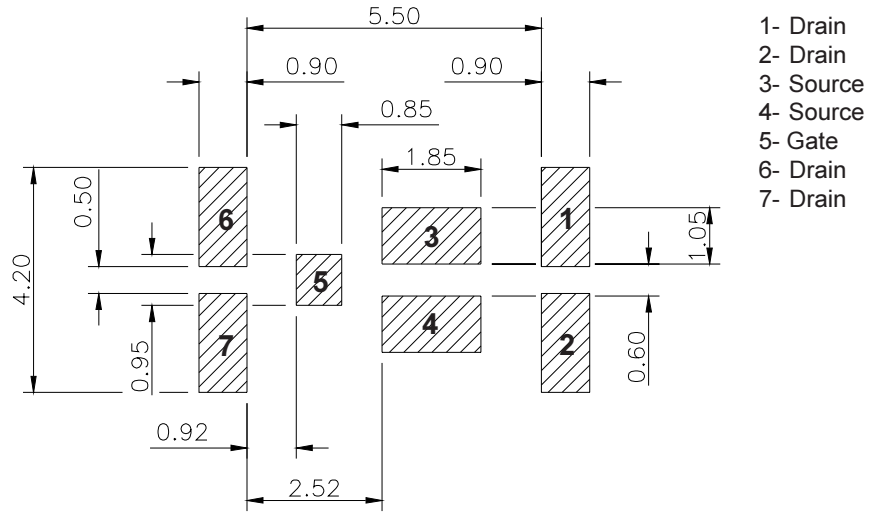
NOTE: CONTROLLING  
DIMENSIONS ARE IN MM

CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.199
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.78	0.82	0.031	0.032
F	0.88	0.92	0.035	0.036
G	1.78	1.82	0.070	0.072
H	0.98	1.02	0.039	0.040
J	0.63	0.67	0.025	0.026
K	0.88	1.01	0.035	0.039
L	2.46	2.63	0.097	0.104
M	0.59	0.70	0.023	0.028
N	0.03	0.08	0.001	0.003
P	0.11	0.14	0.004	0.006

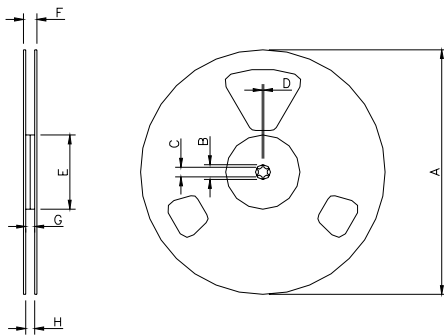


## DirectFET™ Substrate and PCB Layout, MT Outline (Medium Size Can, T-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.

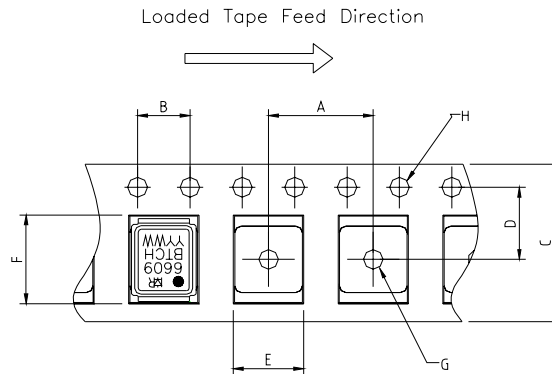


## DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm  
Std reel quantity is 4800 parts. (ordered as IRF6618). For 1000 parts on 7" reel, order IRF6618TR1

CODE	STANDARD OPTION (QTY 4800)				TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C



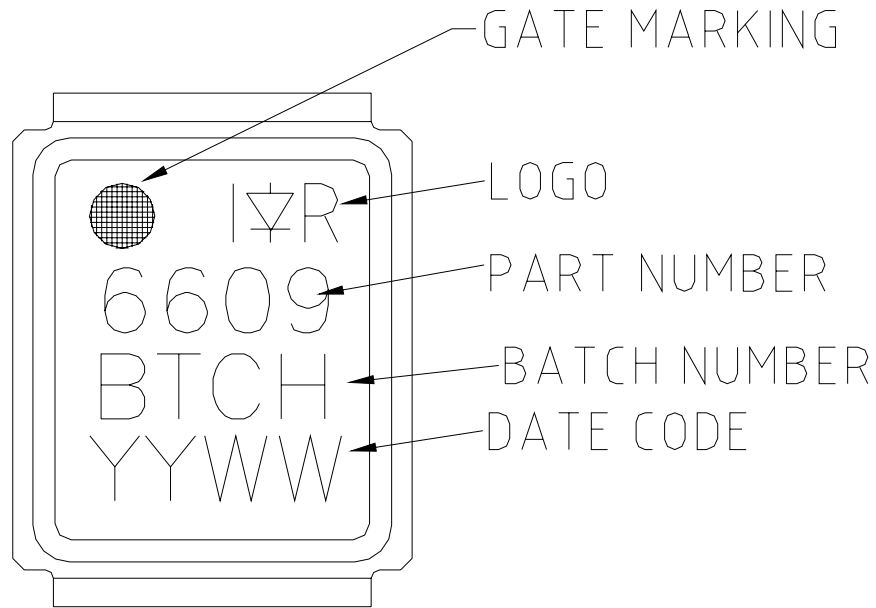
NOTE: CONTROLLING DIMENSIONS IN MM

CODE	DIMENSIONS			
	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

# IRF6609

International  
**IR** Rectifier

## DirectFET™ Part Marking



### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.75\text{mH}$ ,  
 $R_G = 25\Omega$ ,  $I_{AS} = 25\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ Surface mounted on 1 in. square Cu board.
- ⑤ Used double sided cooling , mounting pad.
- ⑥ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑦  $T_C$  measured with thermal couple mounted to top (Drain) of part.
- ⑧  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Consumer market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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