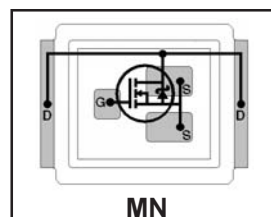


- RoHs Compliant ①
- Lead-Free (Qualified up to 260°C Reflow)
- Application Specific MOSFETs
- Ideal for High Performance Isolated Converter Primary Switch Socket
- Optimized for Synchronous Rectification
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①

Typical values (unless otherwise specified)

V_{DS}	V_{GS}	$R_{DS(on)}$			
80V max	±20V max	7.6mΩ @ 10V			
$Q_{g\ tot}$	Q_{gd}	Q_{gs2}	Q_{rr}	Q_{oss}	$V_{gs(th)}$
36nC	12nC	2.0nC	48nC	18nC	3.8V



Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SQ	SX	ST		MQ	MX	MT	MN			
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Description

The IRF6646PbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of a SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques. Application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6646PbF is optimized for primary side bridge topologies in isolated DC-DC applications, for 48V(±10%) or 36V to 60V ETSI input voltage range systems, and is also ideal for secondary side synchronous rectification in regulated isolated DC-DC topologies. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes this device ideal for high performance isolated DC-DC converters.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	80	V
V_{GS}	Gate-to-Source Voltage	±20	
I_D @ $T_A = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V ③	12	A
I_D @ $T_A = 70^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V ③	9.6	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V ④	68	
I_{DM}	Pulsed Drain Current ⑤	96	
E_{AS}	Single Pulse Avalanche Energy ⑥	230	mJ
I_{AR}	Avalanche Current ⑤	7.2	A

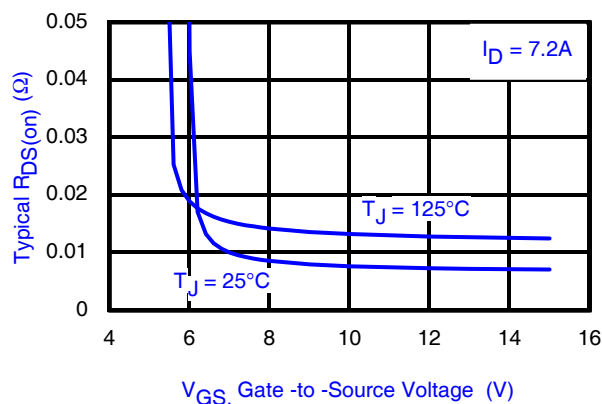


Fig 1. Typical On-Resistance vs. Gate Voltage

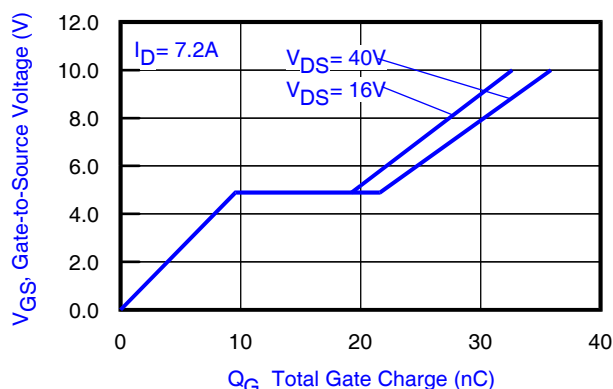


Fig 2. Typical Total Gate Charge vs. Gate-to-Source Voltage

Notes:

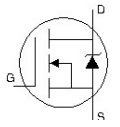
- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.

- ④ T_C measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting $T_J = 25^\circ\text{C}$, $L = 8.8\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 7.2\text{A}$.

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	80	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	7.6	9.5	mΩ	V _{GS} = 10V, I _D = 12A ⑦
V _{GS(th)}	Gate Threshold Voltage	3.0	—	4.9	V	V _{DS} = V _{GS} , I _D = 150μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-11	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	250		V _{DS} = 64V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Transconductance	17	—	—	S	V _{DS} = 10V, I _D = 7.2A
Q _g	Total Gate Charge	—	36	50	nC	V _{DS} = 40V V _{GS} = 10V I _D = 7.2A See Fig. 15
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	—	7.6	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	—	2.0	—		
Q _{gd}	Gate-to-Drain Charge	—	12	—		
Q _{godr}	Gate Charge Overdrive	—	14	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	14	—		
Q _{oss}	Output Charge	—	18	—	nC	V _{DS} = 16V, V _{GS} = 0V
R _G	Gate Resistance	—	1.0	—	Ω	
t _{d(on)}	Turn-On Delay Time	—	17	—	ns	V _{DD} = 40V, V _{GS} = 10V ⑦ I _D = 7.2A R _G =6.2Ω See Fig. 16 & 17
t _r	Rise Time	—	20	—		
t _{d(off)}	Turn-Off Delay Time	—	31	—		
t _f	Fall Time	—	12	—		
C _{iss}	Input Capacitance	—	2060	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	480	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	120	—		f = 1.0MHz
C _{oss}	Output Capacitance	—	2180	—		V _{GS} = 0V, V _{DS} = 1.0V, f=1.0MHz
C _{oss}	Output Capacitance	—	310	—		V _{GS} = 0V, V _{DS} = 64V, f=1.0MHz

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.5⑧	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ⑤	—	—	96		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 7.2A, V_{GS} = 0V$ ⑦
t_{rr}	Reverse Recovery Time	—	36	54	ns	$T_J = 25^\circ\text{C}, I_F = 7.2A, V_{DD} = 40V$ $di/dt = 100A/\mu s$ ⑦ See Fig. 18
Q_{rr}	Reverse Recovery Charge	—	48	72	nC	

Notes:

- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑦ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑧ Thermally limited and used $R_{\theta ja}$ to calculate.

Absolute Maximum Ratings

	Parameter	Max.	Units
P_D @ $T_A = 25^\circ\text{C}$	Power Dissipation ③	2.8	W
P_D @ $T_A = 70^\circ\text{C}$	Power Dissipation ③	1.8	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation ④	89	
T_P	Peak Soldering Temperature	270	$^\circ\text{C}$
T_J	Operating Junction and	-40 to + 150	
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③ ①	—	45	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient ⑨ ①	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑩ ①	20	—	
$R_{\theta JC}$	Junction-to-Case ④ ①	—	1.4	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	—	
	Linear Derating Factor ③	0.022		

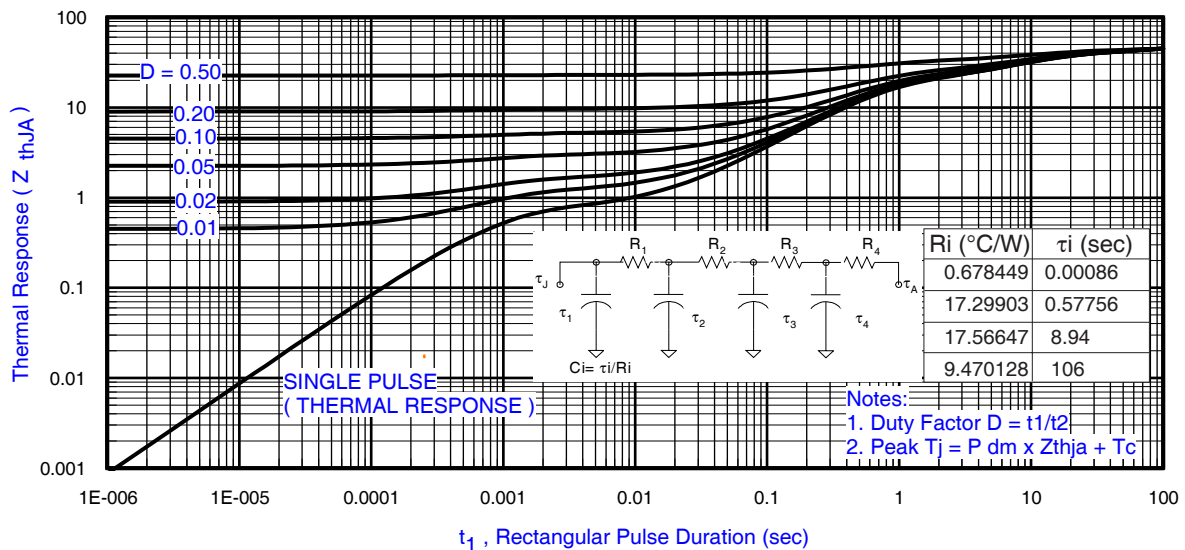


Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ①

Notes:

⑨ Used double sided cooling, mounting pad.

① R_{θ} is measured at T_J of approximately 90°C .

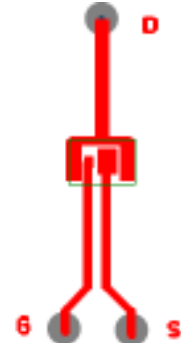
⑩ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.



③ Surface mounted on 1 in. square Cu (still air).



⑨ Mounted to a PCB with small clip heatsink (still air)



⑩ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

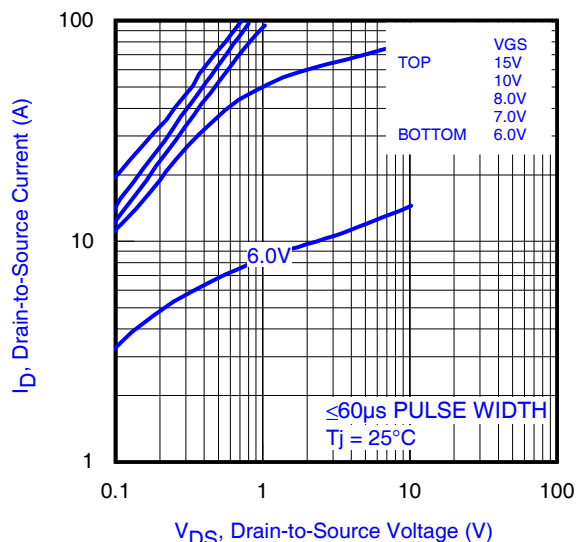


Fig 4. Typical Output Characteristics

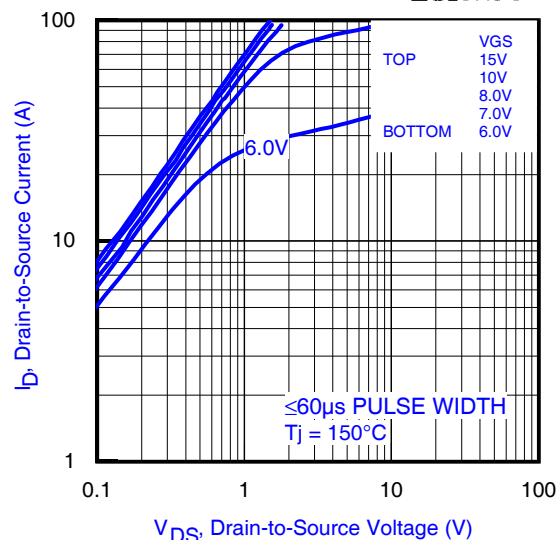


Fig 5. Typical Output Characteristics

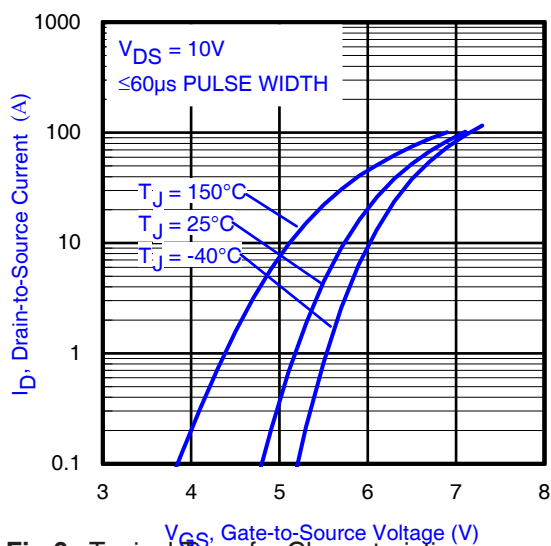


Fig 6. Typical Transfer Characteristics

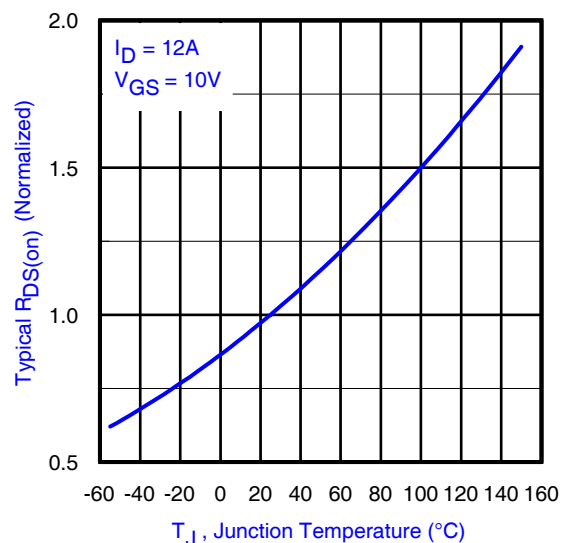


Fig 7. Normalized On-Resistance vs. Temperature

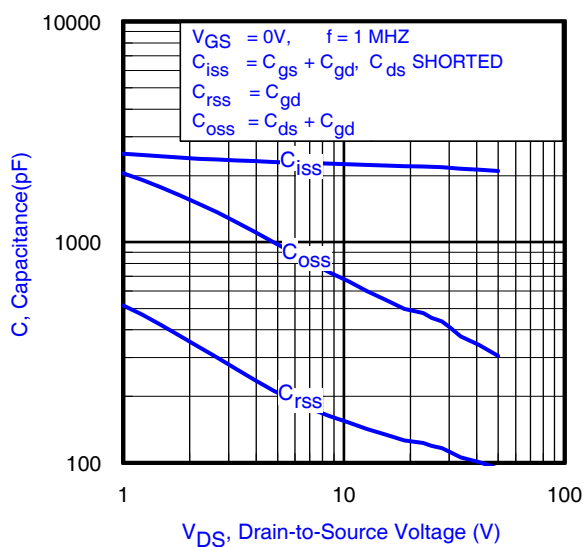


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

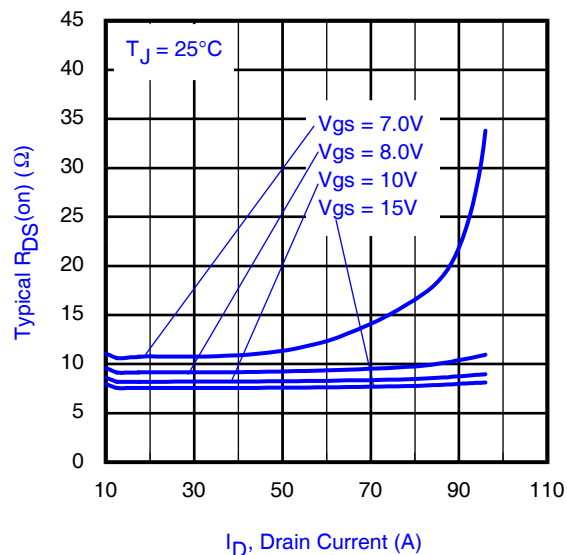


Fig 9. Typical On-Resistance vs. Drain Current

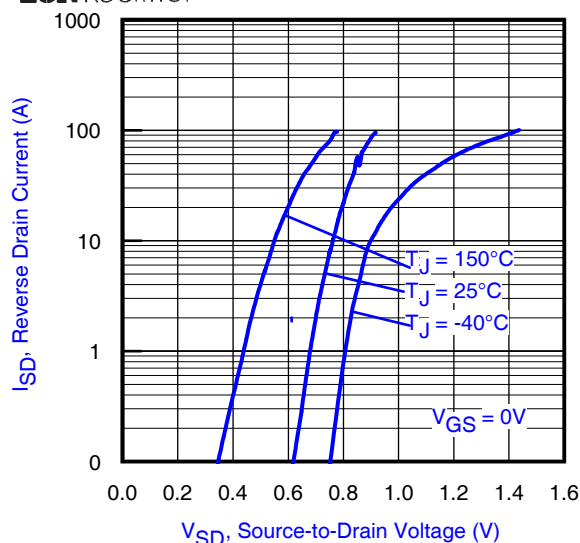


Fig 10. Typical Source-Drain Diode Forward Voltage

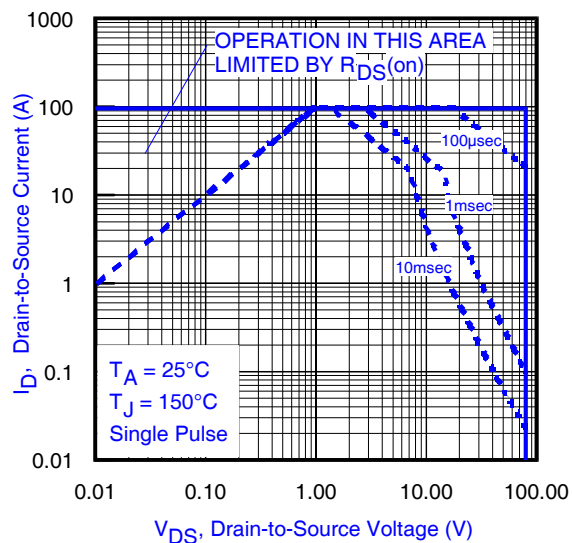


Fig 11. Maximum Safe Operating Area

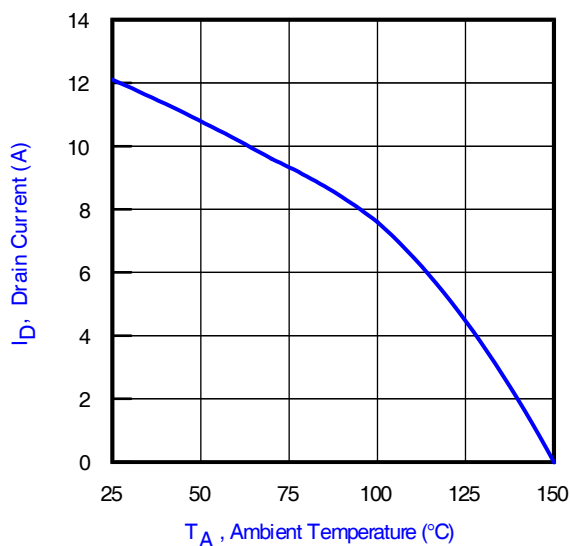


Fig 12. Maximum Drain Current vs. Ambient Temperature

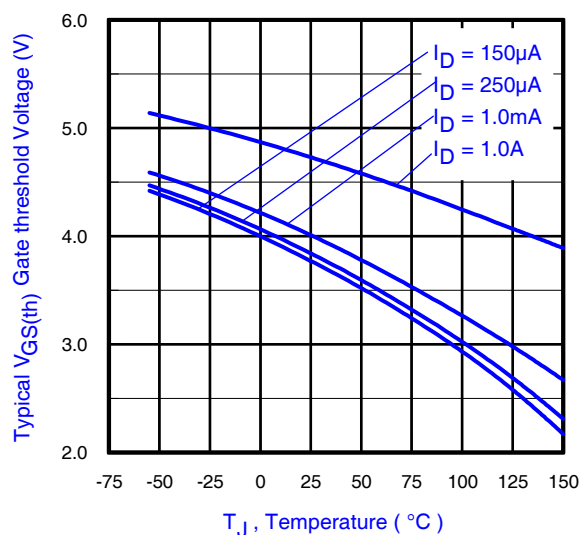


Fig 13. Typical Threshold Voltage vs. Junction Temperature

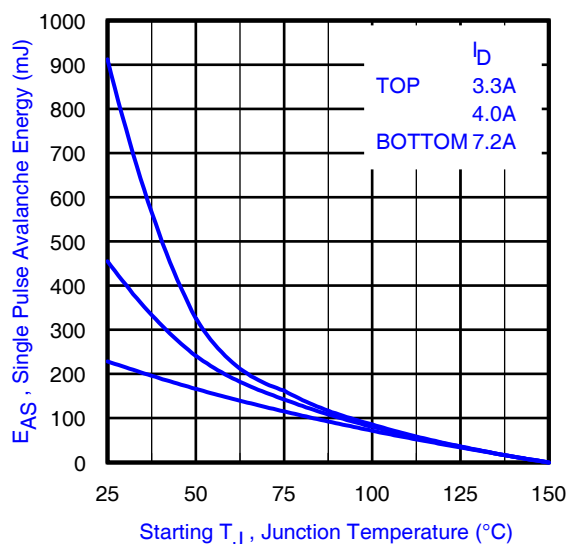


Fig 14. Maximum Avalanche Energy vs. Drain Current



Fig 15a. Gate Charge Test Circuit

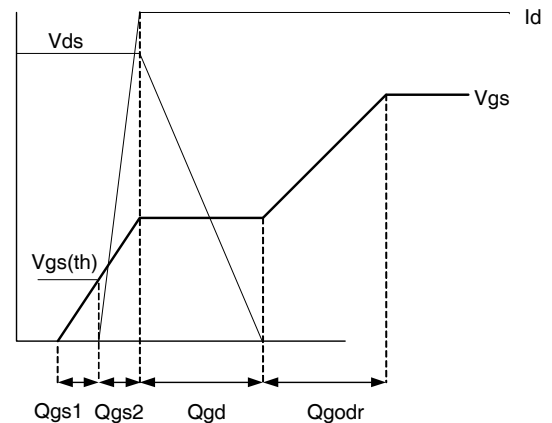


Fig 15b. Gate Charge Waveform

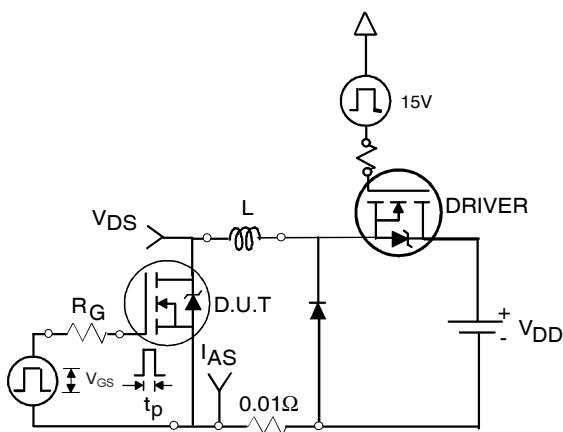


Fig 16a. Unclamped Inductive Test Circuit

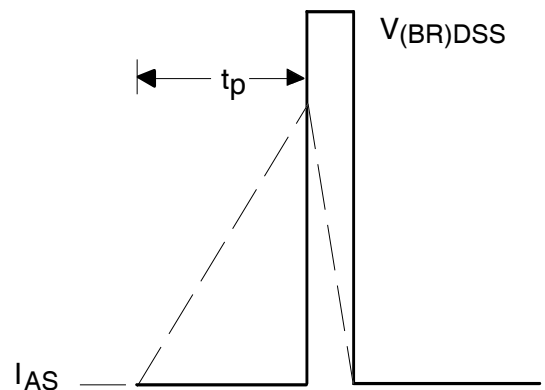


Fig 16b. Unclamped Inductive Waveforms

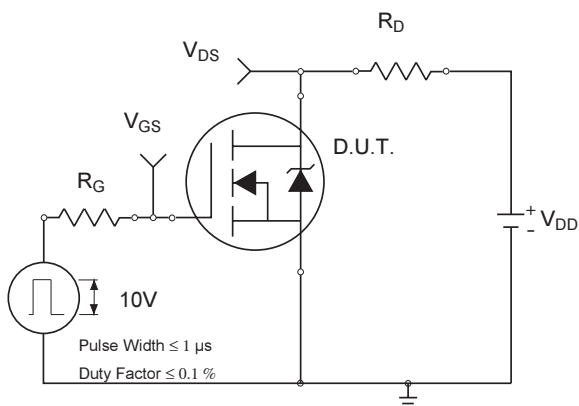


Fig 17a. Switching Time Test Circuit

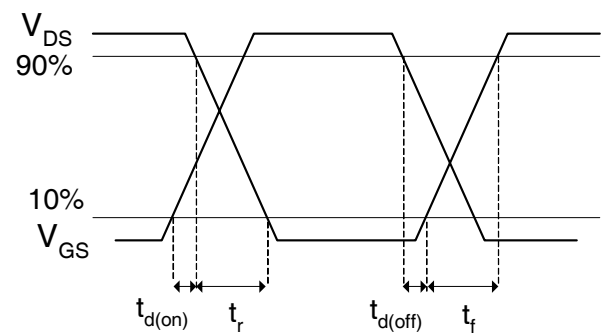


Fig 17b. Switching Time Waveforms

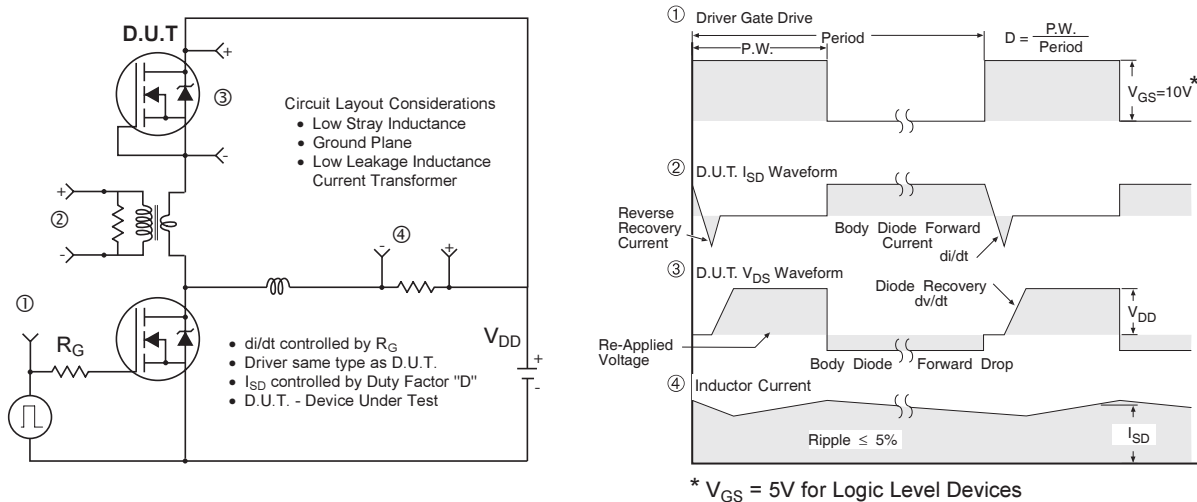
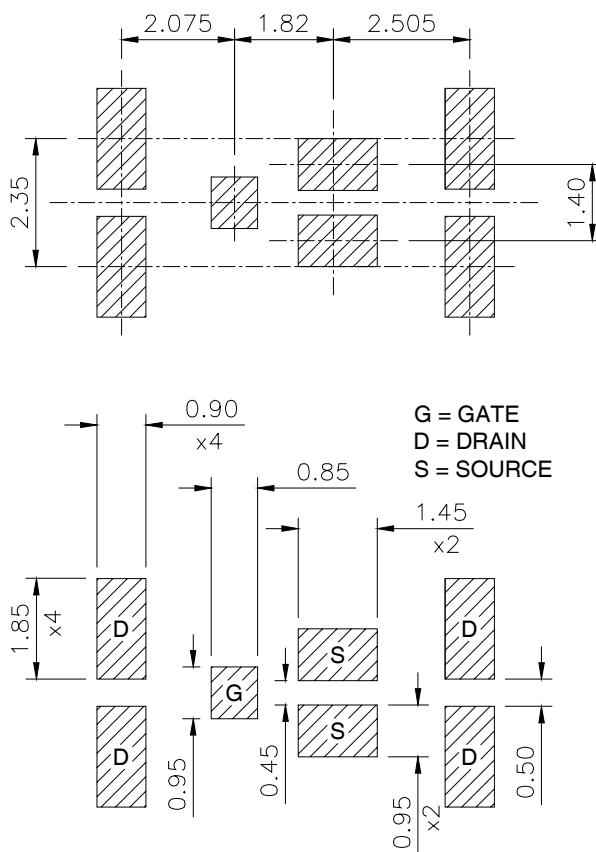


Fig 18. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

DirectFET™ Substrate and PCB Layout, MN Outline (Medium Size Can, N-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.

This includes all recommendations for stencil and substrate designs.

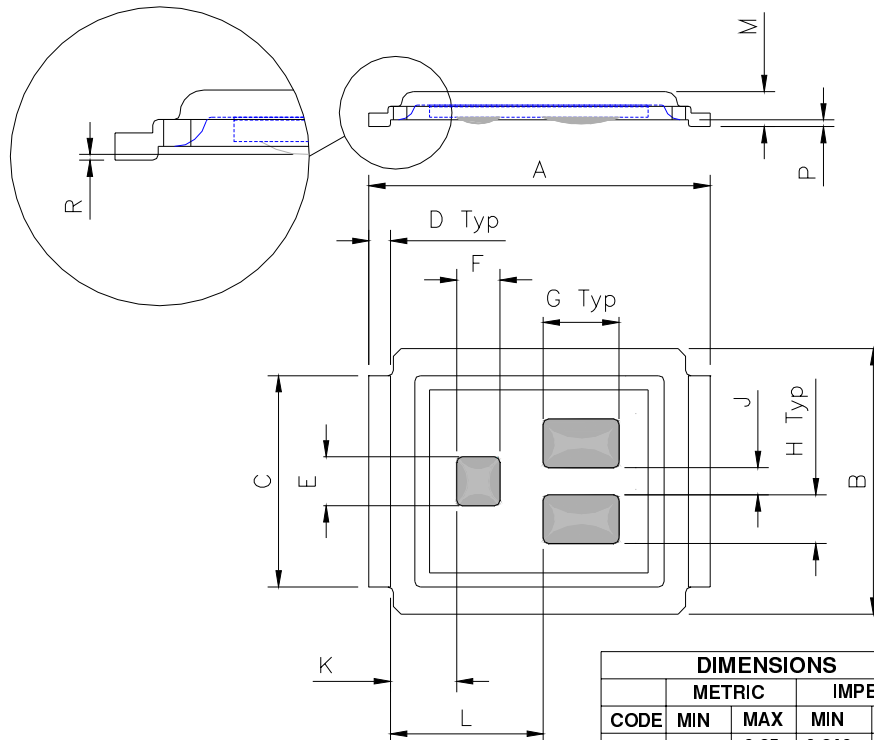


IRF6646PbF

DirectFET™ Outline Dimension, MN Outline (Medium Size Can, N-Designation).

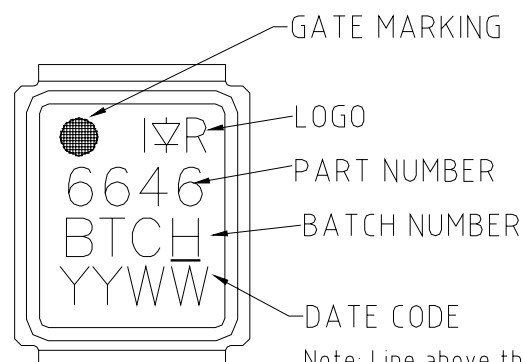
Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.

This includes all recommendations for stencil and substrate designs.



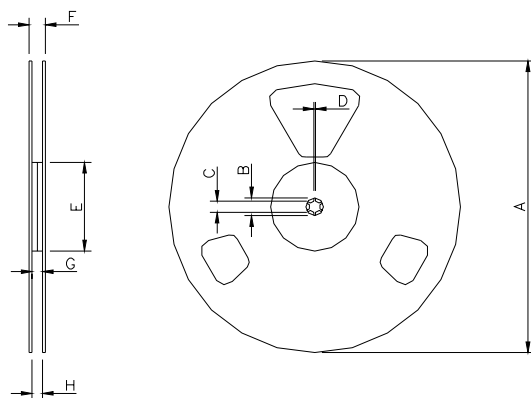
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.201
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.88	0.92	0.034	0.036
F	0.78	0.82	0.031	0.032
G	1.38	1.42	0.054	0.056
H	0.88	0.92	0.034	0.036
J	0.48	0.52	0.019	0.020
K	1.16	1.29	0.046	0.051
L	2.74	2.91	0.109	0.115
M	0.616	0.676	0.0235	0.0274
R	0.020	0.080	0.0008	0.0031
P	0.08	0.17	0.003	0.007

DirectFET™ Part Marking



Note: Line above the last character of the date-code indicates "Lead-Free".

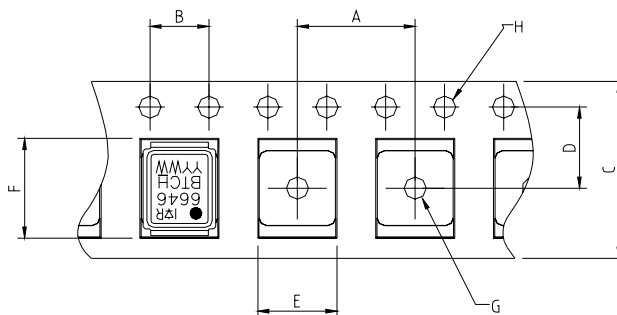
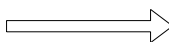
DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. (ordered as IRF6646TRPBF). For 1000 parts on 7" reel, order IRF6646TR1PBF

REEL DIMENSIONS								
STANDARD OPTION (QTY 4800)					TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

LOADED TAPE FEED DIRECTION



DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Data and specifications subject to change without notice.

This product has been designed and qualified for the Consumer market.

Qualification Standards can be found on IR's Web site.

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.08/06

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>