

N-Channel Power MOSFET (5.5A, 400Volts)

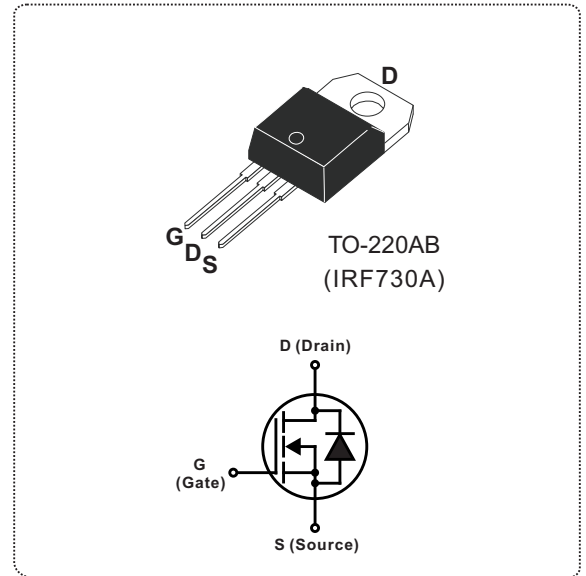
DESCRIPTION

The Nell **IRF730** are N-Channel enhancement mode silicon gate power field effect transistors. They are designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation.

They are designed as an extremely efficient and reliable device for use in a wide variety of applications such as switching regulators, convertors, UPS, switching mode power supplies and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These transistors can be operated directly from integrated circuits.

FEATURES

- $R_{DS(ON)} = 1.00\Omega @ V_{GS} = 10V$
- Ultra low gate charge(22nC Max.)
- Low reverse transfer capacitance ($C_{RSS} = 4pF$ typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature



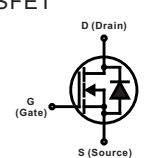
PRODUCT SUMMARY	
I_D (A)	5.5
V_{DSS} (V)	400
$R_{DS(ON)}$ (Ω)	1.00 @ $V_{GS} = 10V$
Q_G (nC) max.	22

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ unless otherwise specified)				
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
V_{DSS}	Drain to Source voltage(Note 1)	$T_J = 25^\circ C$ to $150^\circ C$	400	V
V_{DGR}	Drain to Gate voltage	$R_{GS} = 20K\Omega$	400	
V_{GS}	Gate to Source voltage		± 30	
I_D	Continuous Drain Current	$V_{GS} = 10V, T_C = 25^\circ C$	5.5	A
		$V_{GS} = 10V, T_C = 100^\circ C$	3.5	
I_{DM}	Pulsed Drain current(Note 1)		22	
I_{AR}	Avalanche current(Note 1)		5.5	
E_{AR}	Repetitive avalanche energy(Note 1)	$I_{AR} = 5.5A, R_{GS} = 50\Omega, V_{GS} = 10V$	7.4	mJ
E_{AS}	Single pulse avalanche energy(Note 2)	$I_{AS} = 5.5A, L = 19mH$	290	mJ
dv/dt	Peak diode recovery dv/dt(Note 3)		4.6	V/ns
P_D	Total power dissipation	$T_C = 25^\circ C$	75	W
	Derating factor above $25^\circ C$		0.6	W / $^\circ C$
T_J	Operation junction temperature		-55 to 150	$^\circ C$
T_{STG}	Storage temperature		-55 to 150	
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf-in (N·m)

Note: 1. Repetitive rating: pulse width limited by junction temperature.
 2. $V_{DD} \leq 50V, L = 19mH, I_{AS} = 5.5A, R_G = 25\Omega, \text{ starting } T_J = 25^\circ C$
 3. $I_{SD} \leq 5.5A, di/dt \leq 90A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ C.$

THERMAL RESISTANCE					
SYMBOL	PARAMETER	Min.	Typ.	Max.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case			1.7	°C/W
$R_{th(c-s)}$	Thermal resistance, case to heatsink		0.50		
$R_{th(j-a)}$	Thermal resistance, junction to ambient			62	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
$V_{(BR)DSS}$	Drain to source breakdown voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	400			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown voltage temperature coefficient	$I_D = 1\text{mA}$, referenced to 25°C		0.5		V/°C
I_{DSS}	Drain to source leakage current	$V_{DS}=400\text{V}, V_{GS}=0\text{V}$ $T_C = 25^\circ\text{C}$			25	μA
		$V_{DS}=320\text{V}, V_{GS}=0\text{V}$ $T_J=125^\circ\text{C}$			250	
I_{GSS}	Gate to source forward leakage current	$V_{GS} = 30\text{V}, V_{DS} = 0\text{V}$			100	nA
	Gate to source reverse leakage current	$V_{GS} = -30\text{V}, V_{DS} = 0\text{V}$			-100	
$R_{DS(ON)}$	Static drain to source on-state resistance	$V_{GS} = 10\text{V}, I_D = 3.3\text{A}$ (Note 1),		0.8	1	Ω
$V_{GS(TH)}$	Gate threshold voltage	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2.0		4.5	V
g_{fs}	Forward transconductance	$V_{DS}=50\text{V}, I_D=3.3\text{A}$,	3.1	4.5		S
C_{ISS}	Input capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		600		μF
C_{OSS}	Output capacitance			103		
C_{RSS}	Reverse transfer capacitance			4		
$t_{d(ON)}$	Turn-on delay time	$V_{DD} = 200\text{V}, I_D = 5.5\text{A}, R_D = 57\Omega,$ $V_{GS} = 10\text{V}, R_G = 12\Omega$ (Note 1)		10		ns
t_r	Rise time			22		
$t_{d(OFF)}$	Turn-off delay time			20		
t_f	Fall time			16		
L_D	Internal drain inductance	Between lead, 6mm from package and center of die		4.5		nH
L_S	internal source inductance			7.5		
Q_G	Total gate charge	$V_{DS} = 320\text{V}, V_{GS} = 10\text{V}, I_D = 5.5\text{A}$			22	nC
Q_{GS}	Gate to source charge				5.8	
Q_{GD}	Gate to drain charge (Miller charge)				9.3	

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
V_{SD}	Diode forward voltage	$I_{SD} = 5.5\text{A}, V_{GS} = 0\text{V}$			1.6	V
I_S (I_{SD})	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET 			5.5	A
I_{SM}	Pulsed source current				22	
t_{rr}	Reverse recovery time	$I_S = 5.5\text{A}, V_{GS} = 0\text{V},$ $di_F/dt = 100\text{A}/\mu\text{s}$		370	550	ns
Q_{rr}	Reverse recovery charge			1.6	2.4	μC
t_{ON}	Forward turn-on time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Note: 1. Pulse test: Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

ORDERING INFORMATION SCHEME

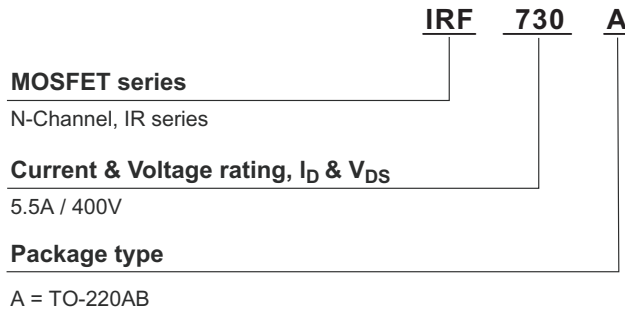


Fig.1 Typical output characteristics

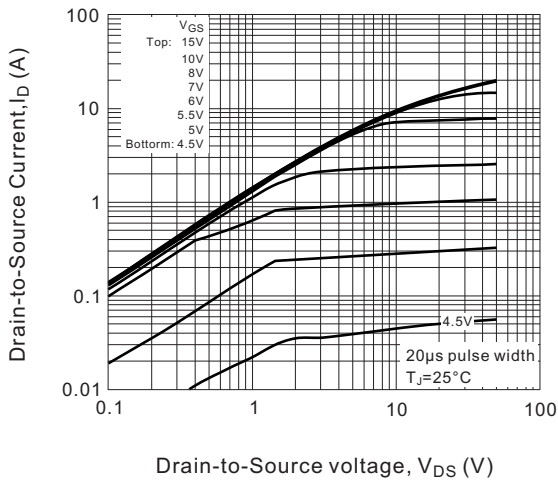


Fig.2 Typical output characteristics

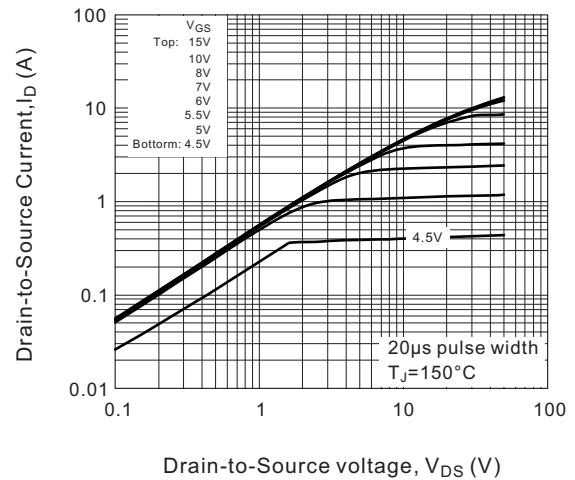


Fig.3 Typical transfer characteristics

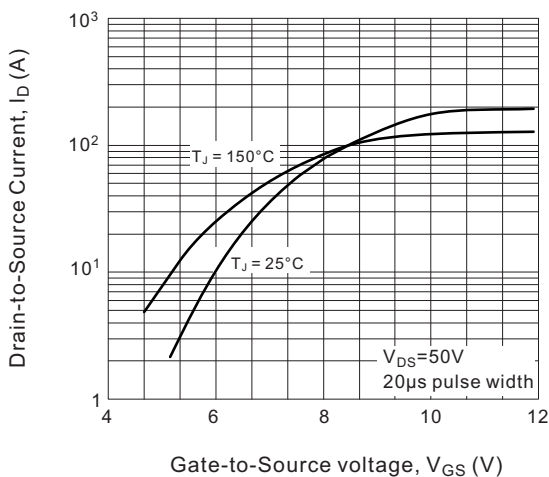


Fig.4 Normalized On-Resistance vs. Temperature

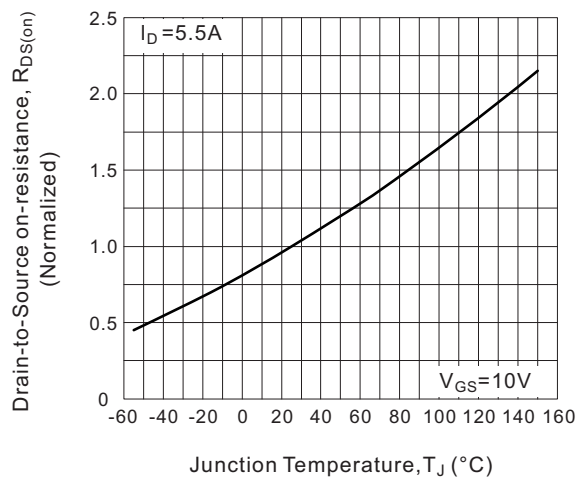


Fig.5 Typical capacitance vs. Drain-to-Source voltage

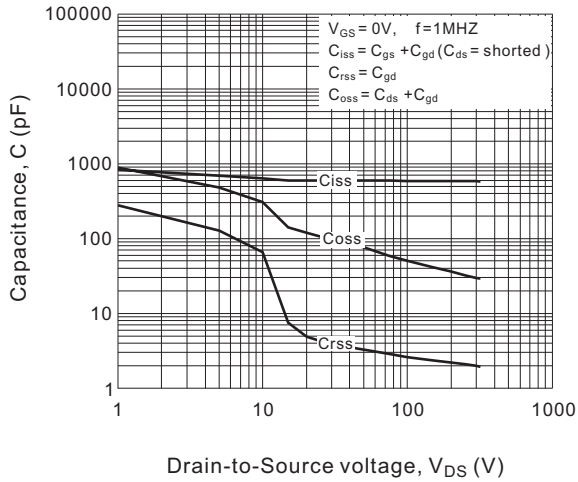


Fig.6 Typical gate charge vs. Gate-to-Source voltage

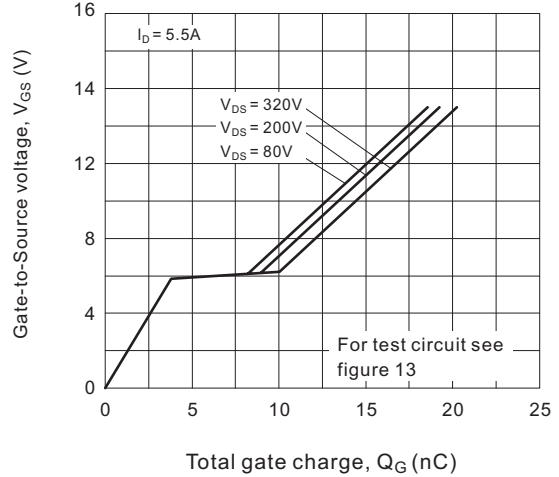


Fig.7 Typical Source-Drain diode forward voltage

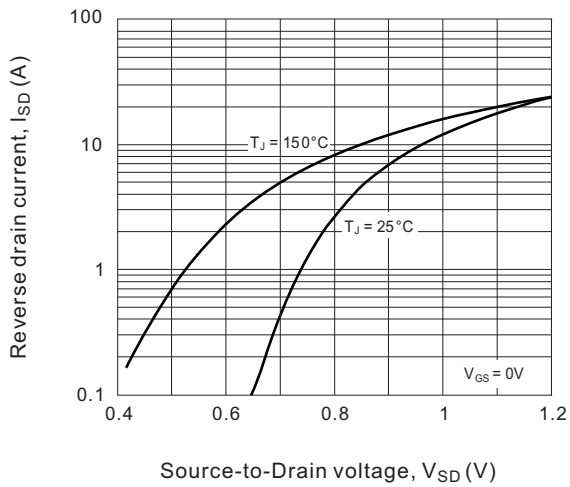


Fig.8 Maximum safe operating area

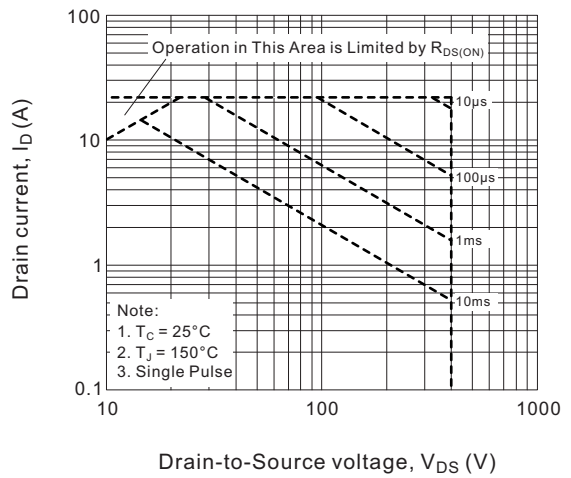


Fig.9 Maximum drain current vs. Case temperature

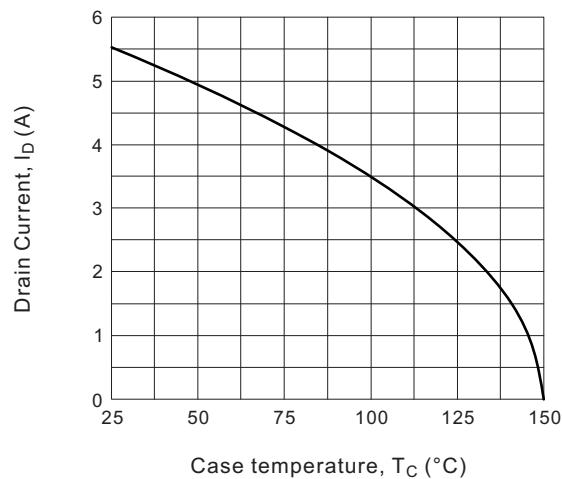


Fig.10 Maximum effective transient thermal Impedance, Junction-to-Case

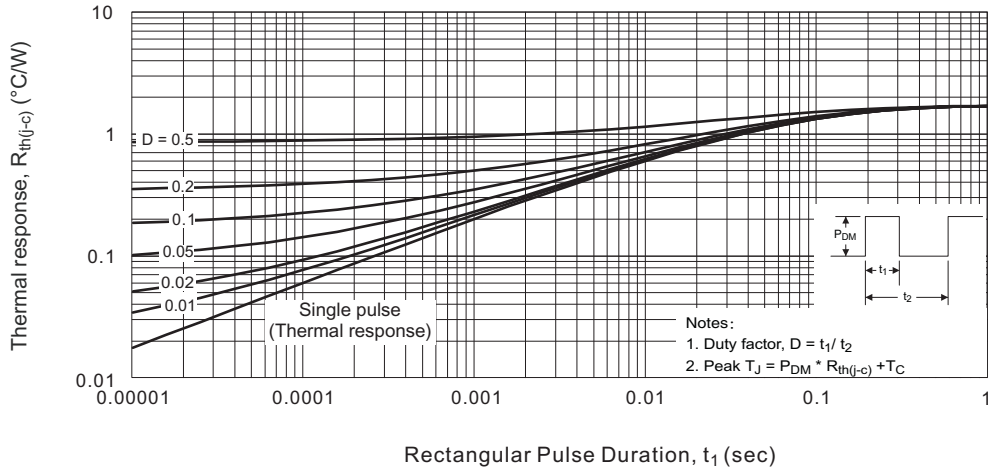


Fig.11a. Switching time test circuit

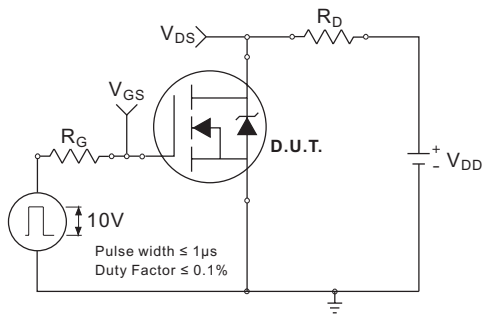


Fig.11b. Switching time waveforms

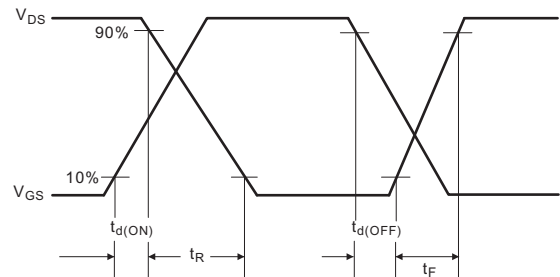


Fig.12a. Unclamped Inductive test circuit

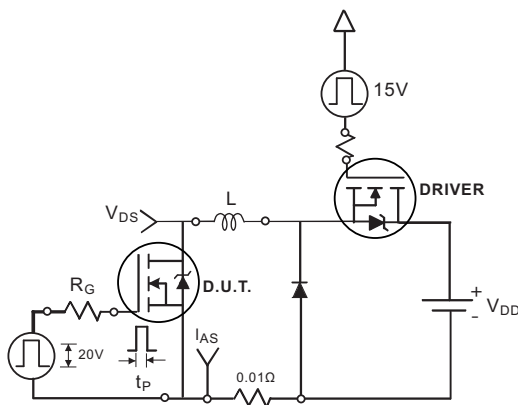


Fig.12b. Unclamped Inductive waveforms

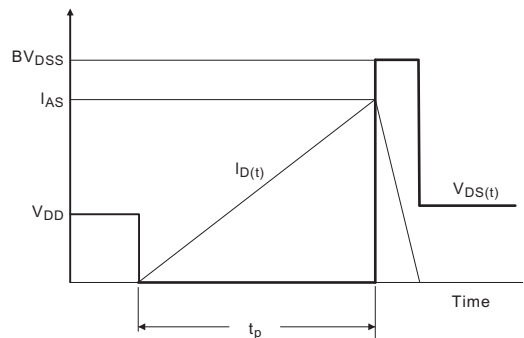


Fig.12c. Maximum avalanche energy vs. Drain current

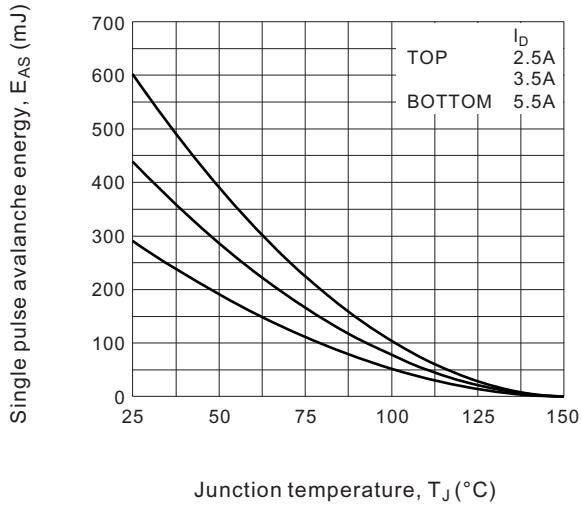


Fig.12d. Typical drain-to-source voltage vs. Avalanche current

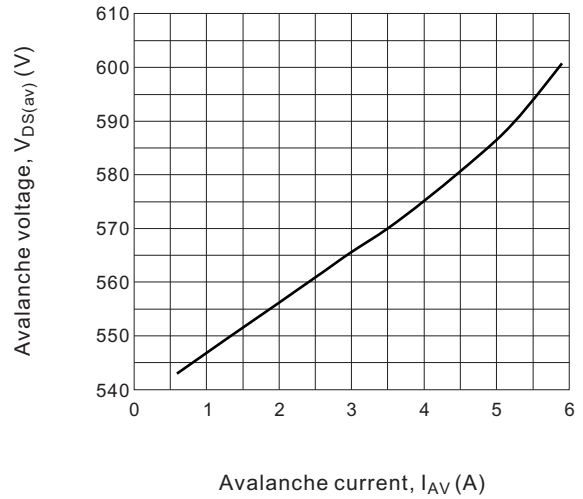


Fig.13a. Basic gate charge waveform

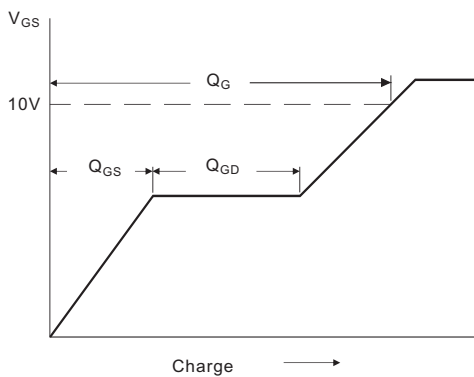


Fig.13b. Gate charge test circuit

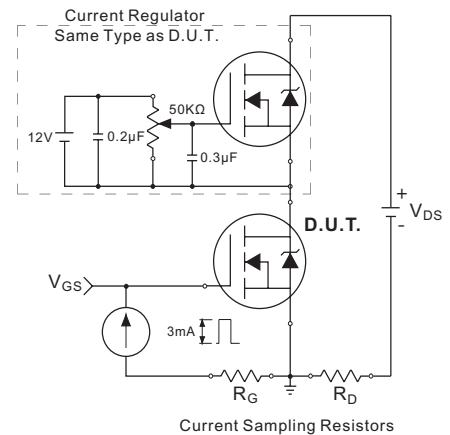
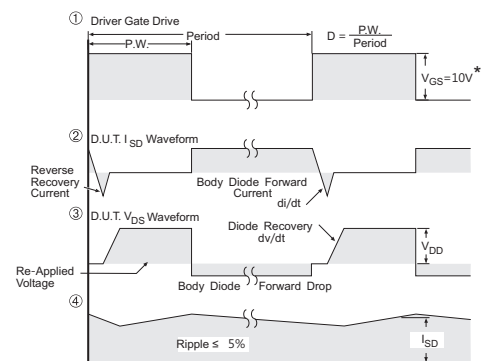
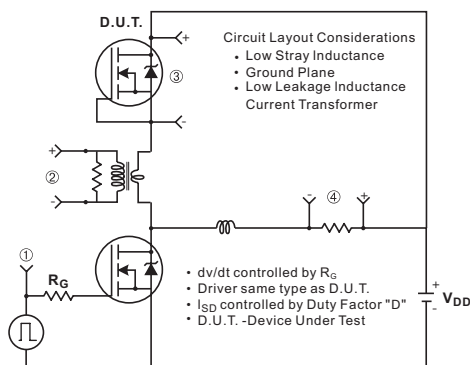
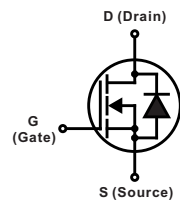
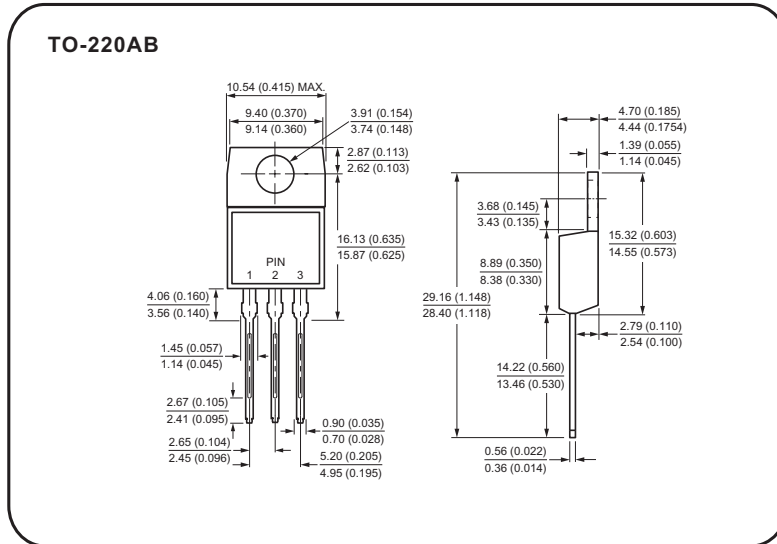


Fig.14 Peak diode recovery dv/dt test circuit for N-Channel MOSFET



* $V_{GS} = 5V$ for Logic Level Devices

Case Style



All dimensions in millimeters(inches)