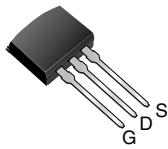




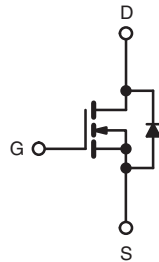
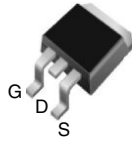
Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	400
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.55
Q_g (Max.) (nC)	36
Q_{gs} (nC)	9.9
Q_{gd} (nC)	16
Configuration	Single

I²PAK (TO-262)



D²PAK (TO-263)



N-Channel MOSFET

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{oss} specified
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High speed Power Switching

TYPICAL SMPS TOPOLOGIES

- Single Transistor Flyback Xfmr. Reset
- Single Transistor Forward Xfmr. Reset (Both for US Line Input Only)

ORDERING INFORMATION				
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHF740AS-GE3	SiHF740ASTRL-GE3 ^a	SiHF740ASTRR-GE3 ^a	SiHF740AL-GE3
Lead (Pb)-free	IRF740ASPbF	IRF740ASTRLPbF ^a	IRF740ASTRRPbF ^a	IRF740ALPbF
	SiHF740AS-E3	SiHF740ASTL-E3 ^a	SiHF740ASTR-E3 ^a	SiHF740AL-E3

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	400	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ^e	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	10
		$T_C = 100\text{ }^\circ\text{C}$	6.3
Pulsed Drain Current ^{a, e}		I_{DM}	40
Linear Derating Factor			1.0
Single Pulse Avalanche Energy ^{b, e}		E_{AS}	630
Avalanche Current ^a		I_{AR}	10
Repetitive Avalanche Energy ^a		E_{AR}	12.5
Maximum Power Dissipation		$T_A = 25\text{ }^\circ\text{C}$	3.1
		$T_C = 25\text{ }^\circ\text{C}$	125
Peak Diode Recovery dV/dt ^{c, e}		dV/dt	5.9
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150
Soldering Recommendations (Peak Temperature)		for 10 s	300 ^d

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 12.6\text{ mH}$, $R_g = 25\text{ } \Omega$, $I_{AS} = 10\text{ A}$ (see fig. 12).
- $I_{SD} \leq 10\text{ A}$, $dI/dt \leq 330\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.
- Uses IRF740A, SiHF740A data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, Steady-State) ^a	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

Note

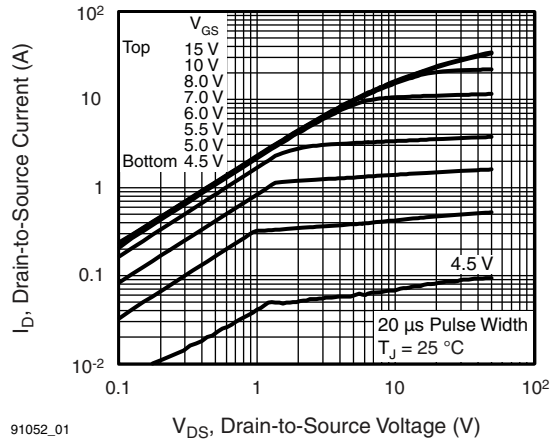
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	400	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^d$	-	0.48	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA	
		$V_{DS} = 320\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 6.0\text{ A}^b$	-	-	0.55	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 6.0\text{ A}^d$	4.9	-	-	S	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5 ^d	-	1030	-	pF	
Output Capacitance	C_{oss}		-	170	-		
Reverse Transfer Capacitance	C_{rss}		-	7.7	-		
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	1490	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 320\text{ V}, f = 1.0\text{ MHz}$	-	52	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}, V_{DS} = 320\text{ V}$, see fig. 6 and 13 ^{b, d}	-	-	36	nC
Gate-Source Charge	Q_{gs}			-	-	9.9	
Gate-Drain Charge	Q_{gd}			-	-	16	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 200\text{ V}, I_D = 10\text{ A}, R_g = 10\text{ }\Omega, R_D = 19.5\text{ }\Omega$, see fig. 10 ^{b, d}	-	10	-	ns	
Rise Time	t_r		-	35	-		
Turn-Off Delay Time	$t_{d(off)}$		-	24	-		
Fall Time	t_f		-	22	-		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	10	A	
Pulsed Diode Forward Current ^a	I_{SM}		-	-	40		
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 10\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	2.0	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b, d$	-	240	360	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	1.9	2.9	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

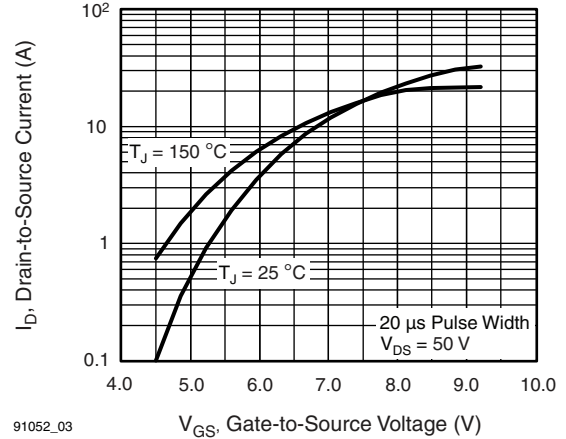
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .
- Uses IRF740A, SiHF740A data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



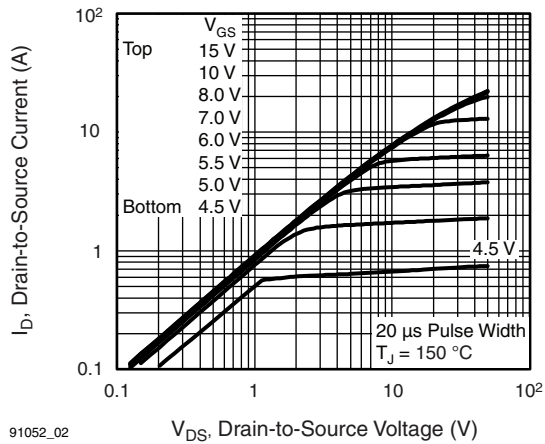
91052_01

Fig. 1 - Typical Output Characteristics



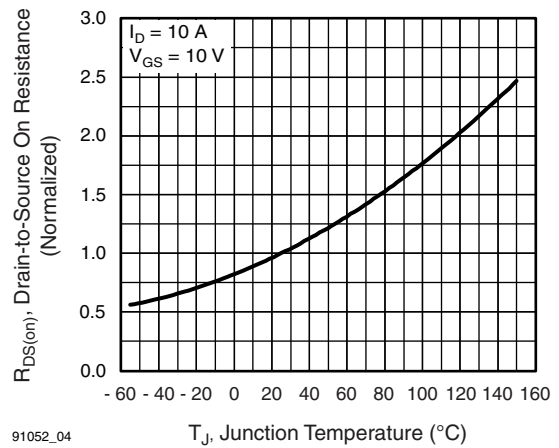
91052_03

Fig. 3 - Typical Transfer Characteristics



91052_02

Fig. 2 - Typical Output Characteristics



91052_04

Fig. 4 - Normalized On-Resistance vs. Temperature

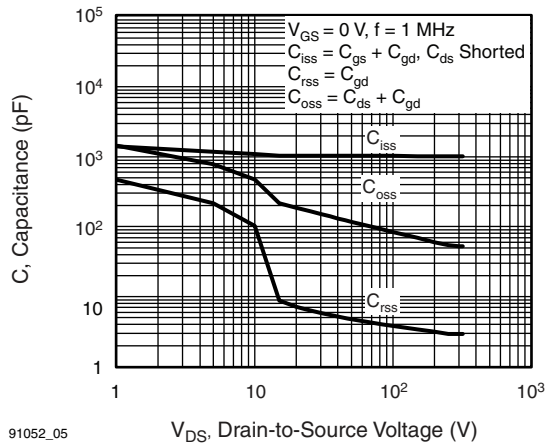


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

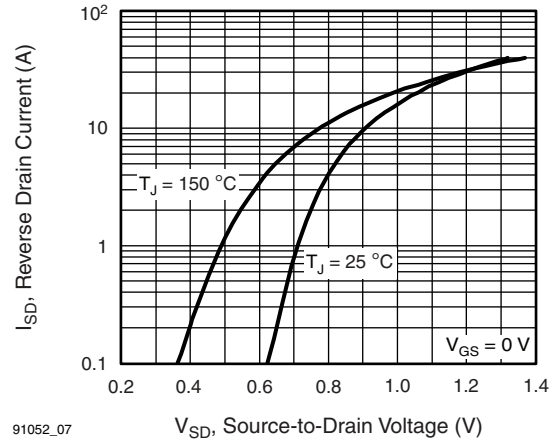


Fig. 7 - Typical Source-Drain Diode Forward Voltage

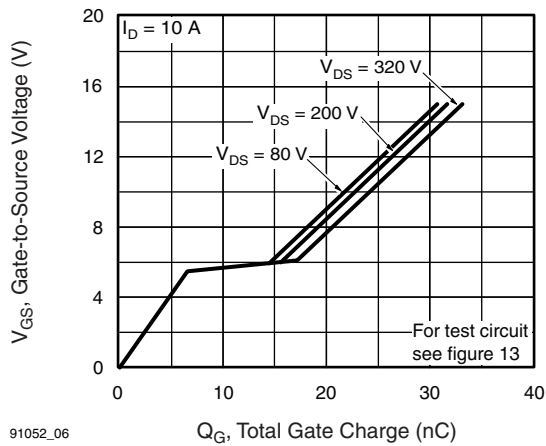


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

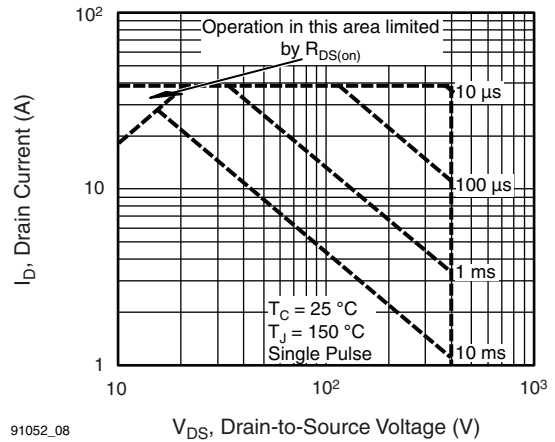
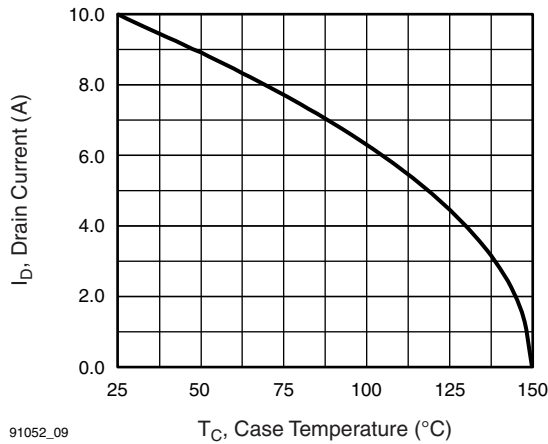


Fig. 8 - Maximum Safe Operating Area



91052_09

Fig. 9 - Maximum Drain Current vs. Case Temperature

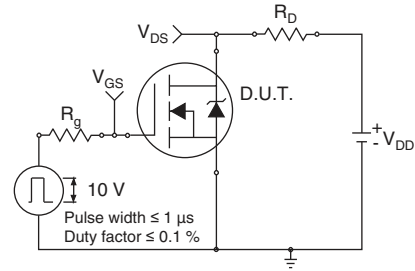


Fig. 10a - Switching Time Test Circuit

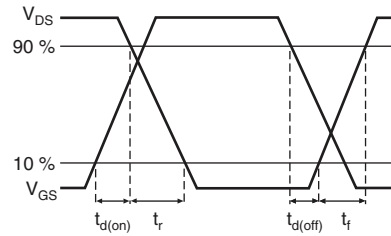
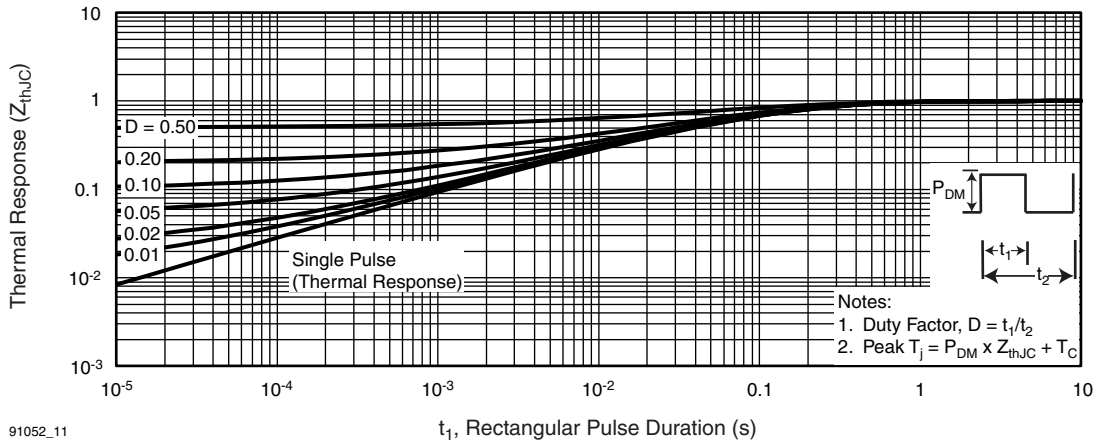


Fig. 10b - Switching Time Waveforms



91052_11

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

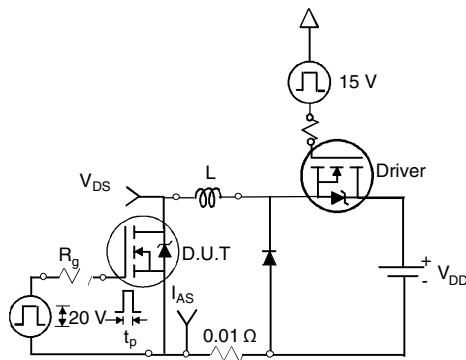


Fig. 12a - Unclamped Inductive Test Circuit

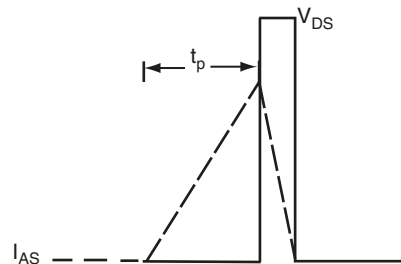


Fig. 12b - Unclamped Inductive Waveforms

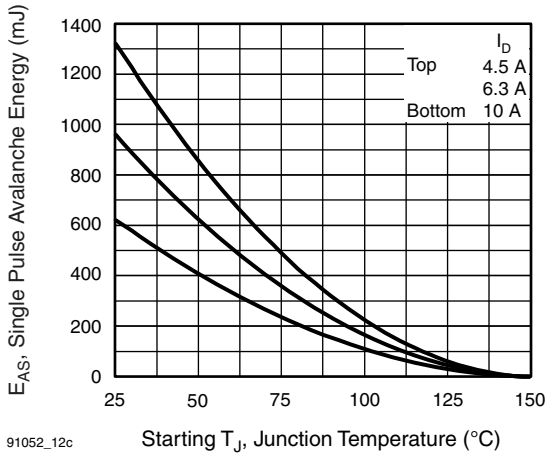


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

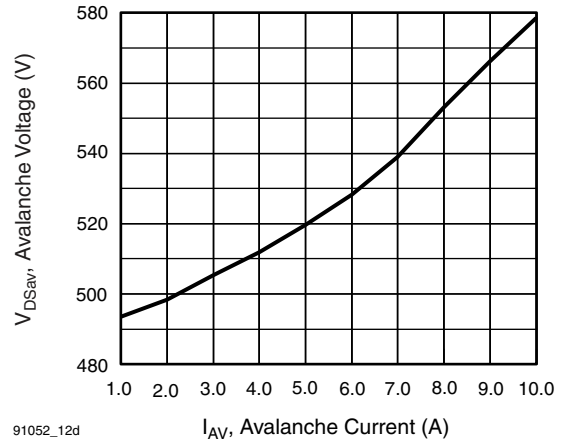


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

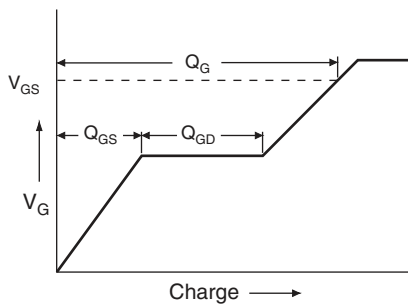


Fig. 13a - Basic Gate Charge Waveform

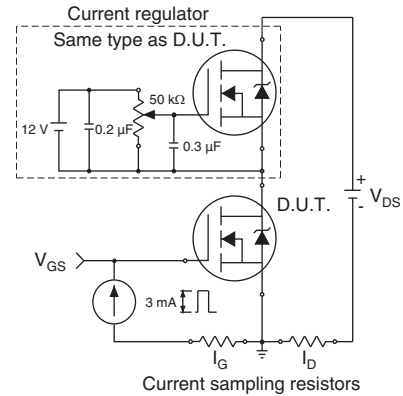
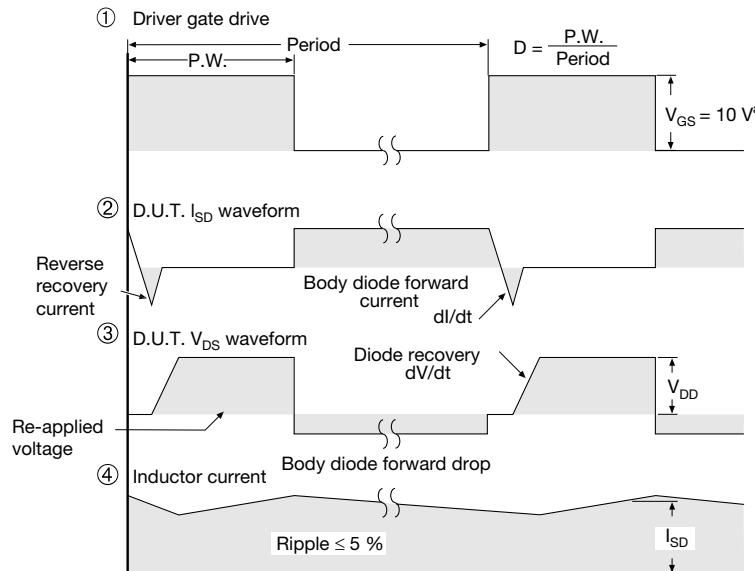


Fig. 13b - Gate Charge Test Circuit



Note
 a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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