International
IOR Rectifier

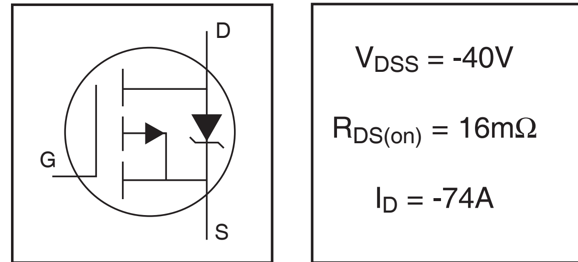
PD - 96277B

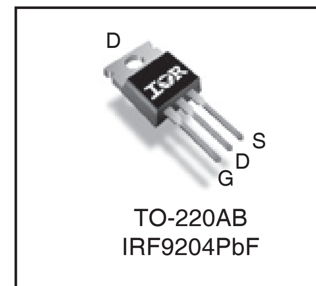
IRF9204PbF

HEXFET® Power MOSFET

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated
- Lead-Free





TO-220AB
IRF9204PbF

G	D	S
Gate	Drain	Source

Description

This HEXFET® Power MOSFET utilizes advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	-74	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	-53	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	-56	
I_{DM}	Pulsed Drain Current ①	-300	
P_D @T_C = 25°C	Power Dissipation	143	W
	Linear Derating Factor	0.95	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy②	270	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	502	
I_{AR}	Avalanche Current ①	See Fig.17a, 17b, 14, 15	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw ⑦	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	–––	1.05	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑦	0.50	–––	
$R_{\theta JA}$	Junction-to-Ambient ⑦	–––	62	

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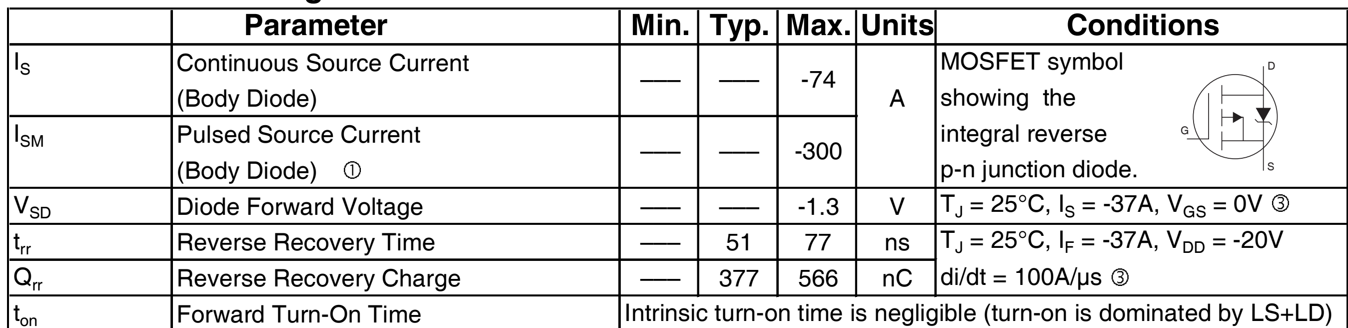
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-40	——	——	V	V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.03	——	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	16	mΩ	V_{GS} = -10V, I_D = -37A ③
		——	——	23		V_{GS} = -4.5V, I_D = -30A ③
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	-2.0	-3.0	V	V_{DS} = V_{GS}, I_D = -100μA
gfs	Forward Transconductance	29	——	——	S	V_{DS} = -10V, I_D = -37A
I_{DSS}	Drain-to-Source Leakage Current	——	——	-25	μA	V_{DS} = -40V, V_{GS} = 0V
		——	——	-250		V_{DS} = -40V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	-100	nA	V_{GS} = -20V
	Gate-to-Source Reverse Leakage	——	——	100		V_{GS} = 20V
Q_g	Total Gate Charge	——	149	224	nC	I_D = -37A
Q_{gs}	Gate-to-Source Charge	——	27	——		V_{DS} = -32V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	31	——		V_{GS} = -10V ③
$t_{d(on)}$	Turn-On Delay Time	——	27	——	ns	V_{DD} = -20V
t_r	Rise Time	——	383	——		I_D = -37A
$t_{d(off)}$	Turn-Off Delay Time	——	139	——		R_G = 7.5 Ω
t_f	Fall Time	——	153	——		V_{GS} = -10V ③
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.)
L_S	Internal Source Inductance	——	7.5	——		from package and center of die contact
C_{iss}	Input Capacitance	——	7676	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	654	——		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	——	539	——		f = 1.0KHz
C_{oss}	Output Capacitance	——	1747	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0KHz
C_{oss}	Output Capacitance	——	598	——		V_{GS} = 0V, V_{DS} = -32V, f = 1.0KHz
C_{oss} eff.	Effective Output Capacitance	——	797	——		V_{GS} = 0V, V_{DS} = 0V to -32V ④

Source-Drain Ratings and Characteristics



	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	-74	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	-300		
V_{SD}	Diode Forward Voltage	——	——	-1.3	V	T_J = 25°C, I_S = -37A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	——	51	77	ns	T_J = 25°C, I_F = -37A, V_{DD} = -20V
Q_{rr}	Reverse Recovery Charge	——	377	566	nC	di/dt = 100A/μs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.399mH R_G = 25Ω, I_{AS} = -37A, V_{GS} =-10V. Part not recommended for use above this value.

③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑤ Limited by T_{Jmax} , see Fig.17a, 17b, 14, 15 for typical repetitive avalanche performance.

⑥ This value determined from sample failure population. 100% tested to this value in production.

⑦ This is only applied to TO-220AB pakcage.

⑧ R_θ is measured at T_J approximately 90°C

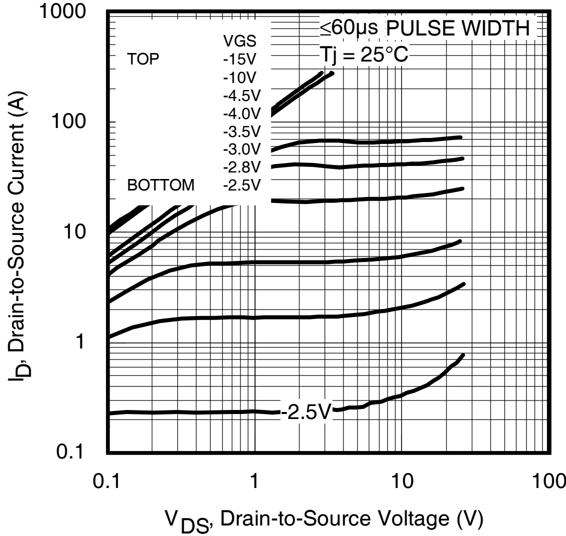


Fig 1. Typical Output Characteristics

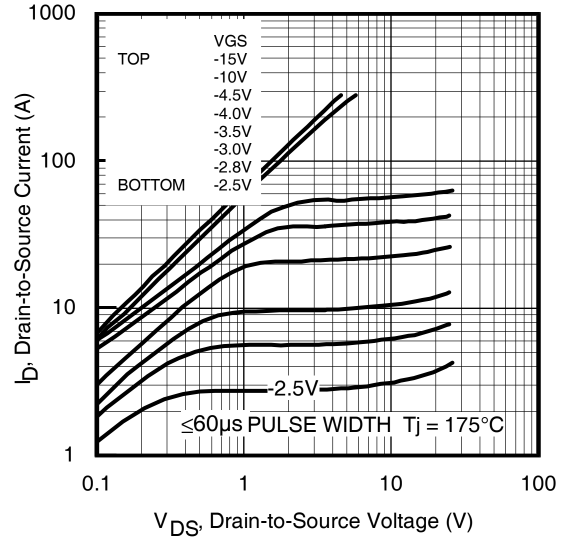


Fig 2. Typical Output Characteristics

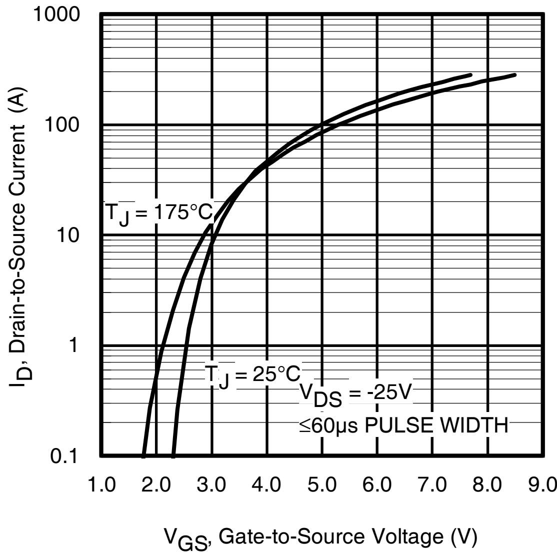


Fig 3. Typical Transfer Characteristics

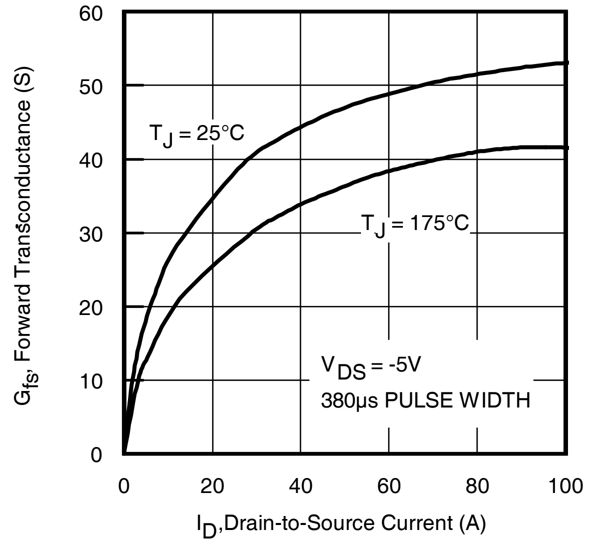


Fig 4. Typical Forward Transconductance Vs. Drain Current

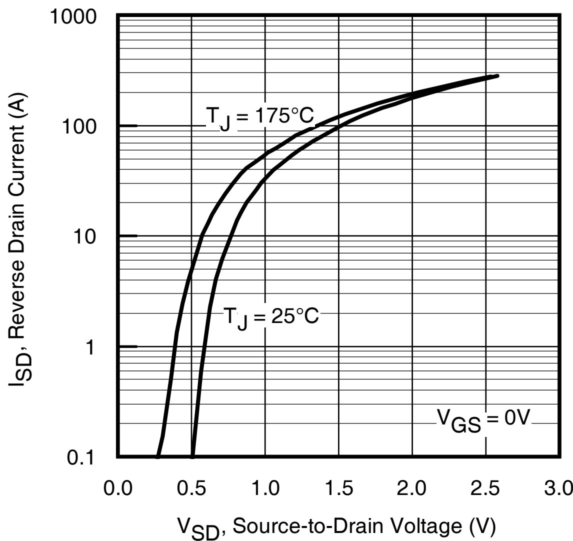


Fig 5. Typical Source-Drain Diode Forward Voltage

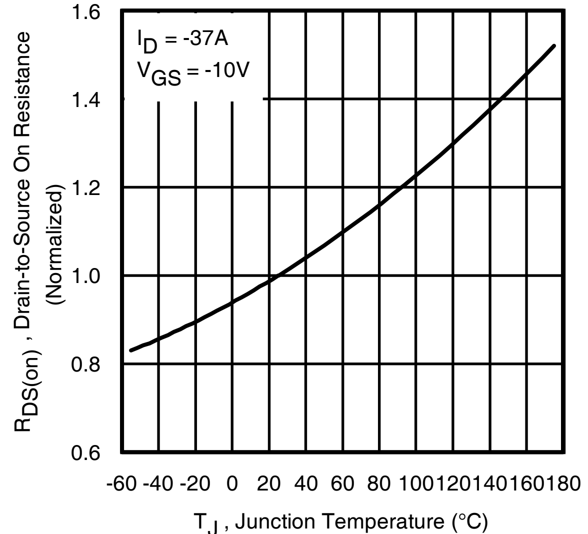


Fig 6. Normalized On-Resistance Vs. Temperature

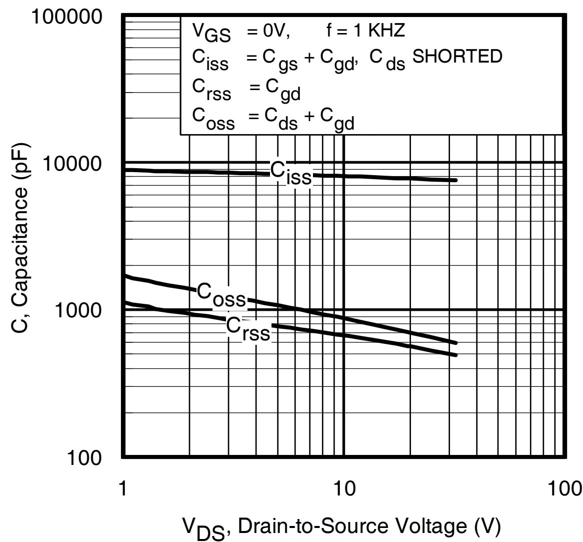


Fig 7. Typical Capacitance Vs. Drain-to-Source Voltage

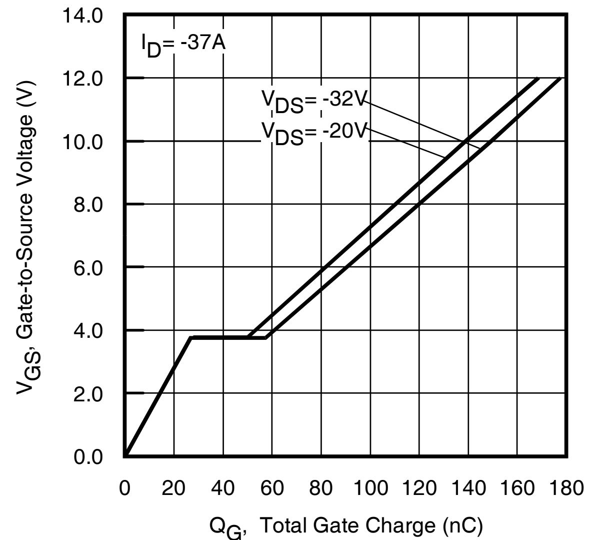


Fig 8. Typical Gate Charge Vs. Gate-to-Source Voltage

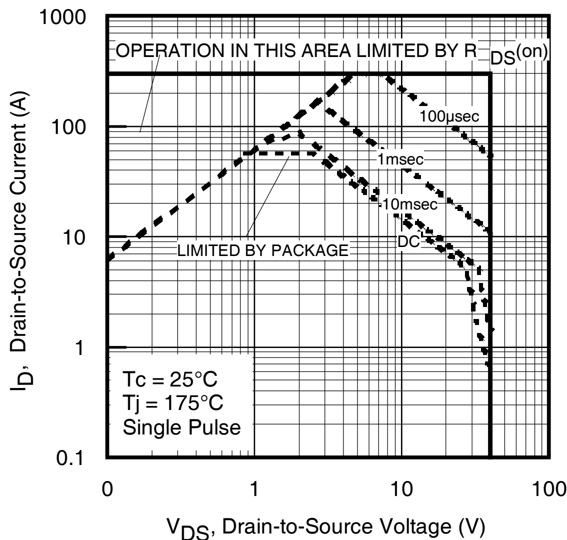


Fig 9. Maximum Safe Operating Area

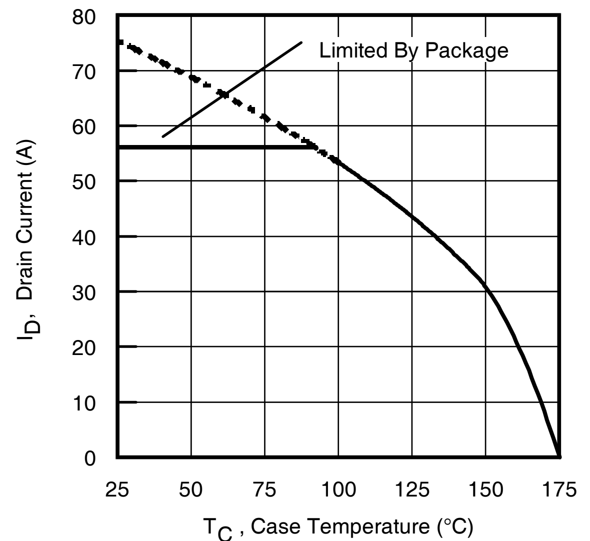


Fig 10. Maximum Drain Current Vs. Case Temperature

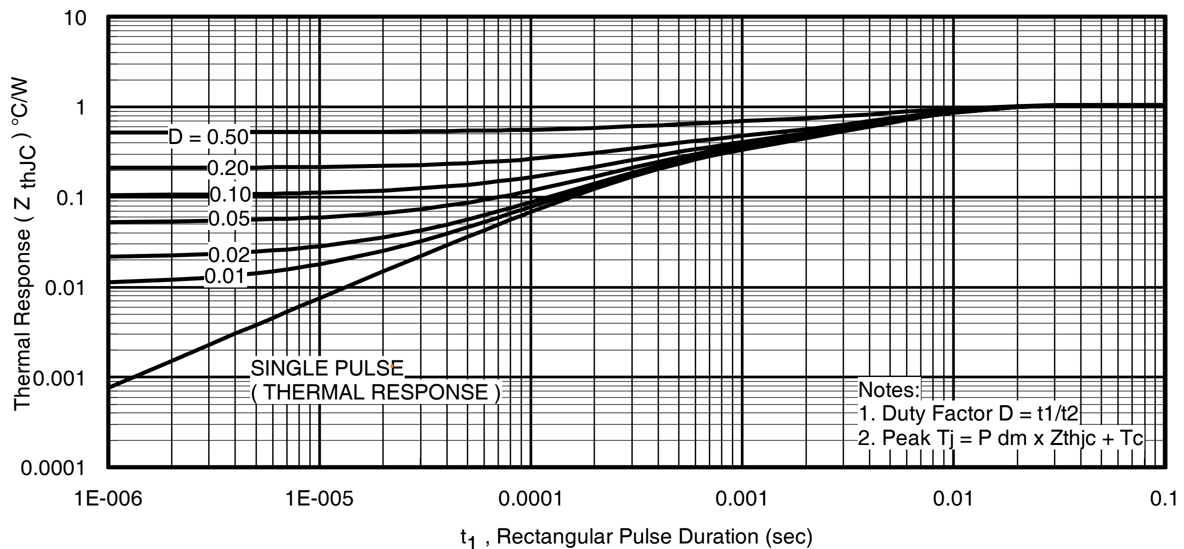


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

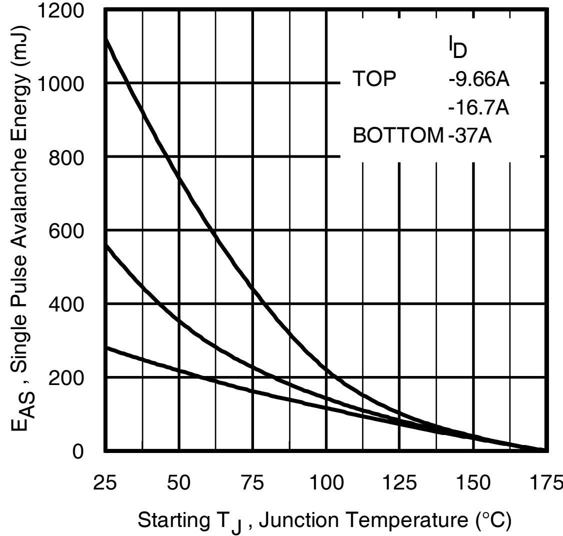


Fig 12. Maximum Avalanche Energy Vs. Drain Current

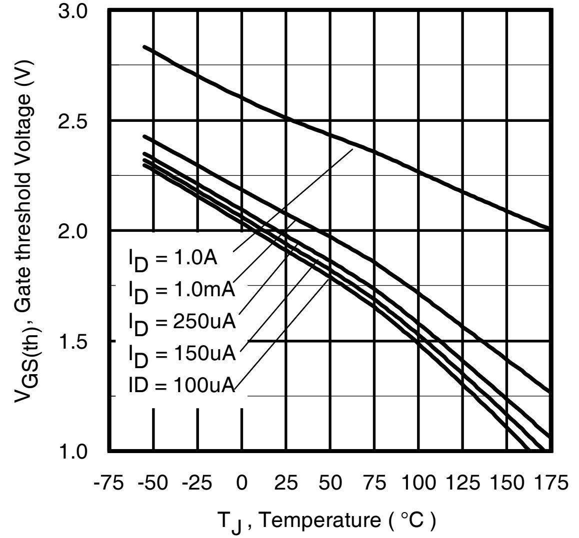


Fig 13. Threshold Voltage Vs. Temperature

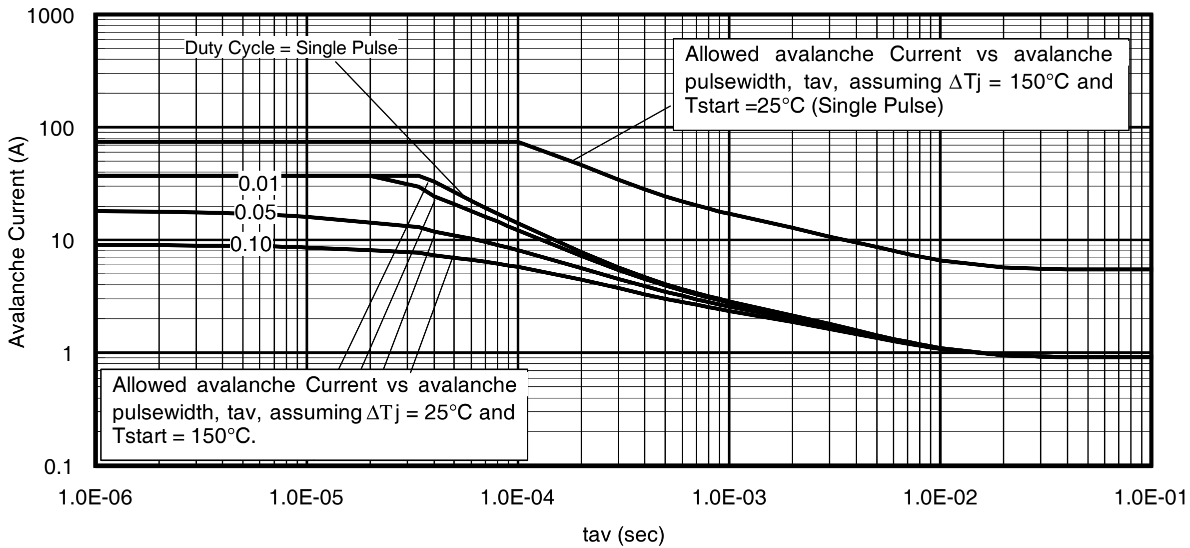


Fig 14. Typical Avalanche Current Vs.Pulsewidth

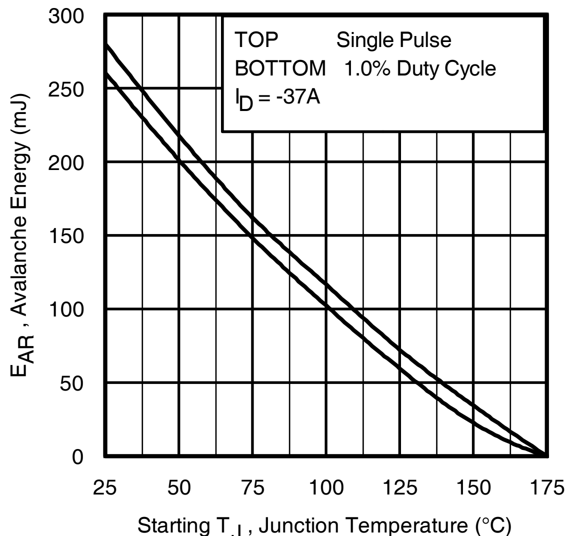
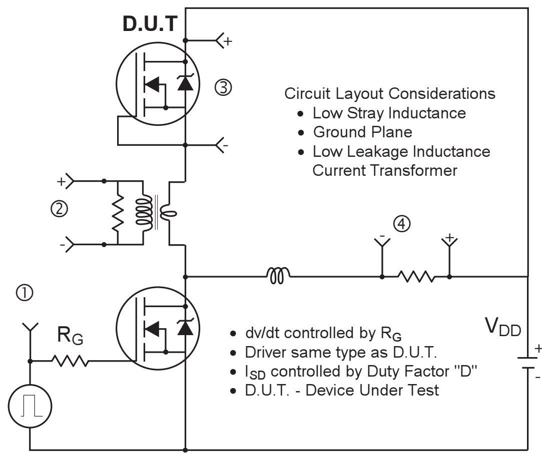


Fig 15. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 17a, 17b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$



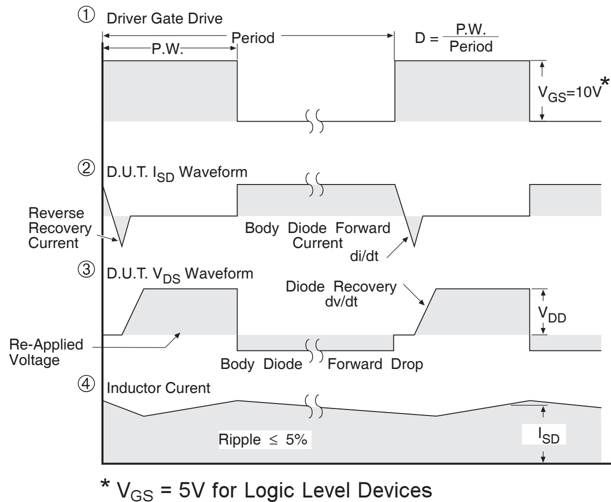


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

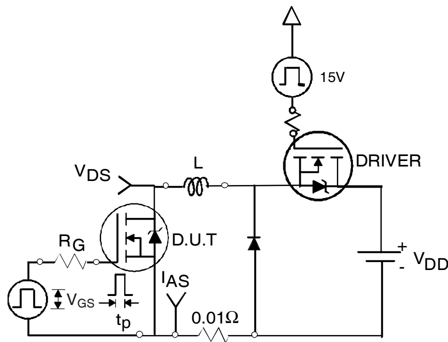


Fig 17a. Unclamped Inductive Test Circuit

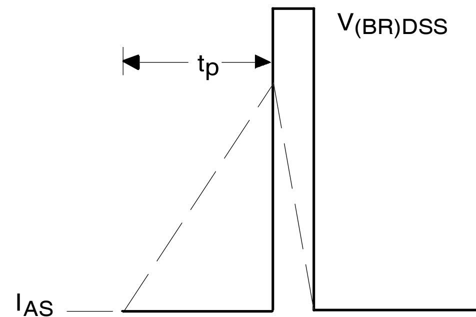


Fig 17b. Unclamped Inductive Waveforms

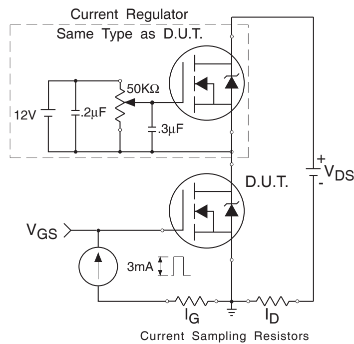


Fig 18a. Gate Charge Test Circuit

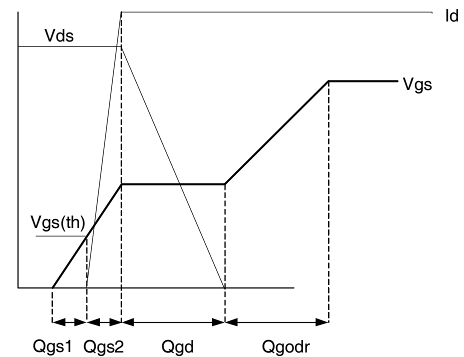


Fig 18b. Gate Charge Waveform

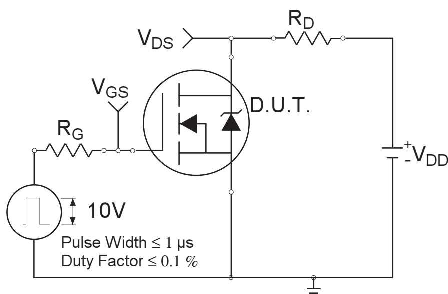


Fig 19a. Switching Time Test Circuit

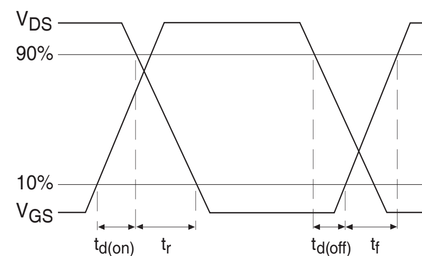
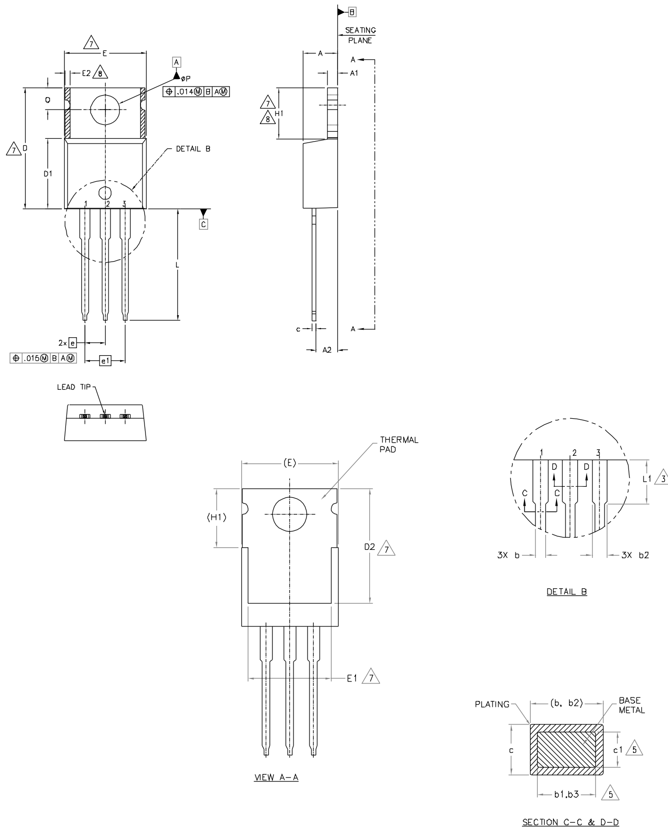


Fig 19b. Switching Time Waveforms

TO-220AB Package Outline Dimensions are shown in millimeters (inches)



NOTES:

1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
6.- CONTROLLING DIMENSION : INCHES.
7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	–	0.76	–	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
ØP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFET
1.- GATE
2.- DRAIN
3.- SOURCE

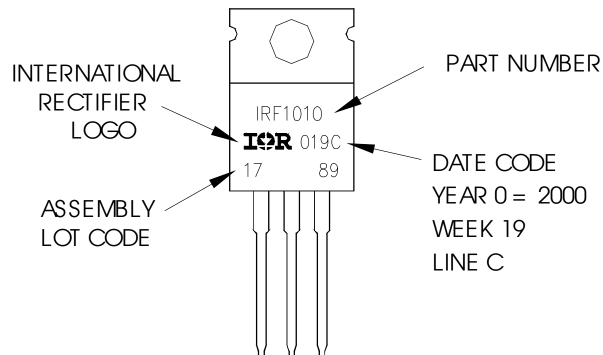
IGBTs, CoPACK
1.- GATE
2.- COLLECTOR
3.- EMITTER

DIODES
1.- ANODE
2.- CATHODE
3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Data and specifications subject to change without notice.
This product has been designed for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 101N. Sepulveda Blvd, El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
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