

Dual P-Channel HEXFET Power MOSFET in a SO-8 package

V _{DS}	-30	v
$\begin{array}{c} \textbf{R}_{DS(on)} \textbf{max} \\ (@ V_{GS} = -10V) \end{array}$	16.3	mΩ
$R_{DS(on)} max$ (@ V _{GS} = -4.5V)	23.8	mΩ
Qg (typical)	19	nC
Ι _D (@ Τ _A = 25°C)	-9.2	Α





Applications

Charge and Discharge Switch for Notebook PC Battery Application

Features and Benefits

Features	_	Benefits
Industry-Standard SO-8 Package	results in	Multi-Vendor Compatibility
RoHS Compliant Containing no Lead, no Bromide and no Halogen		Environmentally Friendlier
MSL1, Consumer Qualification		Increased Reliability

Ordorable Bart Number	Pookogo Typo	Standard	l Pack	Noto
Orderable Part Nulliber	Package Type	Form	Quantity	Note
IRF9358PbF	SO8	Tube/Bulk	95	
IRF9358TRPbF	SO8	Tape and Reel	4000	

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	-30	V
V _{GS}	Gate-to-Source Voltage	± 20	V
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ -10V	-9.2	
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ -10V	-7.3	А
I _{DM}	Pulsed Drain Current ①	-73	
P _D @ T _A = 25°C	Power Dissipation ④	2.0	14/
P _D @T _A = 70°C	Power Dissipation ④	1.3	VV
	Linear Derating Factor	0.016	W/°C
TJ	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		C



	Parameter	Min.	Тур.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-30			V	V _{GS} = 0V, I _D = -250µA
$\Delta V_{(BR)DSS} / \Delta T_J$	Breakdown Voltage Temp. Coefficient		0.02		V/°C	Reference to 25°C, I _D = -1.0mA
D	Statia Drain ta Source On Registance		13.0	16.3		V _{GS} = -10V, I _D = -9.2A ③
N DS(on)	Static Drain-to-Source On-Resistance		19.0	23.8	mc2	V _{GS} = -4.5V, I _D = -7.3A ③
V _{GS(th)}	Gate Threshold Voltage	-1.3	-1.8	-2.4	V	
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient		-5.9		mV/°C	$v_{\rm DS} = v_{\rm GS}, I_{\rm D} = -25\mu{\rm A}$
	Drain to Source Lookana Current			-1.0		$V_{DS} = -24V, V_{GS} = 0V$
IDSS	Drain-to-Source Leakage Current			-150	μΑ	V _{DS} = -24V, V _{GS} = 0V, T _J = 125°C
	Gate-to-Source Forward Leakage			-100		$V_{GS} = -20V$
I _{GSS}	Gate-to-Source Reverse Leakage			100	nA	$V_{GS} = 20V$
gfs	Forward Transconductance	23			S	V _{DS} = -10V, I _D = -7.3A
Qg	Total Gate Charge ⑥		19		nC	V _{DS} = -15V,V _{GS} = -4.5V, I _D = -7.3A
Qg	Total Gate Charge ⑥		38			I _D = -7.3A
Q_{gs}	Gate-to-Source Charge		5.8		nC	V _{DS} = -15V
Q _{gd}	Gate-to-Drain Charge®		8.9			V _{GS} = -10V
R _G	Internal Gate Resistance6		15		Ω	
t _{d(on)}	Turn-On Delay Time		5.7			V _{DD} = -15V, V _{GS} = -4.5V③
t _r	Rise Time		7.2			I _D = -1.0A
t _{d(off)}	Turn-Off Delay Time		146		ns	$R_{G} = 6.8\Omega$
t _f	Fall Time		69			See Figs. 19a &19b
C _{iss}	Input Capacitance		1740			$V_{GS} = 0V$
C _{oss}	Output Capacitance		360		pF	V _{DS} = -25V
Crss	Reverse Transfer Capacitance		240		1	f = 1.0 MHz

Electric Characteristics @ T_J = 25°C (unless otherwise specified)

Avalanche Characteristics

	Parameter	Тур.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②		210	mJ
I _{AR}	Avalanche Current ①		-7.3	A

Source - Drain Ratings and Characteristics

	Parameter	Min.	Тур.	Max.	Units	Conditions
ls	Continuous Source Current (Body Diode)			-2.0	_	MOSFET symbol showing the
I _{SM}	Pulsed Source Current (Body Diode) ①			-73		integral reverse of the second s
V _{SD}	Diode Forward Voltage			-1.2	V	T_J = 25°C, I_S = -2.0A, V_{GS} = 0V ③
t _{rr}	Reverse Recovery Time		55	83	ns	T _J = 25°C, I _F = -2.0A, V _{DD} = -24V
Q _{rr}	Reverse Recovery Charge		35	53	nC	di/dt = 100A/µs

Thermal Resistance

	Parameter	Тур.	Max.	Units
$R_{ ext{ heta}JL}$	Junction-to-Ambient S		20	°C / M
$R_{ heta JA}$	Junction-to-Ambient ④		62.5	C/W

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- $\$ Starting T_J = 25°C, L = 4.6mH, R_G = 50 Ω , I_{AS} = -6.4A.
- ③ Pulse width \leq 400µs; duty cycle \leq 2%.
- ④ When mounted on 1 inch square copper board.
- $\label{eq:R_theta}$ R_theta is measured at T_J of approximately 90°C.
- 6 For DESIGN AID ONLY, not subject to production testing.

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-V_{GS}, Gate-to-Source Voltage (V)

4

5



3

2















Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

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Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to- Ambient



Fig 12. Typical On-Resistance vs. Gate Voltage



Fig 14. Maximum Avalanche Energy vs. Drain Current



Fig 13. Typical On-Resistance vs. Drain Current





Fig 16. Peak Diode Recovery dv/dt Test Circuit for P-Channel HEXFET® Power MOSFETs





Fig 17a. Gate Charge Test Circuit



Fig 18a. Unclamped Inductive Test Circuit



Fig 17b. Basic Gate Charge Waveform



Fig 18b. Unclamped Inductive Waveform



Fig 19a. Switching Time Test Circuit



Fig 19b. Switching Time Waveforms



SO-8 Package Outline (Mosfet and Fetky)

Dimension are shown in millimeters (inches)









FOOTPRINT



- 1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
- 2. CONTROLLING DIMENSION: MILLIMETER
- 3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- 5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS.
- MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006). (6) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS.
- MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010). [7] DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO
- A SUBSTRATE.



SO-8 Part Marking Information





SO-8 Tape and Reel Information

Dimension are shown in millimeters (inches)



NOTES:

- 1. CONTROLLING DIMENSION : MILLIMETER.
- 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER. 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.



Qualification Information

Qualification level	Consumer (per JEDEC JESD47F [†] guidelines)		
Moisture Sensitivity Level	SO-8	MSL1 (per JEDEC J-STD-020D ^{†)}	
RoHS Compliant	Yes		

† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Rev.	Comments
		Update datasheet to Infineon format.
2024-10-08	2.1	 Added title" Dual P-Channel HEXFET Power MOSFET in a SO-8 package "-page1
		Added disclaimer on last page.

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