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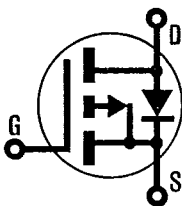
T-39-21

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HEXFET[®] TRANSISTORS IRF9630

**P-CHANNEL
200 VOLT
POWER MOSFETs**



IRF9631

IRF9632

IRF9633

-200 Volt, 0.8 Ohm HEXFET TO-220AB Plastic Package

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability. The P-Channel IRF9630 device is an approximate electrical complement to the N-Channel IRF620 HEXFET.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

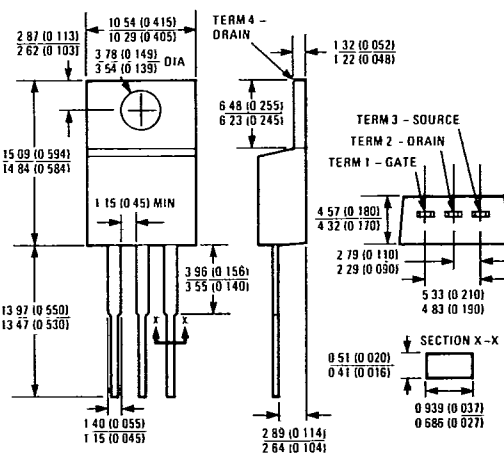
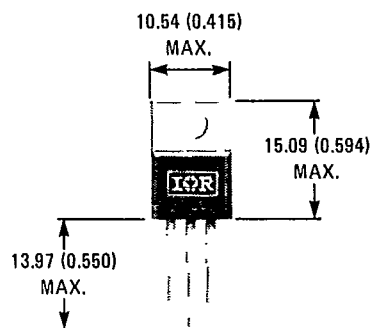
Product Summary

Part Number	V _{DS}	R _{DS(on)}	I _D
IRF9630	-200V	0.8Ω	-6.5A
IRF9631	-150V	0.8Ω	-6.5A
IRF9632	-200V	1.2Ω	-5.5A
IRF9633	-150V	1.2Ω	-5.5A

Features:

- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability

CASE STYLE AND DIMENSIONS



Case Style TO-220AB

All Dimensions in Millimeters and (Inches)

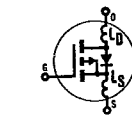
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Absolute Maximum Ratings

Parameter	IRF9630	IRF9631	IRF9632	IRF9633	Units
V_{DS} Drain - Source Voltage ①	-200	-150	-200	-150	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20\text{ k}\Omega$) ①	-200	-150	-200	-150	V
I_D @ $T_C = 25^\circ\text{C}$ Continuous Drain Current	-6.5	-6.5	-5.5	-5.5	A
I_D @ $T_C = 100^\circ\text{C}$ Continuous Drain Current	-4.0	-4.0	-3.5	-3.5	A
I_{DM} Pulsed Drain Current ③	-26	-26	-22	-22	A
V_{GS} Gate - Source Voltage	± 20				V
P_D @ $T_C = 25^\circ\text{C}$ Max. Power Dissipation	75 (See Fig. 14)				W
Linear Derating Factor	0.6 (See Fig. 14)				W/K ④
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	IRF9630 IRF9632	-200	—	—	V	$V_{GS} = 0\text{V}$
	IRF9631 IRF9633	-150	—	—	V	$I_D = -250\mu\text{A}$
$V_{GS(th)}$ Gate Threshold Voltage	ALL	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	-500	nA	$V_{GS} = -20\text{V}$
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	500	nA	$V_{GS} = 20\text{V}$
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	-250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0\text{V}$
		—	—	-1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$
$I_{D(on)}$ On-State Drain Current ②	IRF9630 IRF9631	-6.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max.}, V_{GS} = -10\text{V}$
	IRF9632 IRF9633	-5.5	—	—	A	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	IRF9630 IRF9631	—	0.5	0.8	Ω	$V_{GS} = -10\text{V}, I_D = -3.5\text{A}$
	IRF9632 IRF9633	—	0.8	1.2	Ω	
g_{fs} Forward Transconductance ②	ALL	2.2	3.5	—	S (①)	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max.}, I_D = -3.5\text{A}$
C_{iss} Input Capacitance	ALL	—	550	650	pF	$V_{GS} = 0\text{V}, V_{DS} = -25\text{V}, f = 1.0\text{ MHz}$ See Fig. 10
C_{oss} Output Capacitance	ALL	—	170	300	pF	
C_{rss} Reverse Transfer Capacitance	ALL	—	50	90	pF	$V_{DD} = 0.5 BV_{DSS}, I_D = -3.5\text{A}, Z_\theta = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
$t_{d(on)}$ Turn-On Delay Time	ALL	—	30	50	ns	
t_r Rise Time	ALL	—	50	100	ns	
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	50	100	ns	
t_f Fall Time	ALL	—	40	80	ns	$V_{GS} = -15\text{V}, I_D = -8.0\text{A}, V_{DS} = 0.8 \text{ Max. Rating.}$ See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	31	45	nC	
Q_{gs} Gate-Source Charge	ALL	—	18	—	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	13	—	nC	
L_D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.



Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	1.67	K/W ④	Mounting surface flat, smooth, and greased.
R_{thCS} Case-to-Sink	ALL	—	1.0	—	K/W ④	
R_{thJA} Junction-to-Ambient	ALL	—	—	80	K/W ④	Typical socket mount

IRF9630, IRF9631, IRF9632, IRF9633 Devices

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Source-Drain Diode Ratings and Characteristics

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I_S	Continuous Source Current (Body Diode)	IRF9630 IRF9631	—	—	-6.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF9632 IRF9633	—	—	-5.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9630 IRF9631	—	—	-26	A	
		IRF9632 IRF9633	—	—	-22	A	
V_{SD}	Diode Forward Voltage ②	IRF9630 IRF9631	—	—	-6.5	V	$T_C = 25^\circ\text{C}, I_S = -6.5\text{A}, V_{GS} = 0\text{V}$
		IRF9632 IRF9633	—	—	-6.3	V	$T_C = 25^\circ\text{C}, I_S = -5.5\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	400	—	ns	$T_J = 150^\circ\text{C}, I_F = -6.5\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.6	—	μC	$T_J = 150^\circ\text{C}, I_F = -6.5\text{A}, di/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

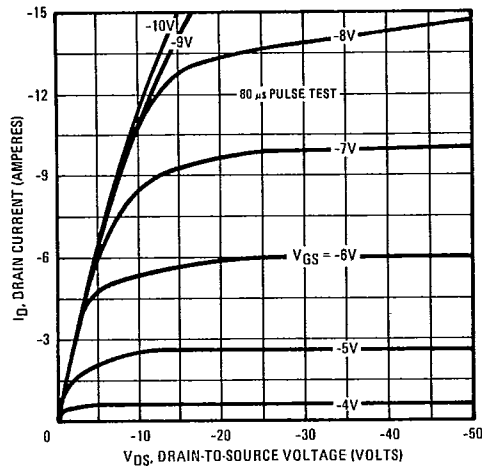
① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.④ $K/W = ^\circ\text{C}/\text{W}$
 $W/K = \text{W}/^\circ\text{C}$ ③ Repetitive Rating: Pulse width limited by max. junction temperature.
See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 - Typical Output Characteristics

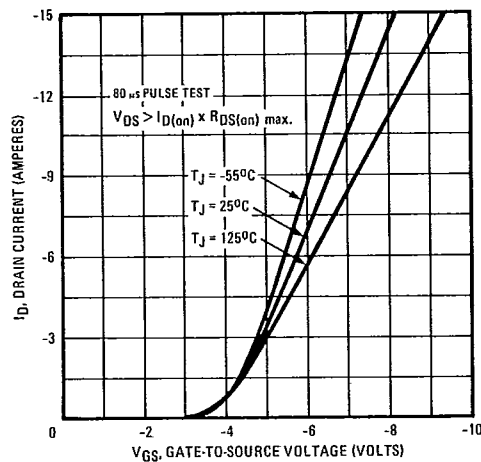


Fig. 2 - Typical Transfer Characteristics

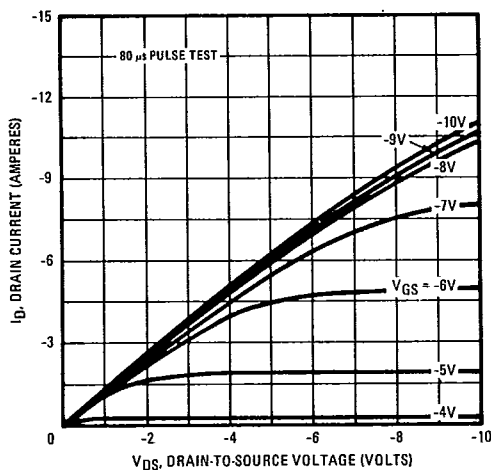


Fig. 3 - Typical Saturation Characteristics

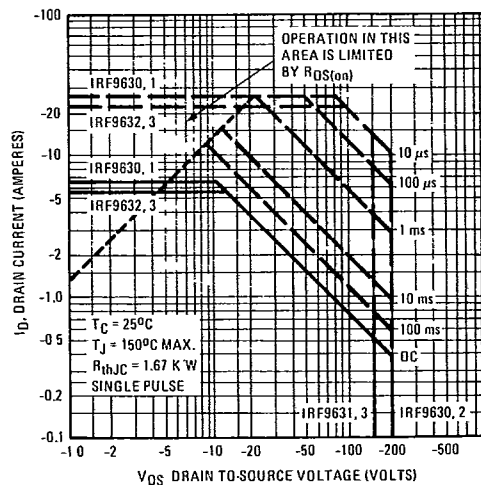


Fig. 4 - Maximum Safe Operating Area

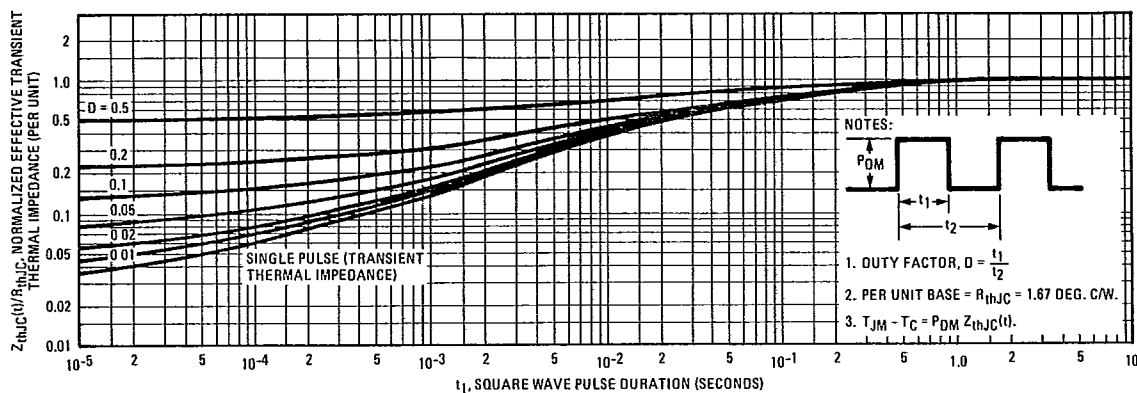


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

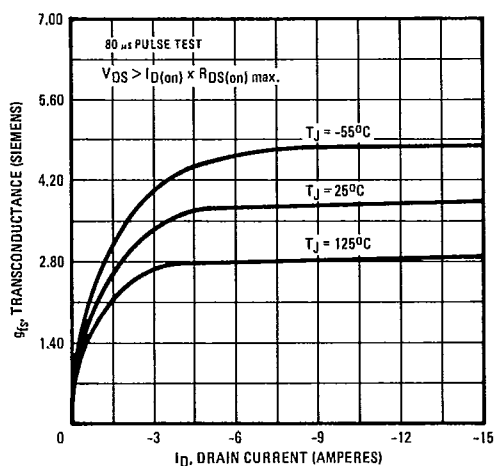


Fig. 6 — Typical Transconductance Vs. Drain Current

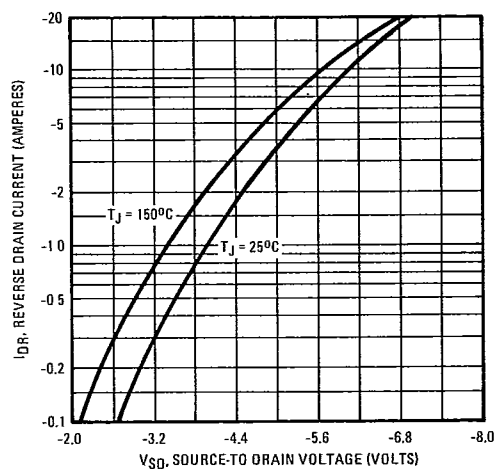


Fig. 7 — Typical Source-Drain Diode Forward Voltage

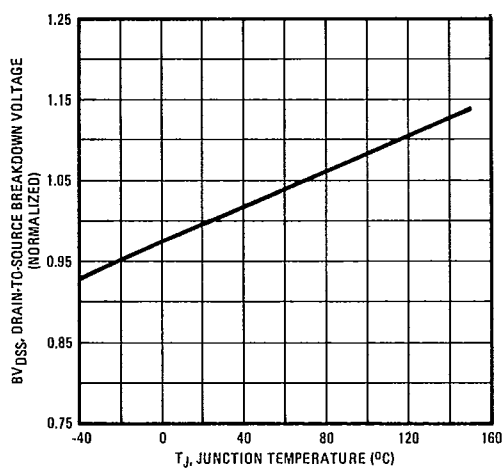


Fig. 8 — Breakdown Voltage Vs. Temperature

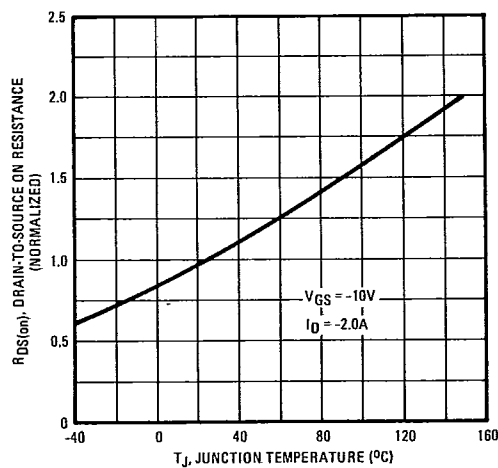


Fig. 9 — Normalized On-Resistance Vs. Temperature

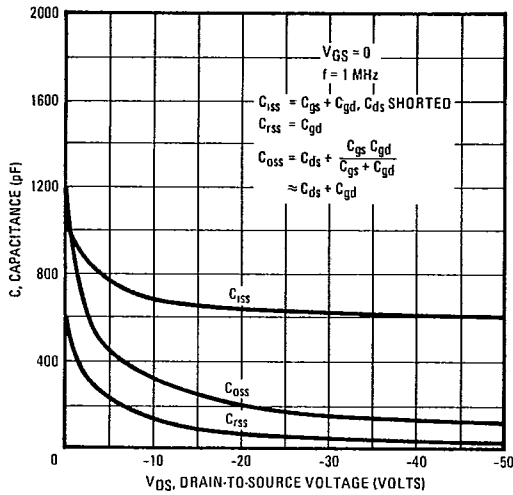


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

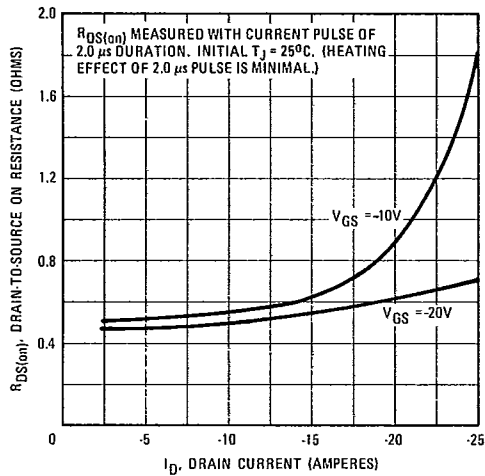


Fig. 12 — Typical On-Resistance Vs. Drain Current

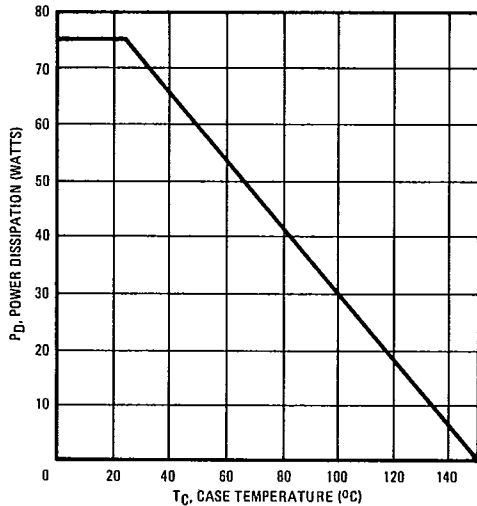


Fig. 14 — Power Vs. Temperature Derating Curve

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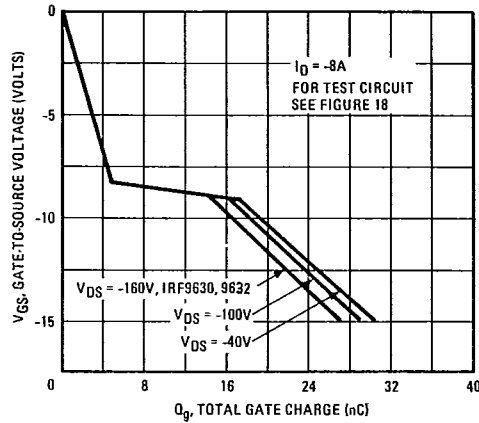


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

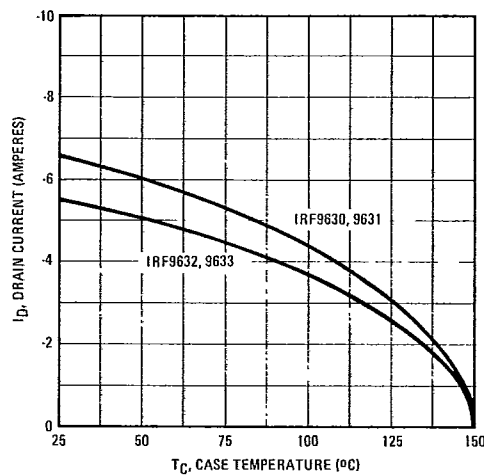


Fig. 13 — Maximum Drain Current Vs. Case Temperature

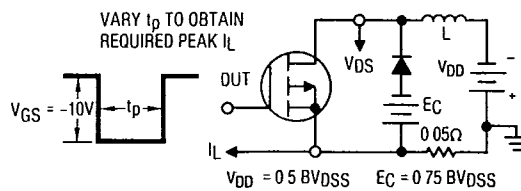


Fig. 15 — Clamped Inductive Test Circuit

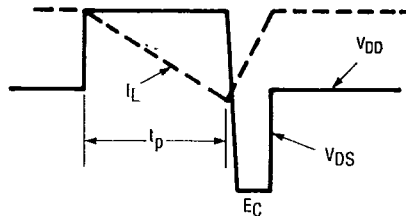


Fig. 16 — Clamped Inductive Waveforms

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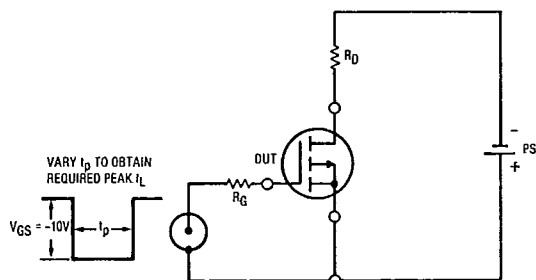


Fig. 17 — Switching Time Test Circuit

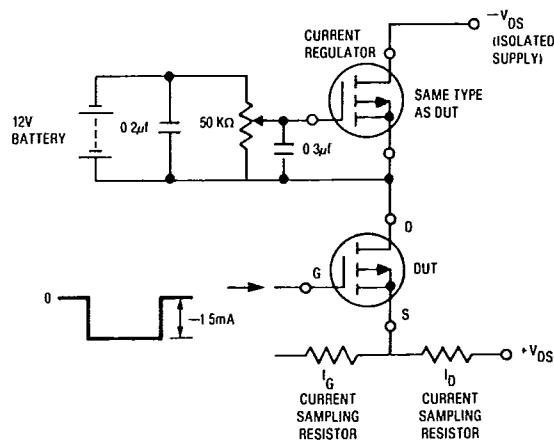
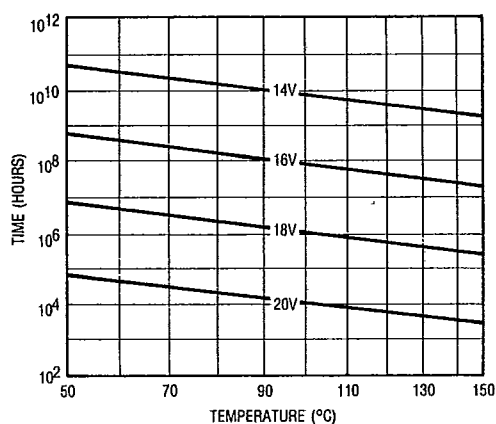
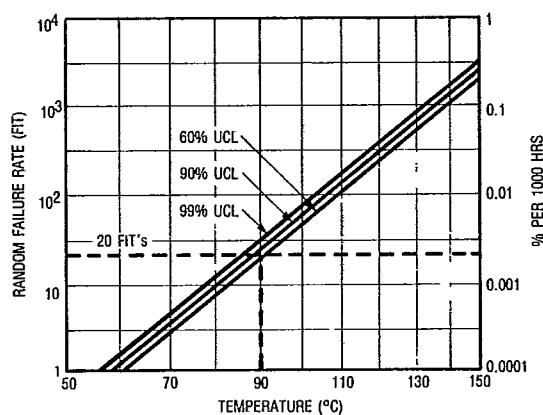


Fig. 18 — Gate Charge Test Circuit



*Fig. 19 — Typical Time to Accumulated 1% Failure



*Fig. 20 — Typical High Temperature Reverse Bias (HTRB) Failure Rate

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.