

IRF9Z30PbF

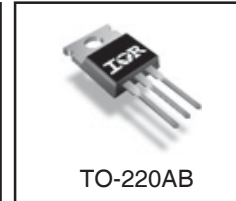
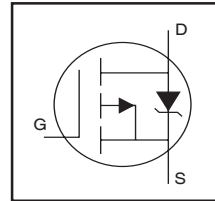
HEXFET® POWER MOSFET

Features

- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability
- Lead-Free

Product Summary

Part Number	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
IRF9Z30PbF	-50	0.14	-18



Description

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuit and pulse amplifiers.

Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage ①	-50	V
V _{DGR}	Drain-to-Gate Voltage (R _{GS} = 20KΩ) ①	-50	
V _{GS}	Gate-to-Source Voltage	±20	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS}	-18	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS}	-11	
I _{DM}	Pulsed Drain Current ②	-60	
P _D @ T _C = 25°C	Max. Power Dissipation	74	W
	Linear Derating Factor	0.59	W/°C
I _{LM}	Inductive Current, Clamped (L= 100μH) See Fig. 14	-60	A
I _L	Unclamped Inductive Current(Avalanche Current) ③ See Fig. 15	-3.1	
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	---	1.7	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	1.0	---	
R _{θJA}	Junction-to-Ambient	---	80	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-50	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-500	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	500		$V_{GS} = 20V$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0V$
		—	—	-1000		$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{D(on)}$	On- State Drain Current ④	-18	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ (max)., $V_{GS} = -10V$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance④	—	0.093	0.14	Ω	$V_{GS} = -10V, I_D = -9.3A$
g_{fs}	Forward Transconductance④	3.1	4.7	—	S	$V_{DS} = 2 \times V_{GS}, I_{DS} = -9.0A$
C_{iss}	Input Capacitance	—	900	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	570	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	140	—		$f = 1.0\text{MHz}$, See Fig.10
$t_{d(on)}$	Turn-On Delay Time	—	12	18	ns	$V_{DD} = -25V, I_D = -18A, R_G = 13\Omega, R_D = 1.3\Omega$ See Fig.16 (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	110	170		
$t_{d(off)}$	Turn-Off Delay Time	—	21	32		
t_f	Fall Time	—	64	96		
Q_g	Total Gate Charge (Gate -Source Plus Gate-Drain)	—	26	39		
Q_{gs}	Post-Vth Gate-to-Source Charge	—	6.9	10	nC	$V_{GS} = -10V, I_D = -18A, V_{DS} = 0.8 \text{ Max. Rating}$ See Fig.17 for test circuit (Gate charge is essentially independent of operating temperature.)
Q_{gd}	Gate-to-Drain Charge	—	9.7	15		
L_D	Internal Drain Inductance	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad. Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	—	7.5	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-18	A	MOSFET symbol showing the integral reverse p-n junction rectifier.
I_{SM}	Pulsed Source Current (Body Diode) ③	—	—	-60		
V_{SD}	Diode Forward Voltage ②	—	—	-6.3	V	$T_J = 25^\circ\text{C}, I_S = -18A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	54	120	250	ns	$T_J = 25^\circ\text{C}, I_F = -18A$
Q_{rr}	Reverse Recovery Charge	0.20	0.47	1.1	μC	$di/dt = 100A/\mu s$
T_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Note:

- ① $T_J = 25^\circ\text{C}$ to 150°C
- ② Repetitive Rating :Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig.5).
- ③ @ $V_{ds} = -25V, T_J = 25^\circ\text{C}, L = 100\mu H, R_G = 25\Omega$.
- ④ Pulse Test : Pulse width $\leq 300\text{ms}$, Duty Cycle $\leq 2\%$.

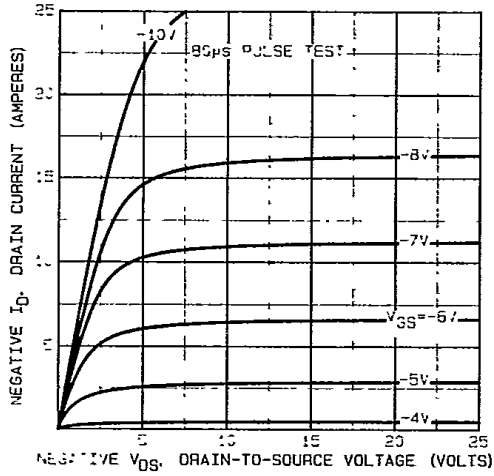


Fig. 1 — Typical Output Characteristics

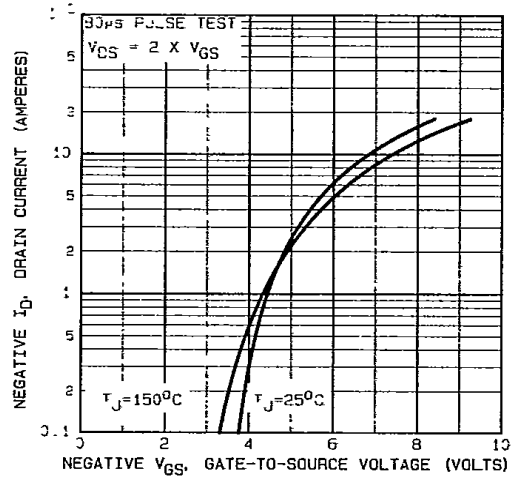


Fig. 2 — Typical Transfer Characteristics

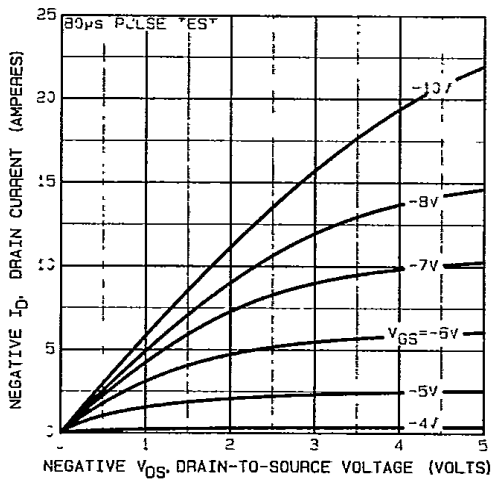


Fig. 3 — Typical Saturation Characteristics

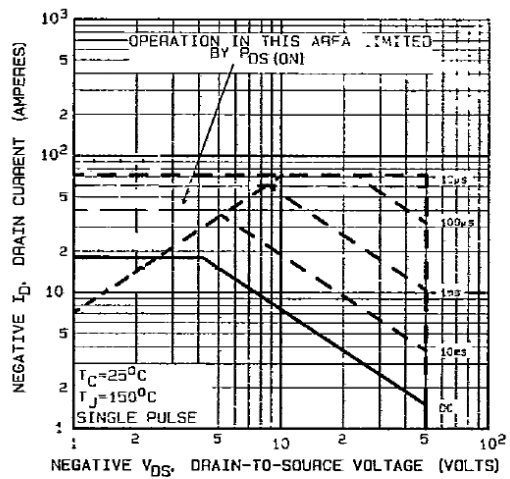


Fig. 4 — Maximum Safe Operating Area

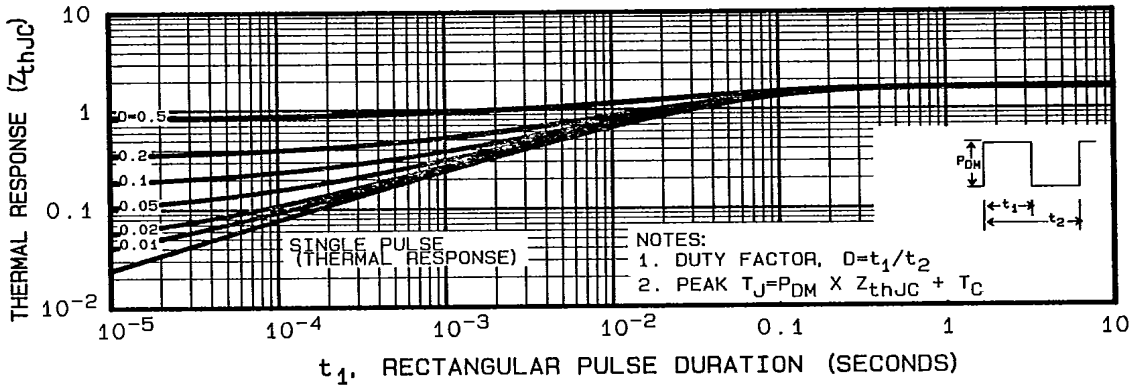


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

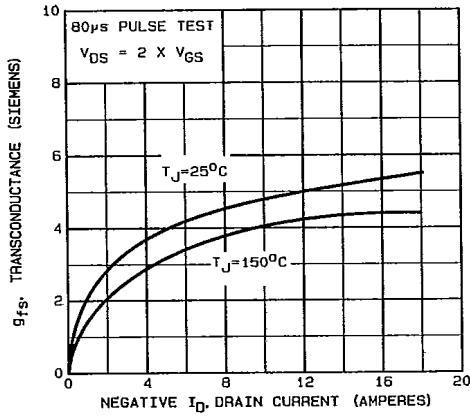


Fig. 6 — Typical Transconductance Vs. Drain Current

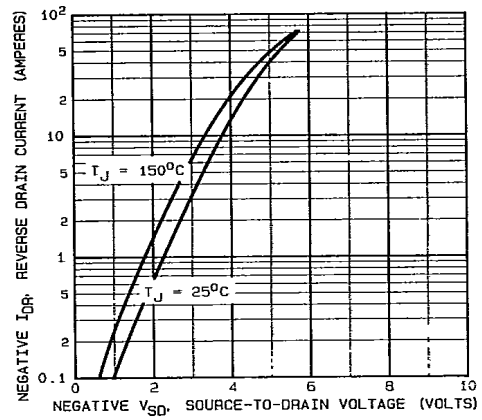


Fig. 7 — Typical Source-Drain Diode Forward Voltage

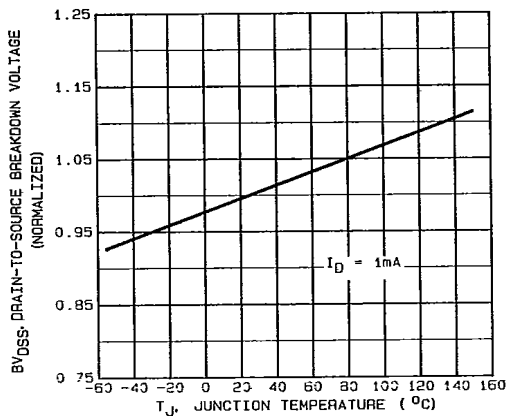


Fig. 8 — Breakdown Voltage Vs. Temperature

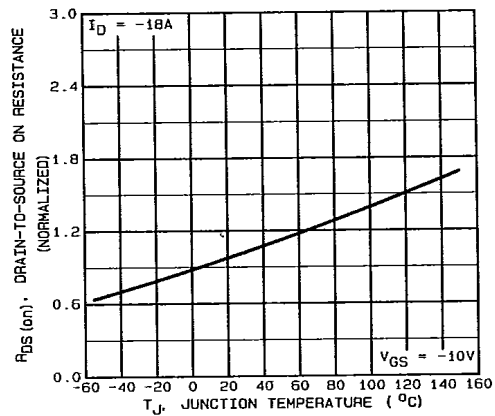


Fig. 9 — Normalized On-Resistance Vs. Temperature

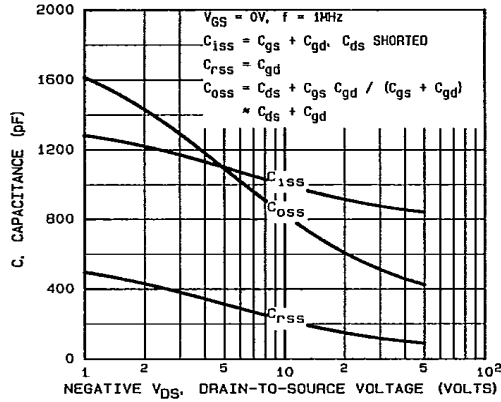


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

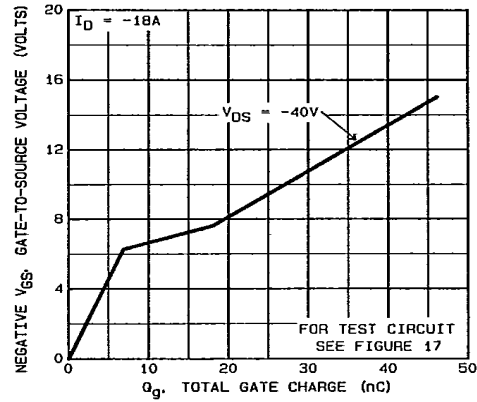


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

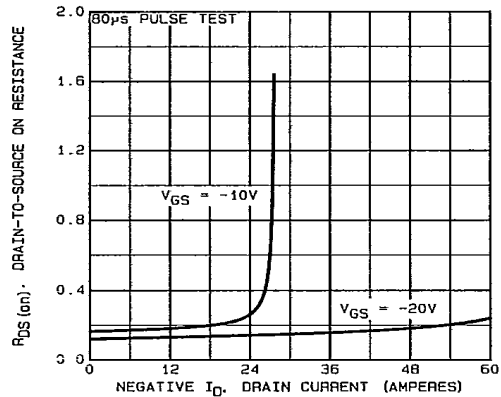


Fig. 12 — Typical On-Resistance Vs. Drain Current

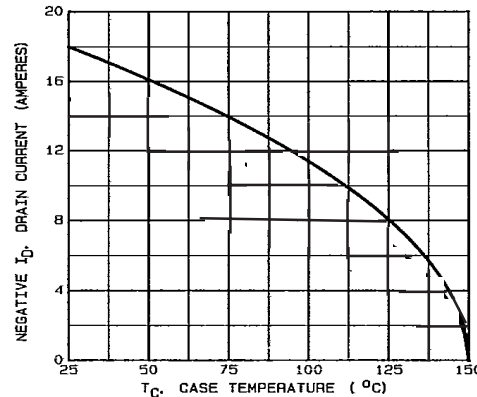


Fig. 13 — Maximum Drain Current Vs. Case Temperature

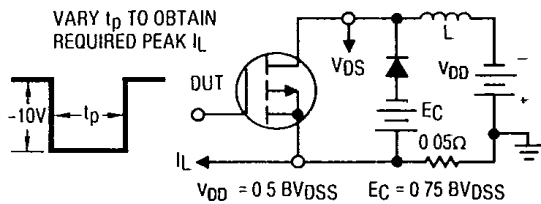


Fig. 14a — Clamped Inductive Test Circuit

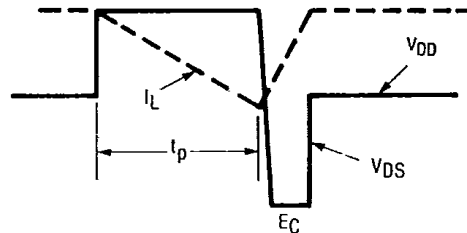


Fig. 14b — Clamped Inductive Waveforms

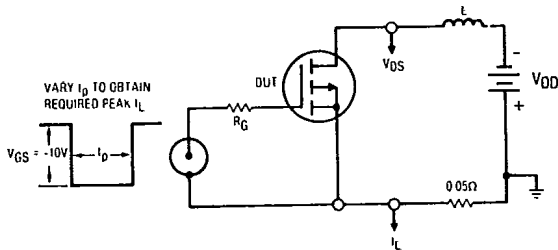


Fig. 15a — Unclamped Inductive Test Circuit

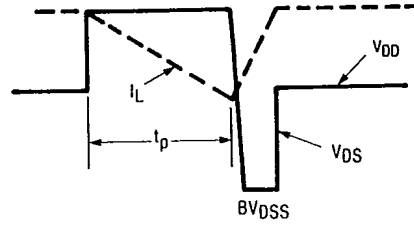


Fig. 15b — Unclamped Inductive Load Test Waveforms

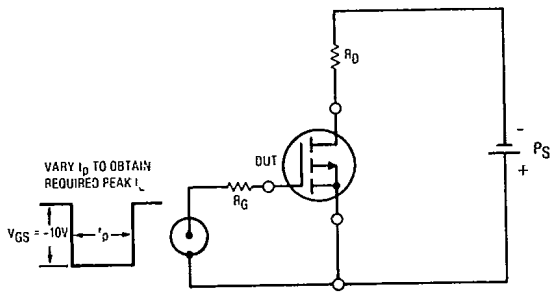


Fig. 16 — Switching Time Test Circuit

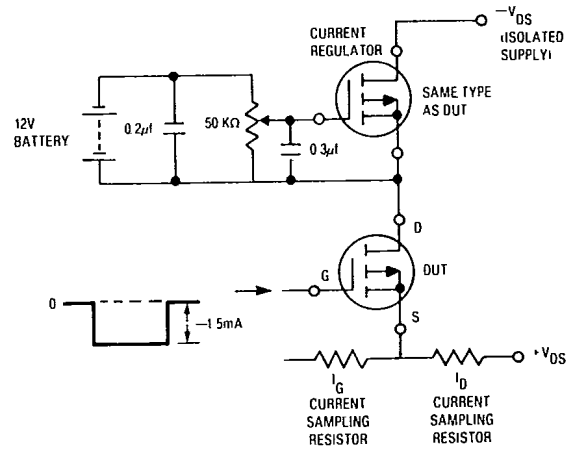
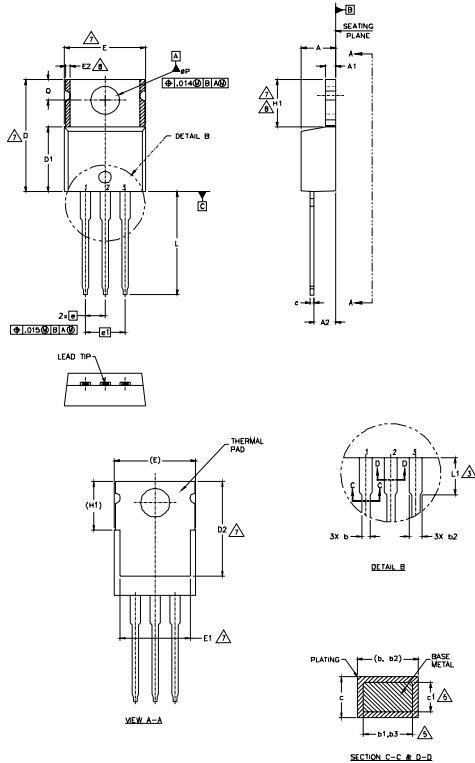


Fig. 17 — Gate Charge Test Circuit

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	5
b1	0.38	0.97	.015	.038	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	-	6.35	-	.250	3
φP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFLET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs_CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

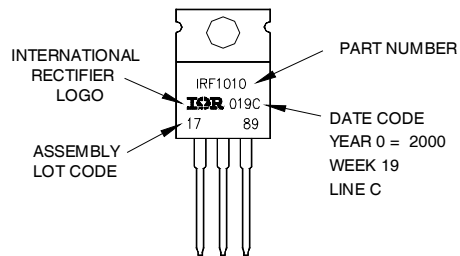
DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.