

REPETITIVE AVALANCHE AND dv/dt RATED HEXFET[®] TRANSISTORS THRU-HOLE (TO-204AA/AE)

IRFAE40 800V, N-CHANNEL

Product Summary

Part Number	BVDSS	RDS(on)	Id
IRFAE40	800V	2.0Ω	4.8A

The HEXFET[®] technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.



TO-3

Features:

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Hermetically Sealed
- Simple Drive Requirements
- Ease of Paralleling

Absolute Maximum Ratings

	Parameter		Units
Id @ VGS = 0V, TC = 25°C	Continuous Drain Current	4.8	A
Id @ VGS = 0V, TC = 100°C	Continuous Drain Current	3.0	
IDM	Pulsed Drain Current ①	19	
PD @ TC = 25°C	Max. Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	550	mJ
IAR	Avalanche Current ①	4.8	A
EAR	Repetitive Avalanche Energy ①	12.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.0	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	11.5(typical)	g

For footnotes refer to the last page

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	800	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.98	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	2.0	Ω	V _{GS} = 10V, I _D = 3.0A ④
		—	—	2.3		V _{GS} = 10V, I _D = 4.8A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	3.9	—	—	S (S)	V _{DS} > 15V, I _{DS} = 3.0A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V _{DS} =640V, V _{GS} =0V
		—	—	250		V _{DS} = 640V V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	48	—	110	nC	V _{GS} = 10V, I _D =4.8A V _{DS} =400V
Q _{gs}	Gate-to-Source Charge	5.3	—	12		
Q _{gd}	Gate-to-Drain (‘Miller’) Charge	30	—	68		
t _{d(on)}	Turn-On Delay Time	—	—	24	n s	V _{DD} =400V, I _D =4.8A, R _G =9.1Ω
t _r	Rise Time	—	—	42		
t _{d(off)}	Turn-Off Delay Time	—	—	170		
t _f	Fall Time	—	—	44		
L _S + L _D	Total Inductance	—	6.1	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
C _{iss}	Input Capacitance	—	1700		pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{Oss}	Output Capacitance	—	230	—		
C _{rss}	Reverse Transfer Capacitance	—	96	—		

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	4.8	A	T _j = 25°C, I _S = 4.8A, V _{GS} = 0V ④
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	19		
V _{SD}	Diode Forward Voltage	—	—	1.8	V	
t _{rr}	Reverse Recovery Time	—	—	1300	nS	T _j = 25°C, I _F = 4.8A, di/dt ≤ 100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	8.5	μC	V _{DD} ≤ 50V ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction to Case	—	—	1.0	°C/W	
R _{thJA}	Junction to Ambient	—	—	30		Typical socket mount

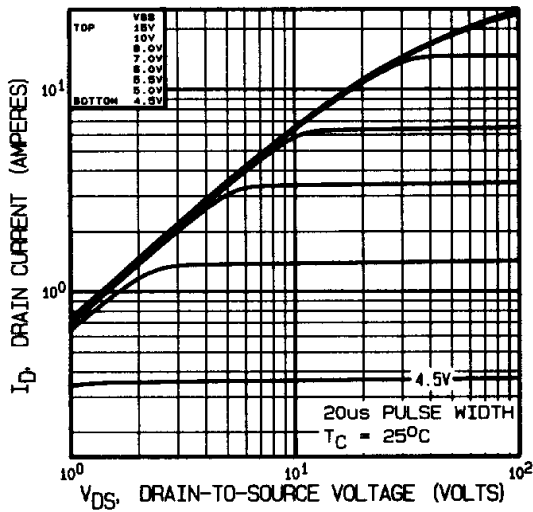


Fig 1. Typical Output Characteristics

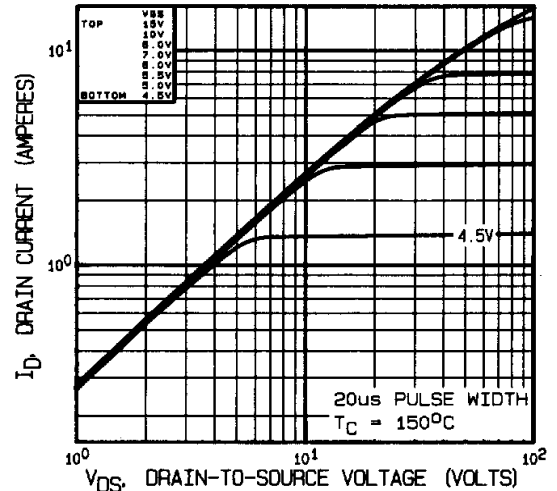


Fig 2. Typical Output Characteristics

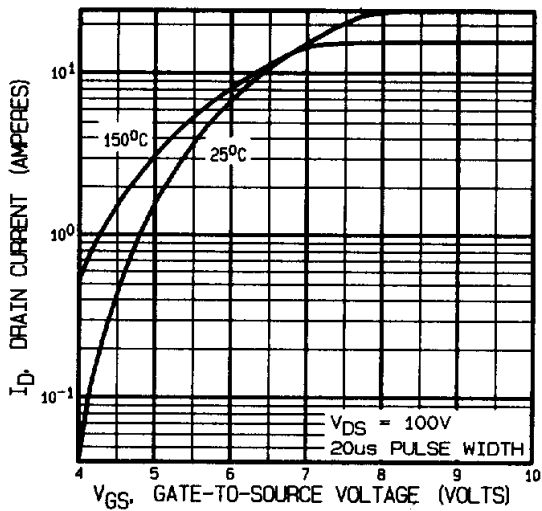


Fig 3. Typical Transfer Characteristics

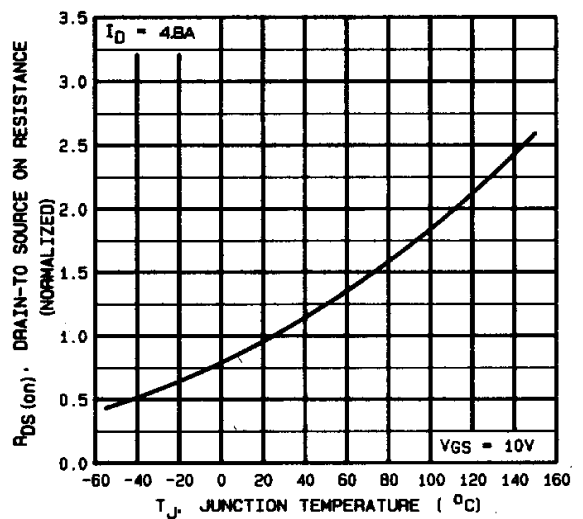


Fig 4. Normalized On-Resistance
Vs. Temperature

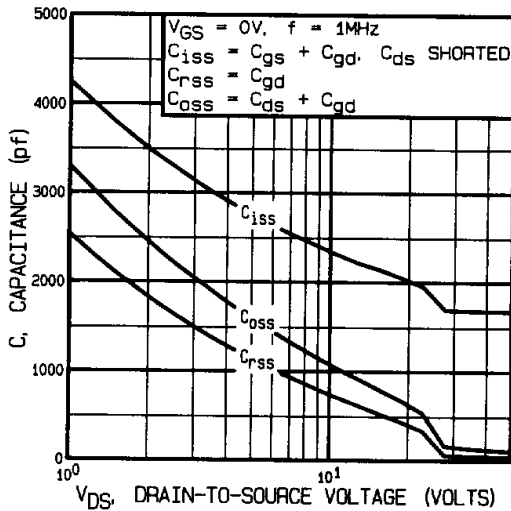


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

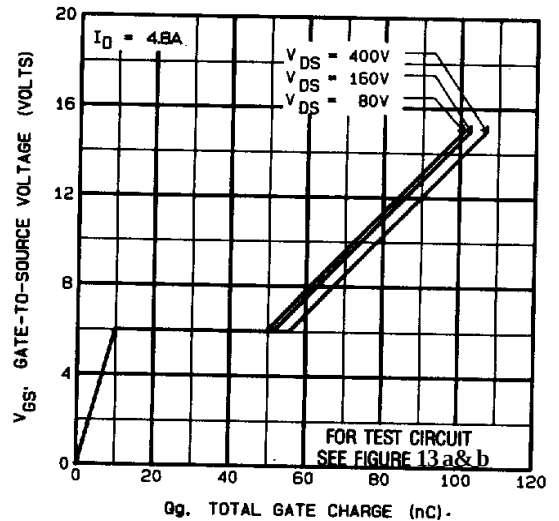


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

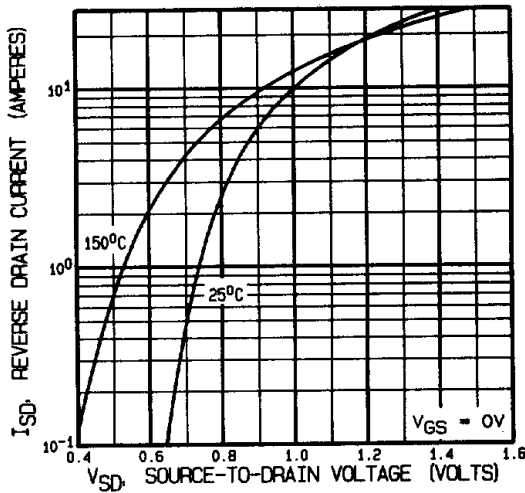


Fig 7. Typical Source-Drain Diode Forward Voltage

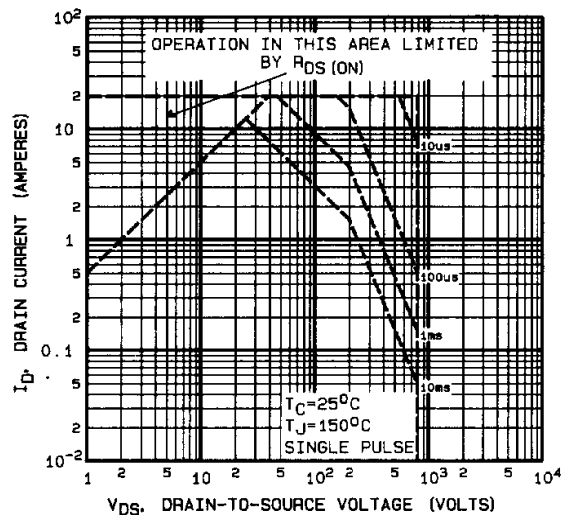


Fig 8. Maximum Safe Operating Area

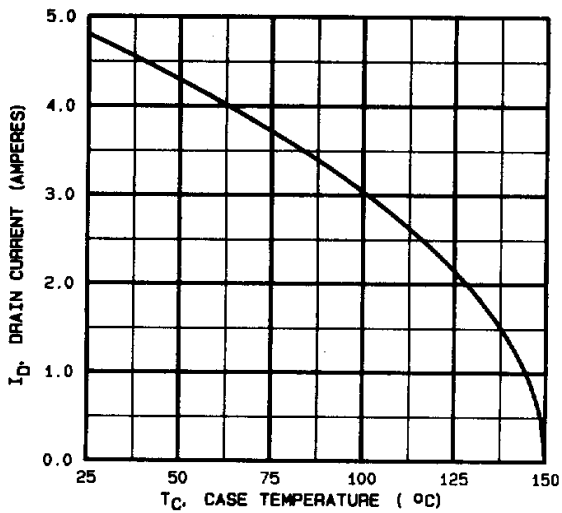


Fig 9. Maximum Drain Current Vs. Case Temperature

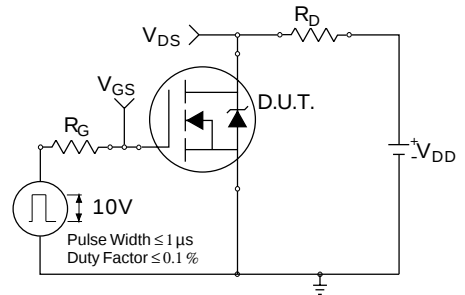


Fig 10a. Switching Time Test Circuit

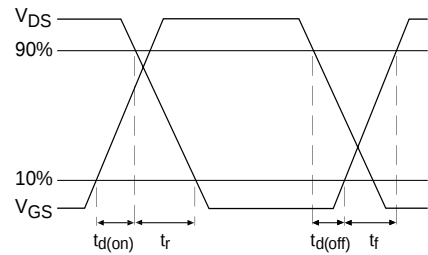


Fig 10b. Switching Time Waveforms

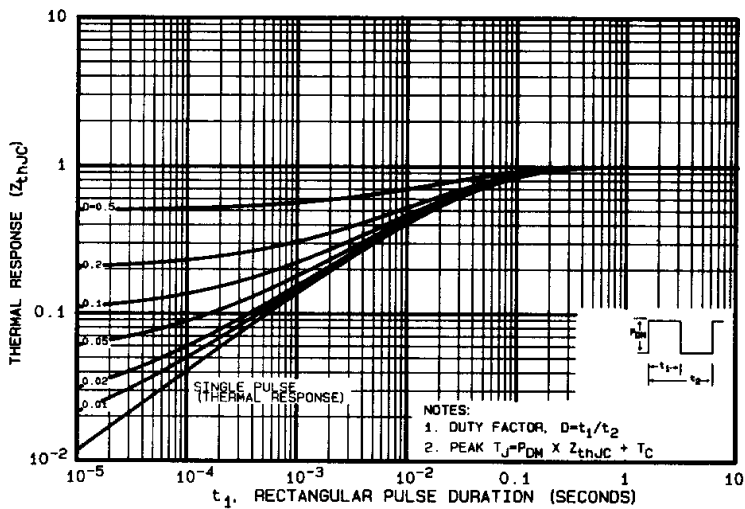


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

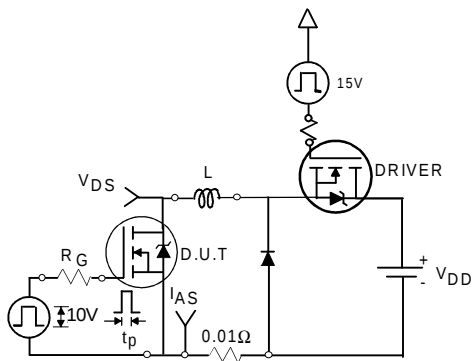


Fig 12a. Unclamped Inductive Test Circuit

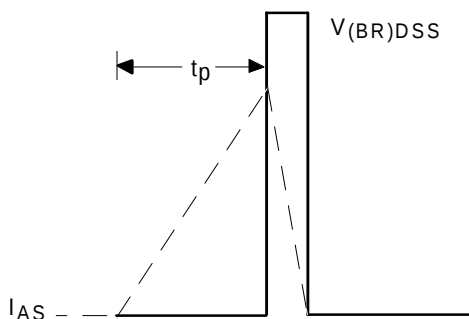


Fig 12b. Unclamped Inductive Waveforms

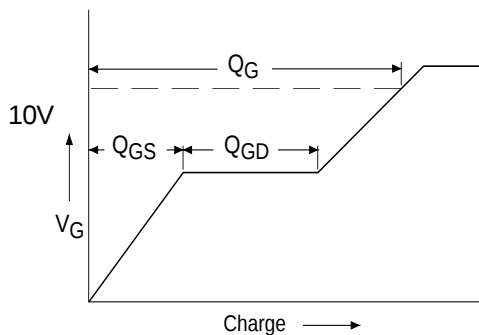


Fig 13a. Basic Gate Charge Waveform

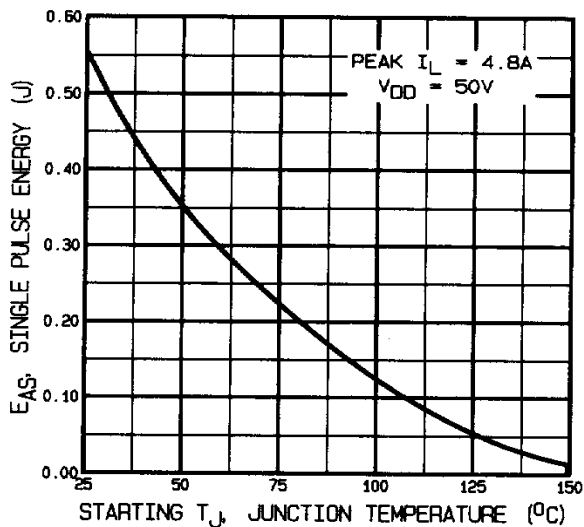
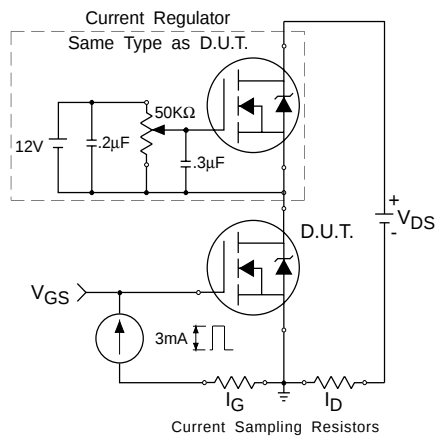
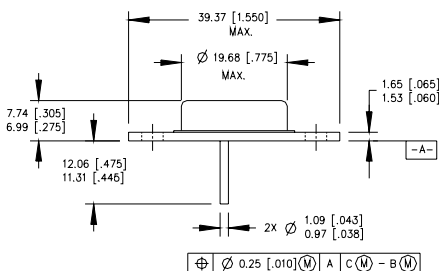
Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

Fig 13b. Gate Charge Test Circuit

Foot Notes:

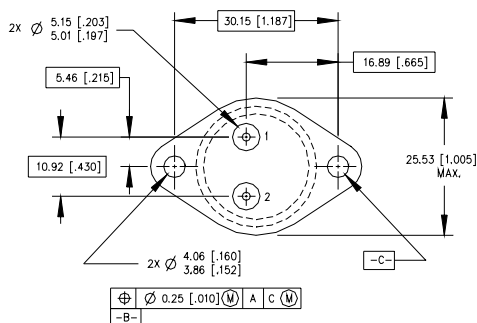
- | | |
|---|--|
| <p>① Repetitive Rating; Pulse width limited by maximum junction temperature.</p> <p>② $V_{DD} = 50V$, starting $T_J = 25^{\circ}C$,
Peak $I_L = 4.8A$,</p> | <p>③ $I_{SD} \leq 4.8A$, $di/dt \leq 120A/\mu s$,
$V_{DD} \leq 800V$, $T_J \leq 150^{\circ}C$
Suggested $R_G = 9.1\ \Omega$</p> |
|---|--|

Case Outline and Dimensions —TO-204AA (Modified TO-3)



PIN ASSIGNMENTS

HEXFET	SCHOTTKY	IGBT
1 - SOURCE	1 - ANODE 1	1 - GATE
2 - GATE	2 - ANODE 2	2 - EMITTER
3 - DRAIN (CASE)	3 - COMMON CATHODE (CASE)	3 - COLLECTOR (CASE)



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-204-AA.

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IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
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Data and specifications subject to change without notice.1/01