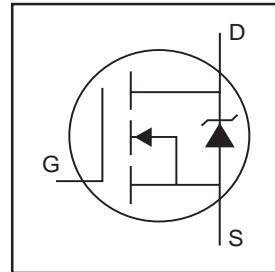


IRFB9N30APbF

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paraleling
- Dynamic dv/dt Rated
- Simple Drive Requirements
- Lead-Free

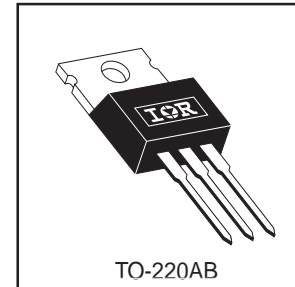


$V_{DSS} = 300V$
$R_{DS(on)} = 0.45\Omega$
$I_D = 9.3A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at lower dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	9.3	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	5.9	
I_{DM}	Pulsed Drain Current ①	37	
$P_D @ T_C = 25^\circ C$	Power Dissipation	96	W
	Linear Derating Factor	0.77	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy②	160	mJ
I_{AR}	Avalanche Current①	9.3	A
E_{AR}	Repetitive Avalanche Energy①	9.6	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.6	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

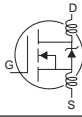
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.3	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	300	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.38	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.45	Ω	$V_{GS} = 10V, I_D = 5.5A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	6.6	—	—	S	$V_{DS} = 50V, I_D = 5.6A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 300V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 240V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$
Q_g	Total Gate Charge	—	—	33	nC	$I_D = 9.3A$
Q_{gs}	Gate-to-Source Charge	—	—	6.9		$V_{DS} = 240V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	12		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = 150V$
t_r	Rise Time	—	25	—		$I_D = 9.3A$
$t_{d(off)}$	Turn-Off Delay Time	—	35	—		$R_G = 12\Omega$
t_f	Fall Time	—	29	—		$R_D = 16\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	920	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	160	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	8.7	—		$f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Input Capacitance	—	1200	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Input Capacitance	—	52	—		$V_{GS} = 0V, V_{DS} = 240V, f = 1.0\text{MHz}$
$C_{oss\text{ eff.}}$	Input Capacitance	—	102	—		$V_{GS} = 0V, V_{DS} = 0V\text{ to }240V$ ⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	9.3	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	37		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 9.3A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	280	420	ns	$T_J = 25^\circ\text{C}, I_F = 9.3A$
Q_{rr}	Reverse Recovery Charge	—	1.5	2.3	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25^\circ\text{C}$, $L = 3.7\text{mH}$
 $R_G = 25\Omega, I_{AS} = 9.3A$. (See Figure 12)

③ $I_{SD} \leq 9.3A, di/dt \leq 270A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

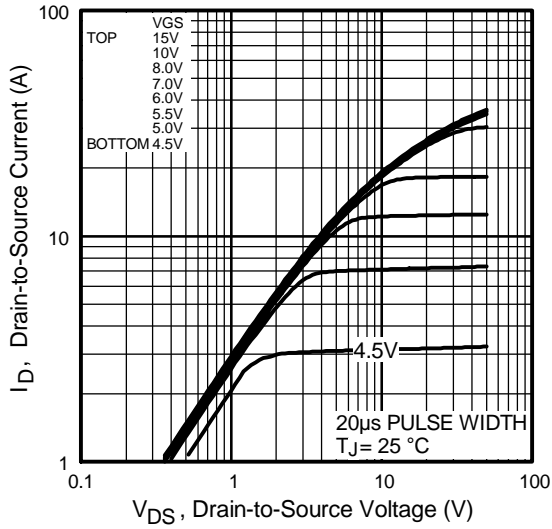


Fig 1. Typical Output Characteristics

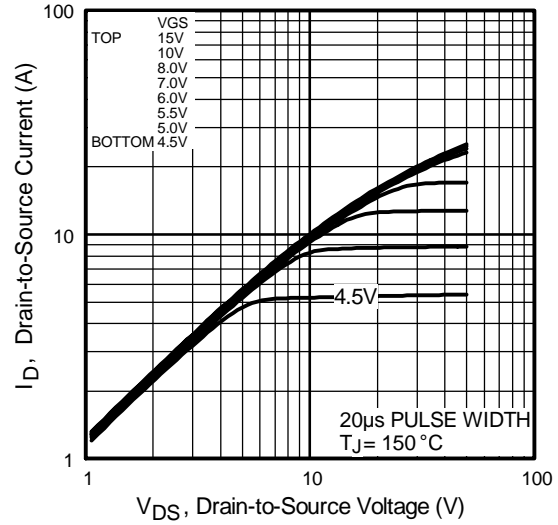


Fig 2. Typical Output Characteristics

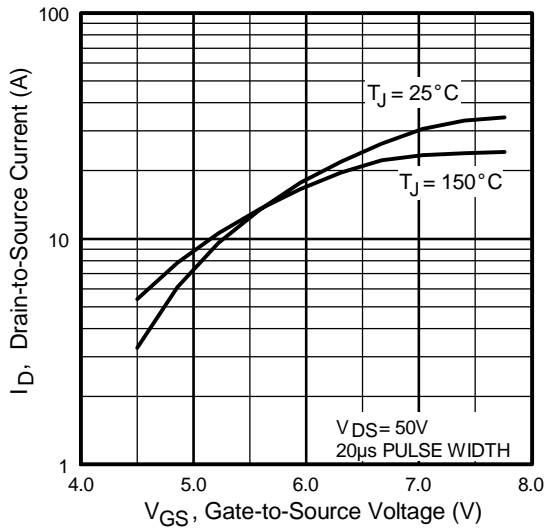


Fig 3. Typical Transfer Characteristics

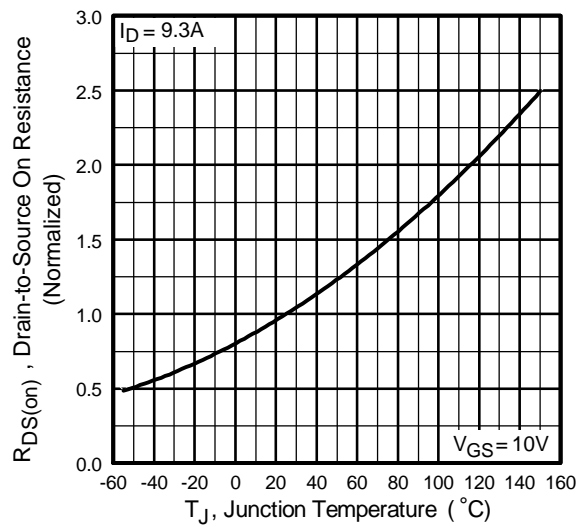


Fig 4. Normalized On-Resistance Vs. Temperature

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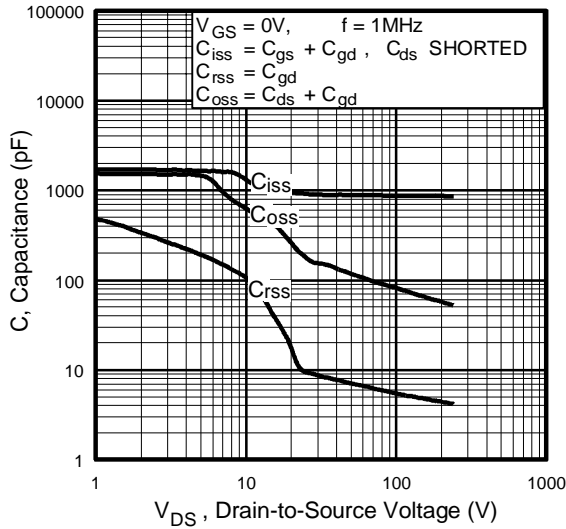


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

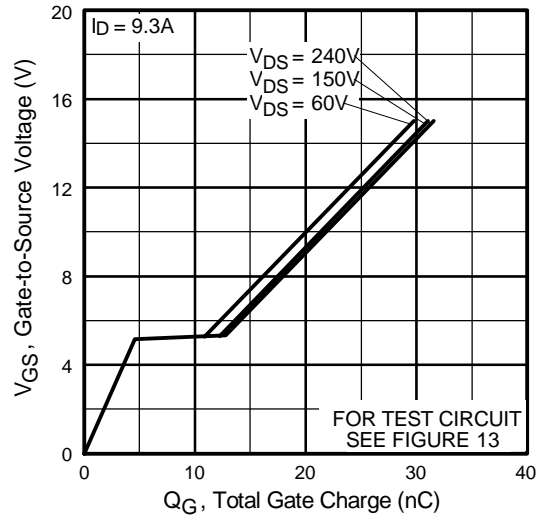


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

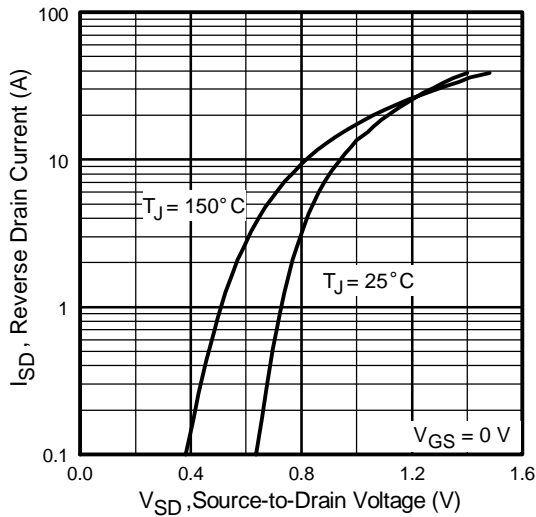


Fig 7. Typical Source-Drain Diode Forward Voltage

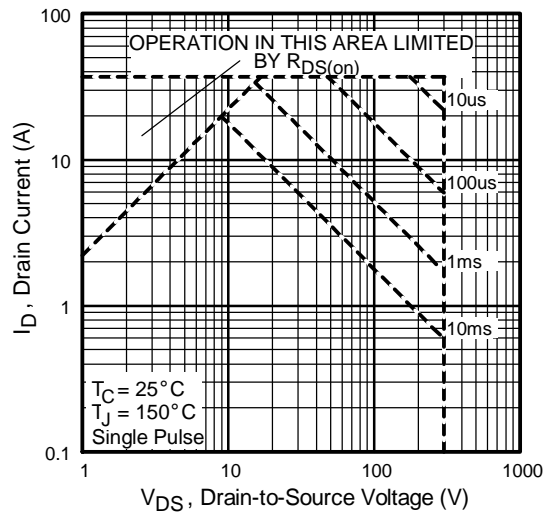


Fig 8. Maximum Safe Operating Area

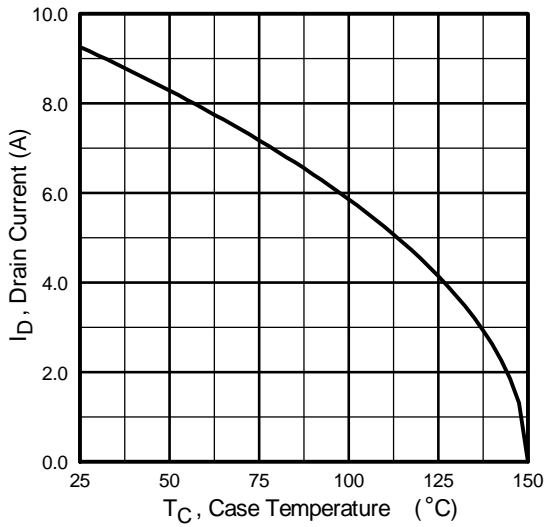


Fig 9. Maximum Drain Current Vs. Case Temperature

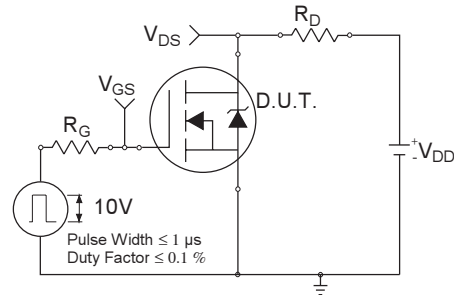


Fig 10a. Switching Time Test Circuit

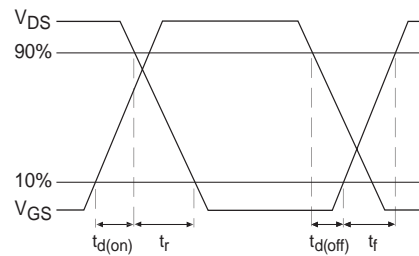


Fig 10b. Switching Time Waveforms

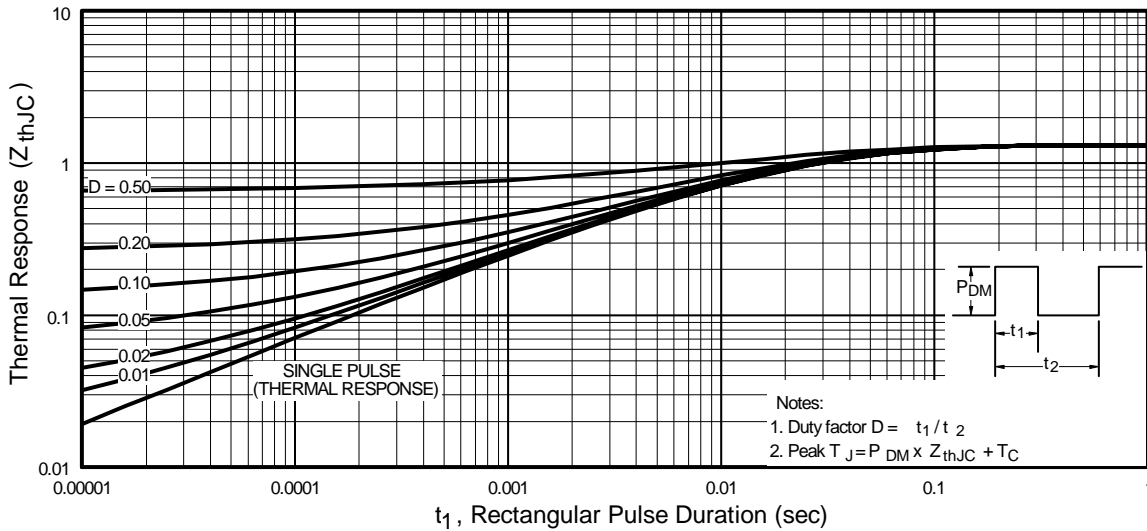


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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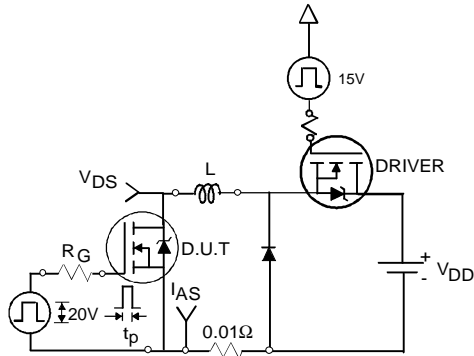


Fig 12a. Unclamped Inductive Test Circuit

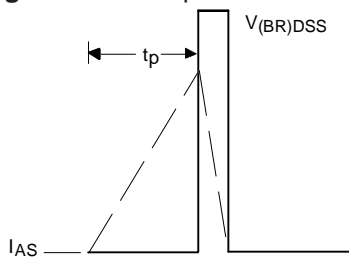


Fig 12b. Unclamped Inductive Waveforms

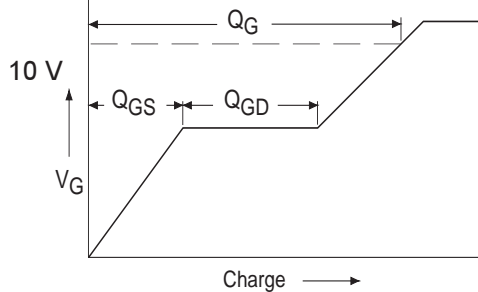


Fig 13a. Basic Gate Charge Waveform

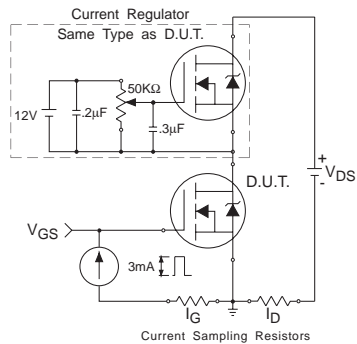


Fig 13b. Gate Charge Test Circuit

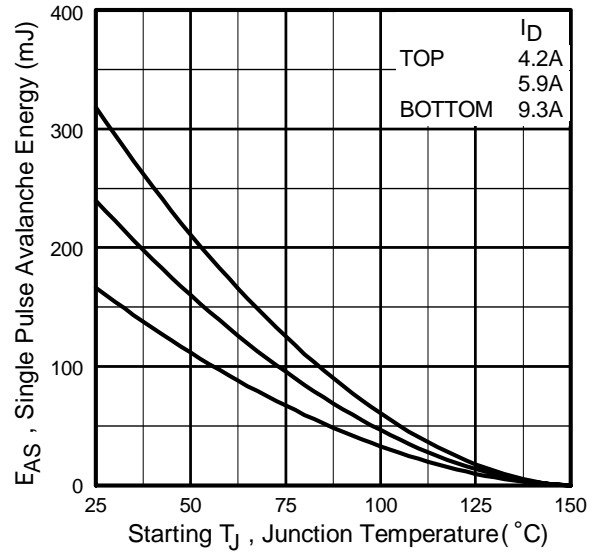


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

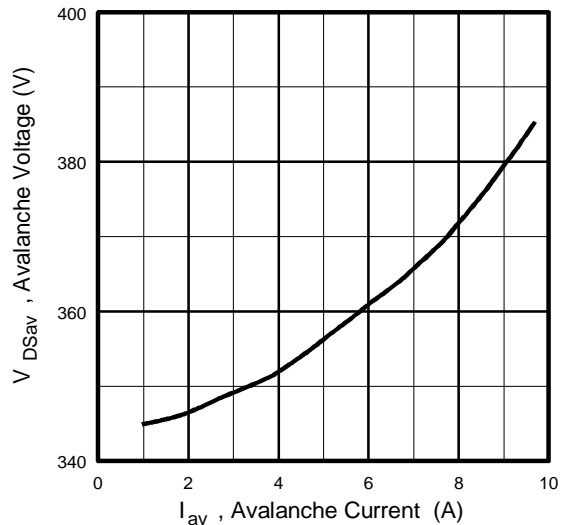


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

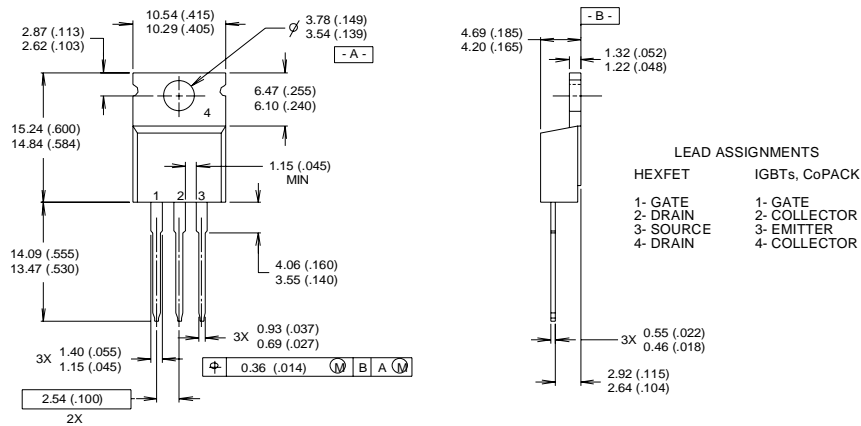
Fig 14. For N-Channel HEXFETS

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TO-220AB Package Outline

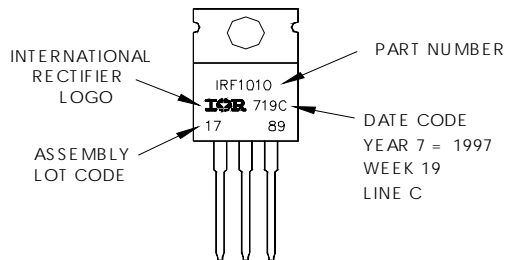
Dimensions are shown in millimeters (inches)



- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 - 2 CONTROLLING DIMENSION : INCH
 - 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
 - 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

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 TAC Fax: (310) 252-7903

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