

IRFBA1404PPbF

HEXFET® Power MOSFET

Typical Applications

- Industrial Motor Drive

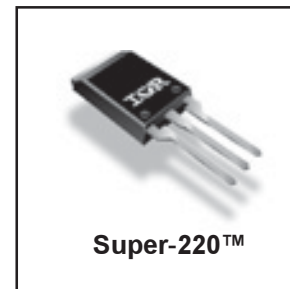
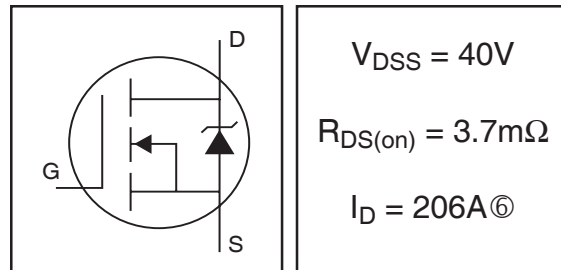
Benefits

- Advanced Process Technology
- Ultra Low On-Resistance
- Increase Current Handling Capability
- 175°C Operating Temperature
- Fast Switching
- Dynamic dv/dt Rating
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free

Description

This Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this MOSFET are a 175°C junction operating temperature, fast switching speed and improved ruggedness in single and repetitive avalanche. The Super-220™ is a package that has been designed to have the same mechanical outline and pinout as the industry standard TO-220 but can house a considerably larger silicon die. The result is significantly increased current handling capability over both the TO-220 and the much larger TO-247 package. The combination of extremely low on-resistance silicon and the Super-220™ package makes it ideal to reduce the component count in multiparalleled TO-220 applications, reduce system power dissipation, upgrade existing designs or have TO-247 performance in a TO-220 outline.

These benefits make this design an extremely efficient and reliable device for use in a wide variety of applications.



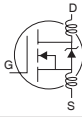
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	206 ⁽⁶⁾	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	145 ⁽⁶⁾	
I_{DM}	Pulsed Drain Current ⁽¹⁾	650	
$P_D @ T_C = 25^\circ C$	Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ⁽²⁾	480	mJ
I_{AR}	Avalanche Current ⁽¹⁾	See Fig.12a, 12b, 14, 15	A
E_{AR}	Repetitive Avalanche Energy ⁽¹⁾		mJ
dv/dt	Peak Diode Recovery dv/dt ⁽³⁾	5.0	V/ns
T_J	Operating Junction and	-40 to + 175	°C
T_{STG}	Storage Temperature Range	-55 to + 175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Recommended clip force	20	N

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	40	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.036	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	3.7	mΩ	V _{GS} = 10V, I _D = 95A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = 10V, I _D = 250μA
g _{fs}	Forward Transconductance	106	—	—	S	V _{DS} = 25V, I _D = 60A
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 40V, V _{GS} = 0V
		—	—	250		V _{DS} = 32V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V
Q _g	Total Gate Charge	—	160	200	nC	I _D = 95A
Q _{gs}	Gate-to-Source Charge	—	35	—		V _{DS} = 32V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	42	60		V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	17	—	ns	V _{DD} = 20V
t _r	Rise Time	—	140	—		I _D = 95A
t _{d(off)}	Turn-Off Delay Time	—	72	—		R _G = 2.5Ω
t _f	Fall Time	—	26	—		R _D = 0.21Ω ④
L _D	Internal Drain Inductance	—	2.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	5.0	—		
C _{iss}	Input Capacitance	—	7360	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1680	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	240	—		f = 1.0MHz, See Fig. 5
C _{oss}	Output Capacitance	—	6630	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	1490	—		V _{GS} = 0V, V _{DS} = 32V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance ⑤	—	1540	—		V _{GS} = 0V, V _{DS} = 0V to 32V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	206⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	650		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 95A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	71	110	ns	T _J = 25°C, I _F = 95A
Q _{rr}	Reverse Recovery Charge	—	180	270	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	0.50	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	0.5	—	
R _{θJA}	Junction-to-Ambient	—	58	

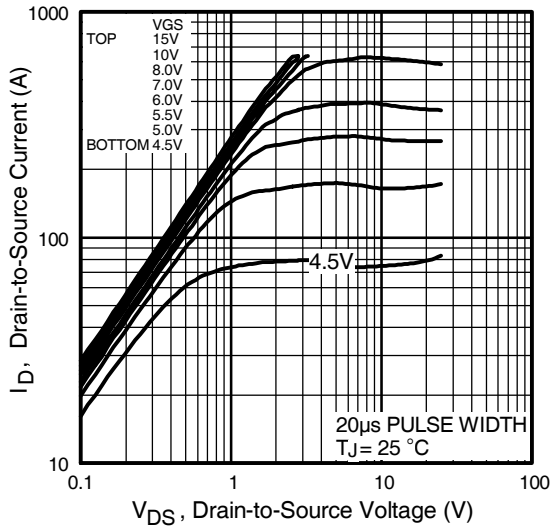


Fig 1. Typical Output Characteristics

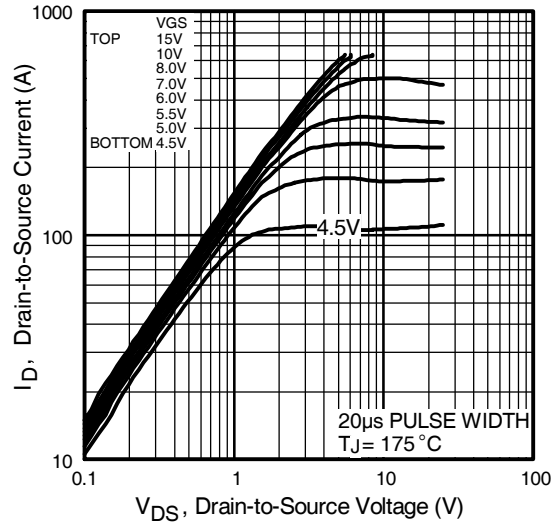


Fig 2. Typical Output Characteristics

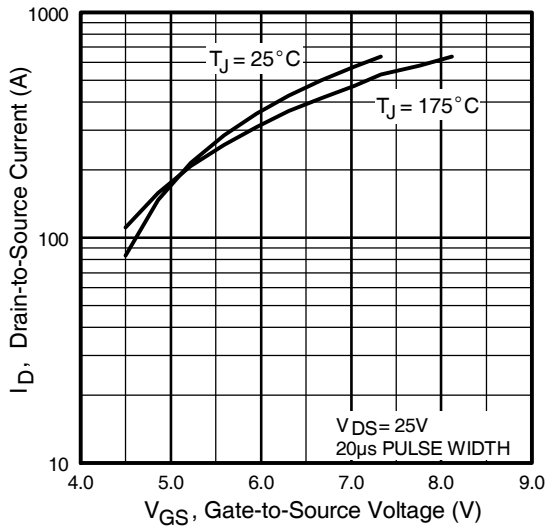


Fig 3. Typical Transfer Characteristics

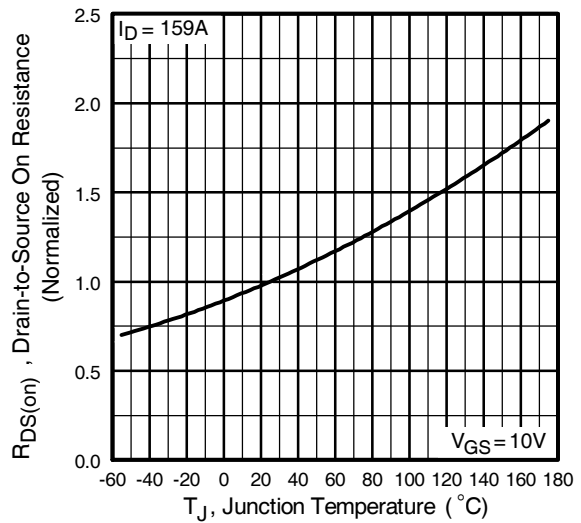


Fig 4. Normalized On-Resistance Vs. Temperature

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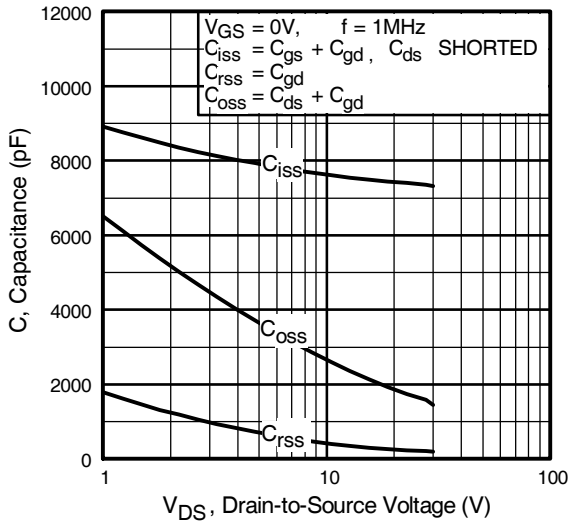


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

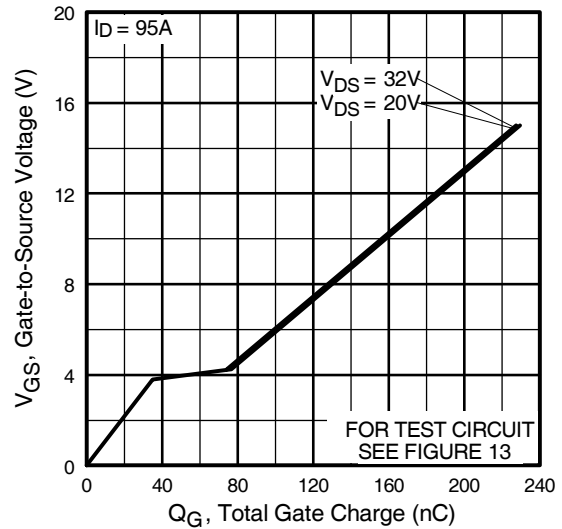


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

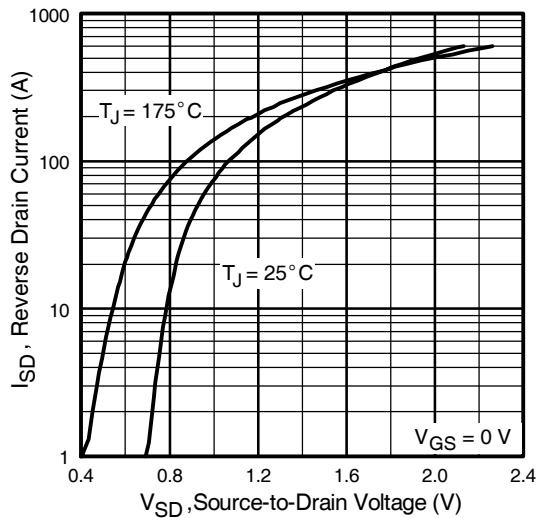


Fig 7. Typical Source-Drain Diode Forward Voltage

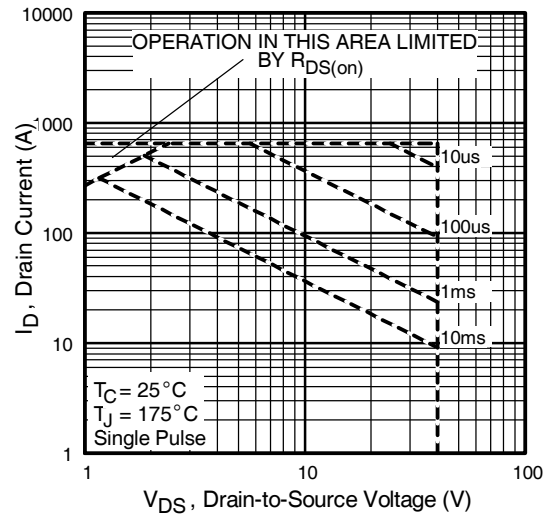


Fig 8. Maximum Safe Operating Area

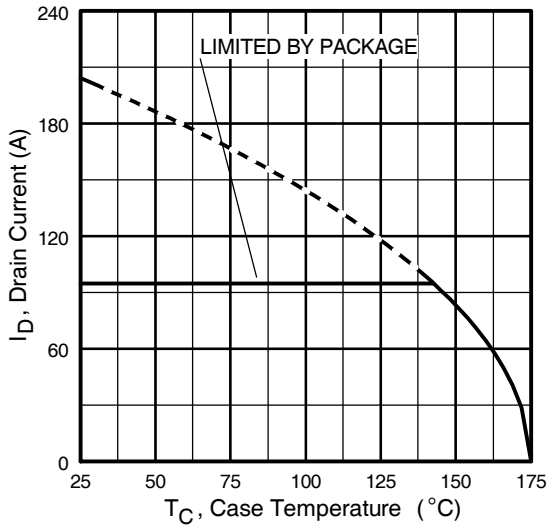


Fig 9. Maximum Drain Current Vs. Case Temperature

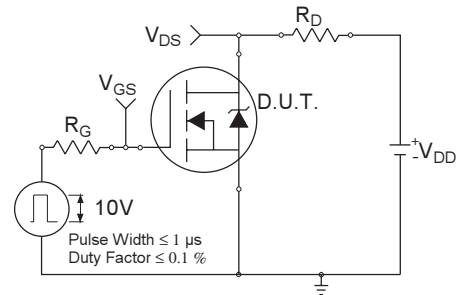


Fig 10a. Switching Time Test Circuit

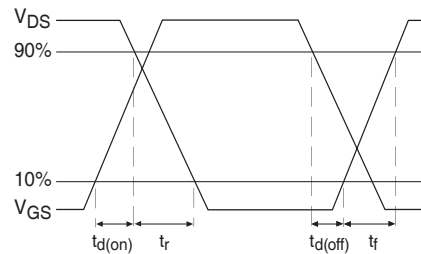


Fig 10b. Switching Time Waveforms

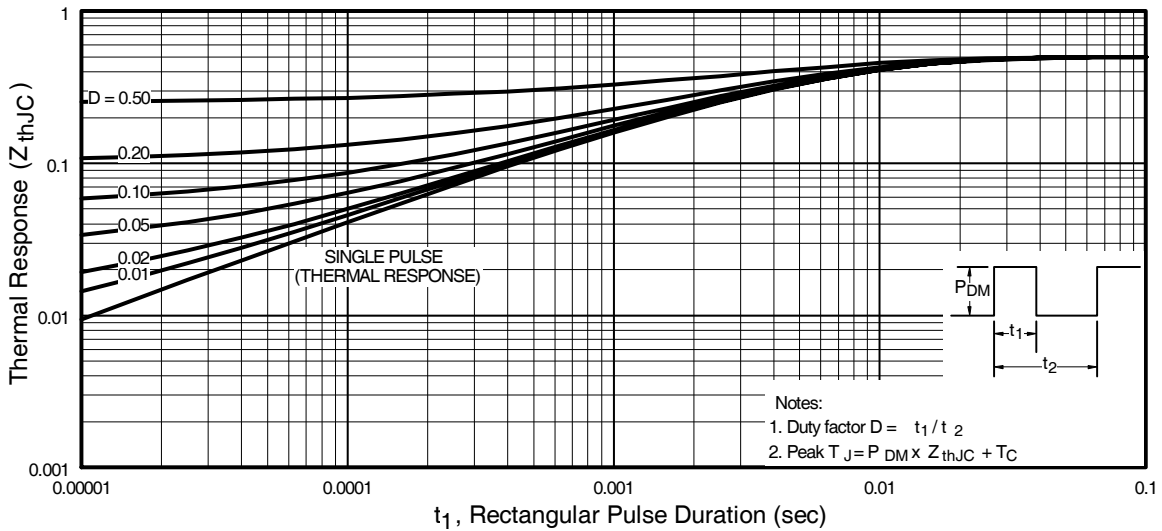


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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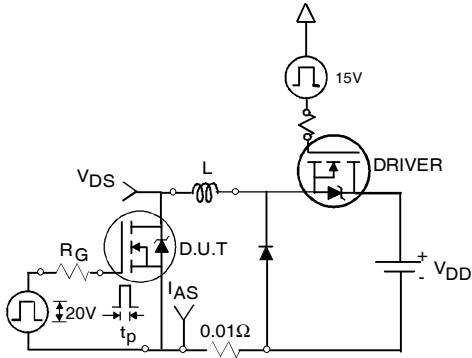


Fig 12a. Unclamped Inductive Test Circuit

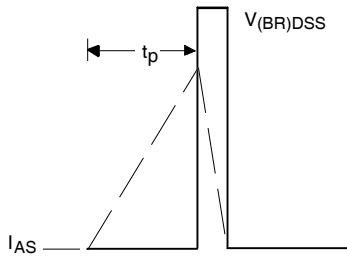


Fig 12b. Unclamped Inductive Waveforms

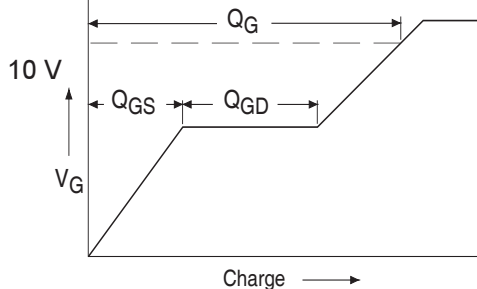


Fig 13a. Basic Gate Charge Waveform

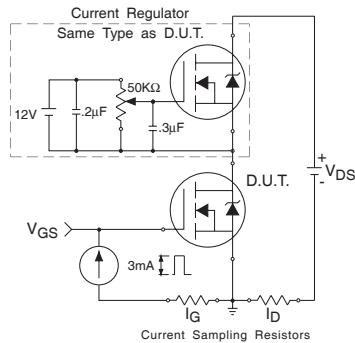


Fig 13b. Gate Charge Test Circuit

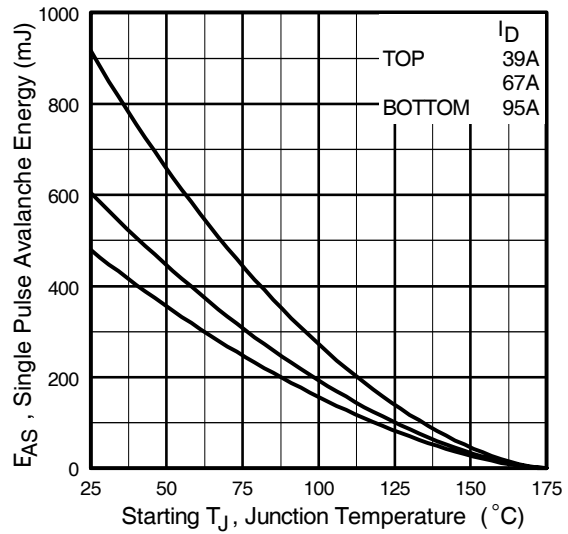


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

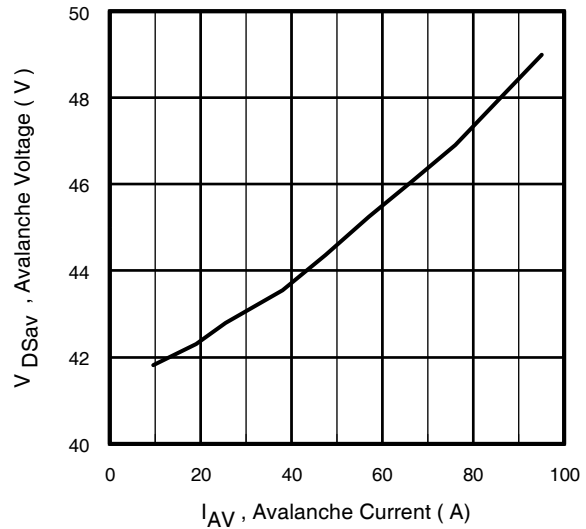


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

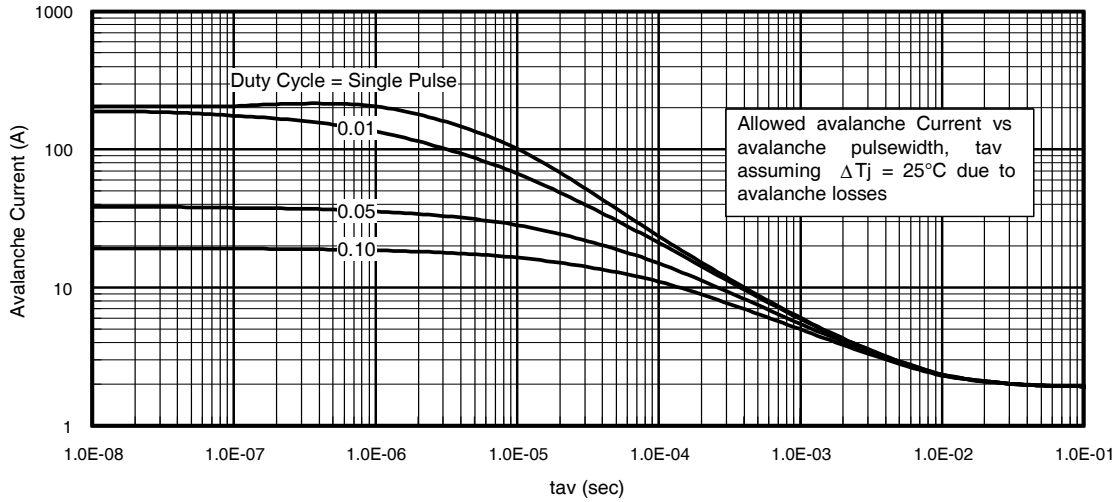


Fig 14. Typical Avalanche Current Vs.Pulsewidth

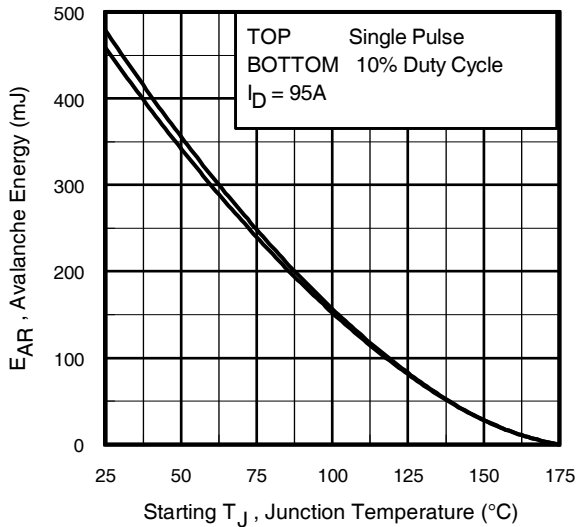


Fig 15. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

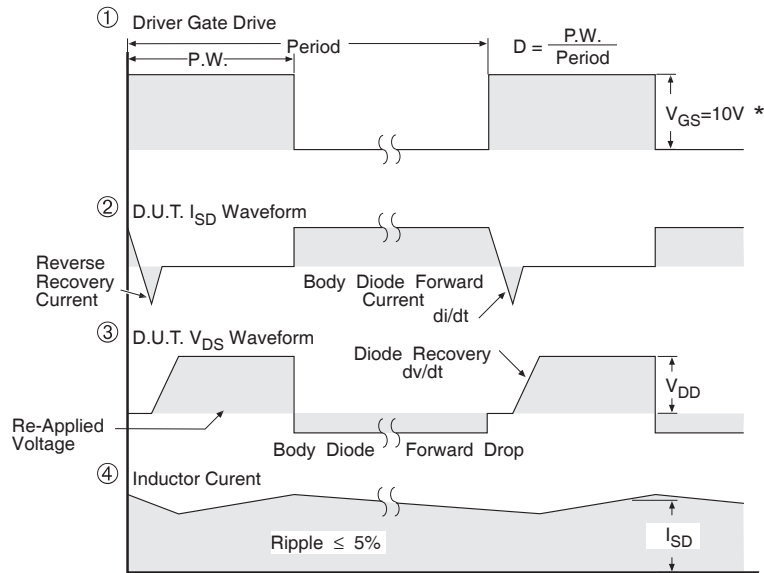
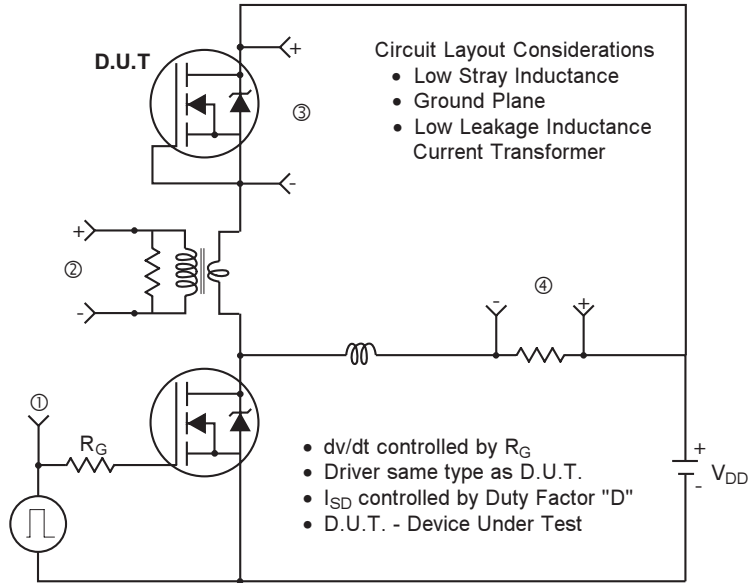
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = \frac{1}{2} (1.3 \cdot BV \cdot I_{av}) = \frac{\Delta T}{Z_{thJC}}$$

$$I_{av} = \frac{2\Delta T}{[1.3 \cdot BV \cdot Z_{th}]}$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

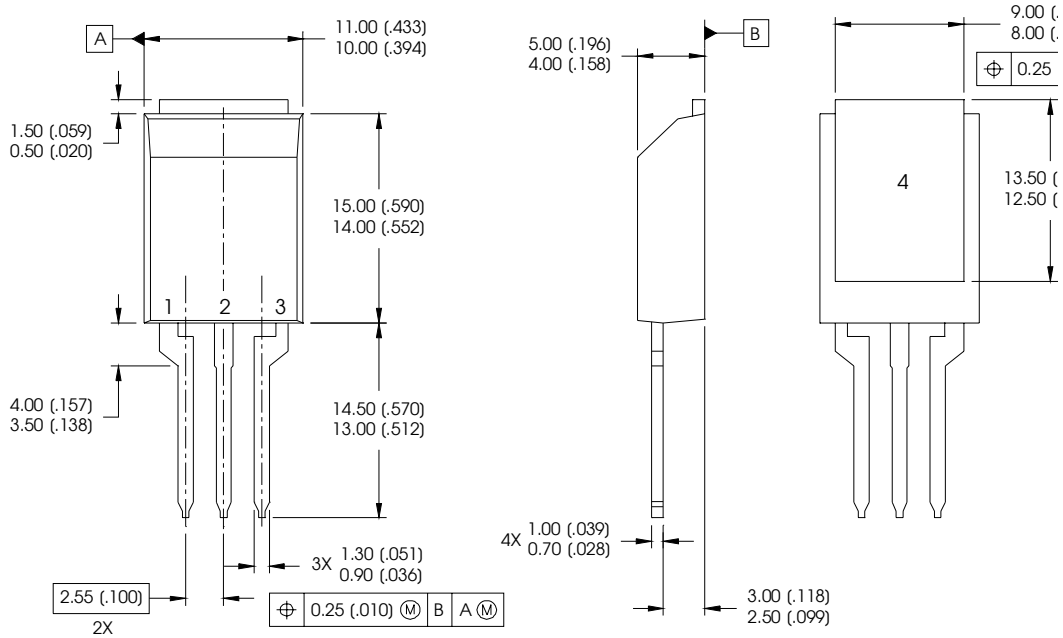
Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 16. For N-Channel HEXFET[®] Power MOSFETs

Super-220™ (TO-273AA) Package Outline



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-273AA.

LEAD ASSIGNMENTS

<u>MOSFET</u>	<u>IGBT</u>
1 – GATE	1 – GATE
2 – DRAIN	2 – COLLECTOR
3 – SOURCE	3 – EMITTER
4 – DRAIN	4 – COLLECTOR

Notes:

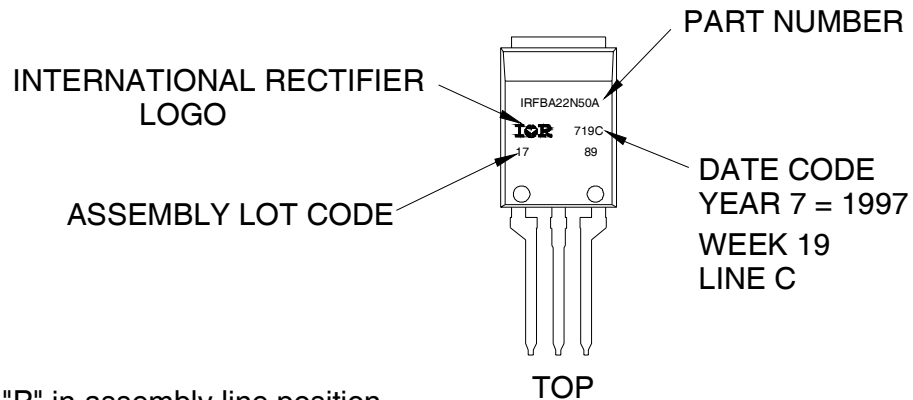
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.11\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 95\text{A}$.
- ③ $I_{SD} \leq 95\text{A}$, $di/dt \leq 150\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} . Refer to AN-1001
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 95A.

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Super-220 (TO-273AA) Part Marking Information

EXAMPLE: THIS IS AN IRFBA22N50A WITH
ASSEMBLY LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Note: "P" in assembly line position
indicates "Lead-Free"

Super-220™ not recommended for surface mount application

Notes:

1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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