International
IOR Rectifier

PD-91897A

**SMPS MOSFET**

# IRFBC40AS

HEXFET® Power MOSFET

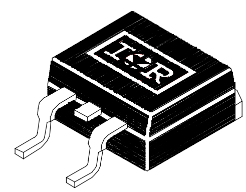
### Applications

- Switch Mode Power Supply ( SMPS )
- Uninterruptable Power Supply
- High speed power switching

| $V_{DSS}$ | Rds(on) max | $I_D$ |
|---|---|---|
| **600V** | **1.2Ω** | **6.2A** |

### Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss Specified ( See AN 1001)



$D^2$Pak

### Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V⑥ | 6.2 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V⑥ | 3.9 | |
| $I_{DM}$ | Pulsed Drain Current ①⑥ | 25 | |
| $P_D$ @$T_C$ = 25°C | Power Dissipation | 125 | W |
| | Linear Derating Factor | 1.0 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 30 | V |
| dv/dt | Peak Diode Recovery dv/dt ③⑥ | 6.0 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 150 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case ) | |

### Typical SMPS Topology:

- Single transistor Forward

Notes ① through ⑤ are on page 9



6/29/99

## Static @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 600 | —— | —— | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | —— | 0.66 | —— | V/°C | Reference to 25°C, $I_D$ = 1mA ⑥ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | —— | —— | 1.2 | Ω | $V_{GS}$ = 10V, $I_D$ = 3.7A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | —— | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | —— | —— | 25 | µA | $V_{DS}$ = 600V, $V_{GS}$ = 0V |
| | | —— | —— | 250 | | $V_{DS}$ = 480V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | —— | —— | 100 | nA | $V_{GS}$ = 30V |
| | Gate-to-Source Reverse Leakage | —— | —— | -100 | | $V_{GS}$ = -30V |

## Dynamic @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $g_{fs}$ | Forward Transconductance | 3.4 | —— | —— | S | $V_{DS}$ = 50V, $I_D$ = 3.7A |
| $Q_g$ | Total Gate Charge | —— | —— | 42 | nC | $I_D$ = 6.2A |
| $Q_{gs}$ | Gate-to-Source Charge | —— | —— | 10 | | $V_{DS}$ = 480V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | —— | —— | 20 | | $V_{GS}$ = 10V, See Fig. 6 and 13 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | —— | 13 | —— | ns | $V_{DD}$ = 300V |
| $t_r$ | Rise Time | —— | 23 | —— | | $I_D$ = 6.2A |
| $t_{d(off)}$ | Turn-Off Delay Time | —— | 31 | —— | | $R_G$ = 9.1Ω |
| $t_f$ | Fall Time | —— | 18 | —— | | $R_D$ = 47Ω,See Fig. 10 ④ |
| $C_{iss}$ | Input Capacitance | —— | 1036 | —— | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | —— | 136 | —— | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | —— | 7.0 | —— | | $f$ = 1.0MHz, See Fig. 5 |
| $C_{oss}$ | Output Capacitance | —— | 1487 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 1.0V, $f$ = 1.0MHz |
| $C_{oss}$ | Output Capacitance | —— | 36 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 480V, $f$ = 1.0MHz |
| $C_{oss}$ eff. | Effective Output Capacitance | —— | 48 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 480V ⑤ |

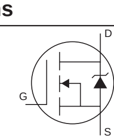
## Avalanche Characteristics

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $E_{AS}$ | Single Pulse Avalanche Energy② | —— | 570 | mJ |
| $I_{AR}$ | Avalanche Current① | —— | 6.2 | A |
| $E_{AR}$ | Repetitive Avalanche Energy① | —— | 13 | mJ |

## Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | —— | 1.0 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient ( PCB Mounted, steady-state)* | —— | 40 | |

## Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | —— | —— | 6.2 | A | MOSFET symbol showing the integral reverse p-n junction diode.   |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | —— | —— | 25 | | |
| $V_{SD}$ | Diode Forward Voltage | —— | —— | 1.5 | V | $T_J$ = 25°C, $I_S$ = 6.2A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | —— | 431 | 647 | ns | $T_J$ = 25°C, $I_F$ = 6.2A |
| $Q_{rr}$ | Reverse RecoveryCharge | —— | 1.8 | 2.8 | µC | di/dt = 100A/µs ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$+$L_D$) | | | | |

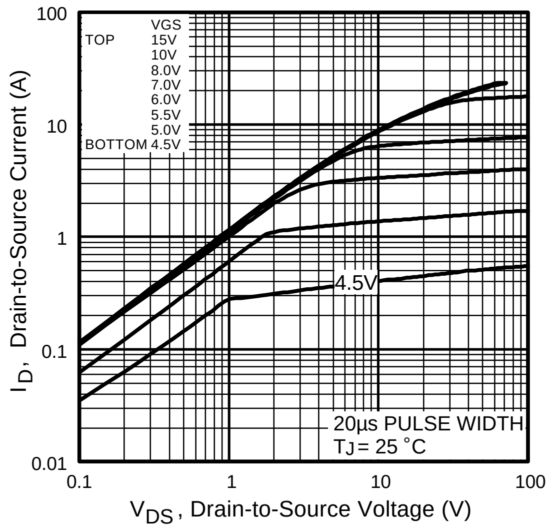



**Fig 1.** Typical Output Characteristics,

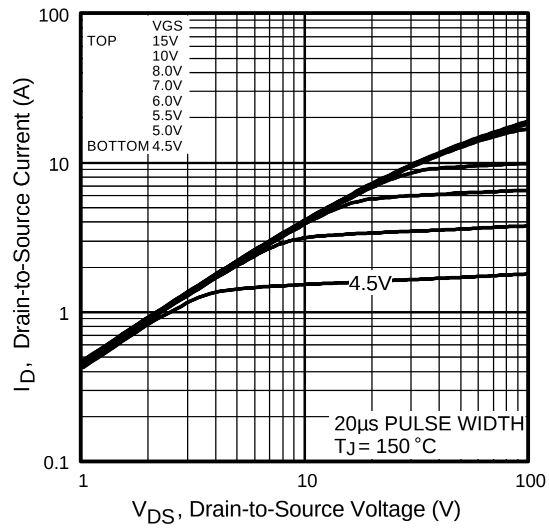



**Fig 2.** Typical Output Characteristics,

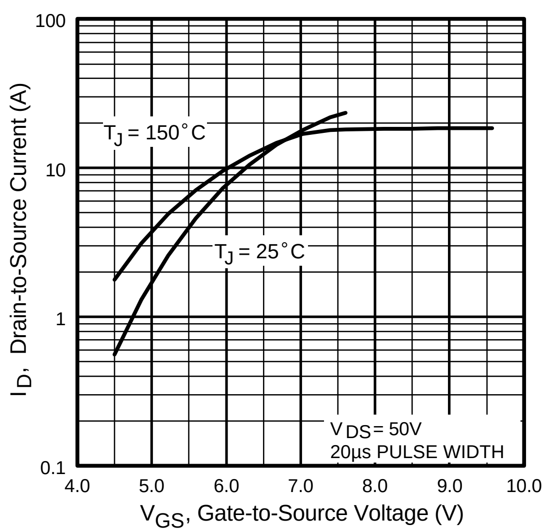



**Fig 3.** Typical Transfer Characteristics

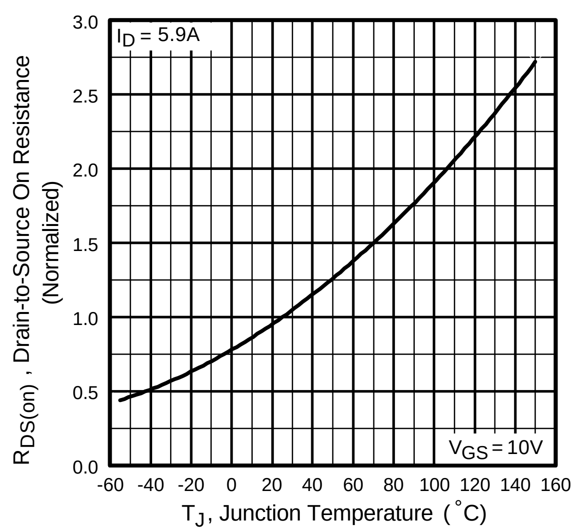



**Fig 4.** Normalized On-Resistance Vs. Temperature

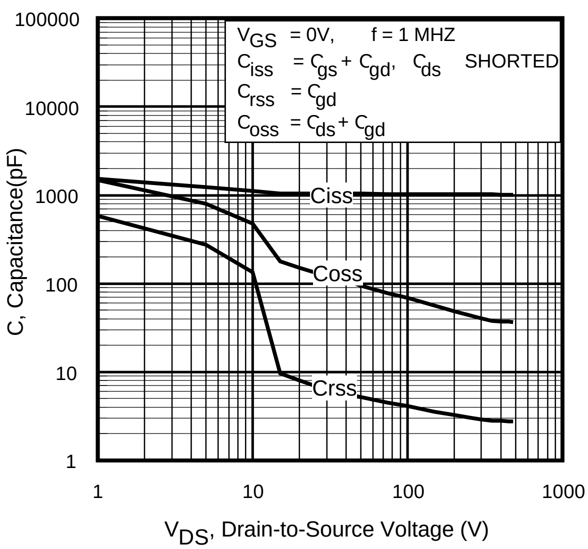



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

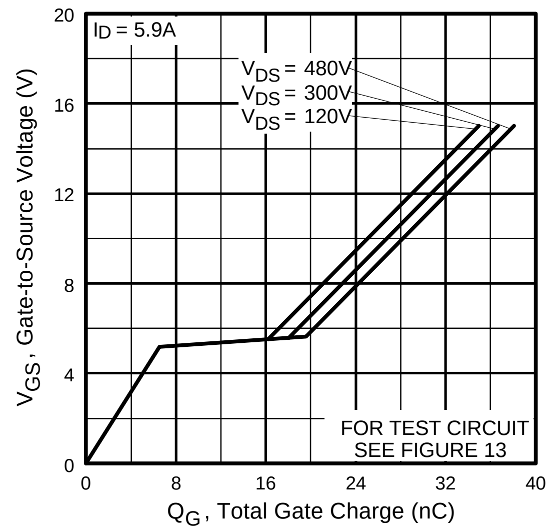



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

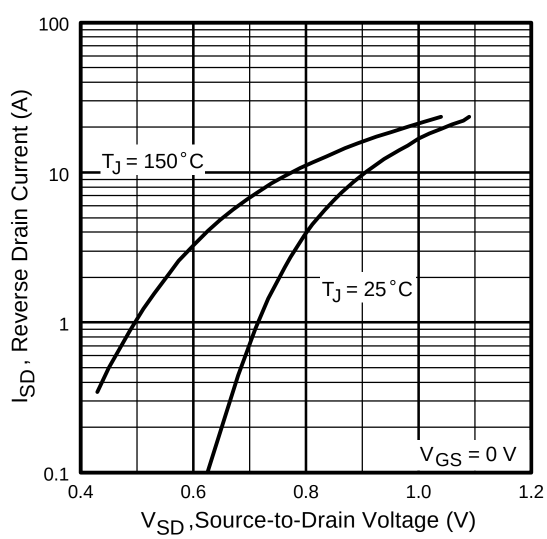



**Fig 7.** Typical Source-Drain Diode Forward Voltage

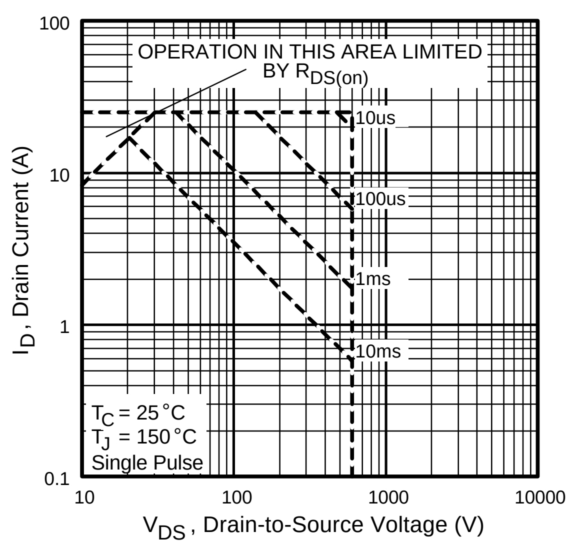



**Fig 8.** Maximum Safe Operating Area

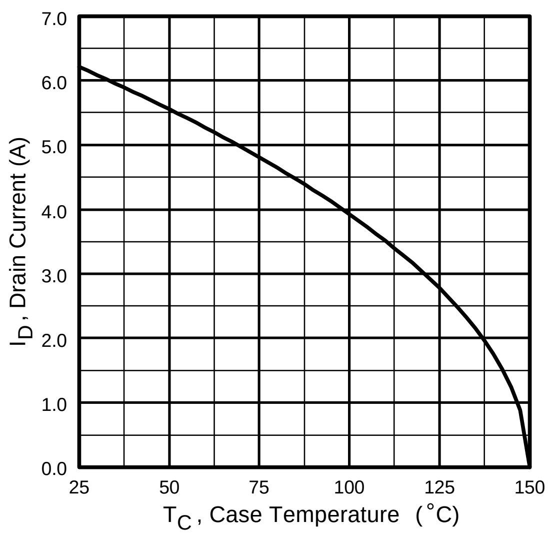



**Fig 9.** Maximum Drain Current Vs. Case Temperature

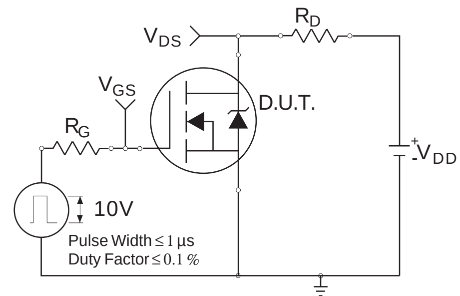



**Fig 10a.** Switching Time Test Circuit

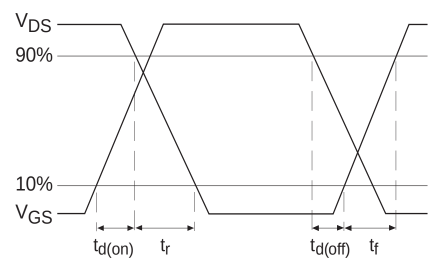



**Fig 10b.** Switching Time Waveforms

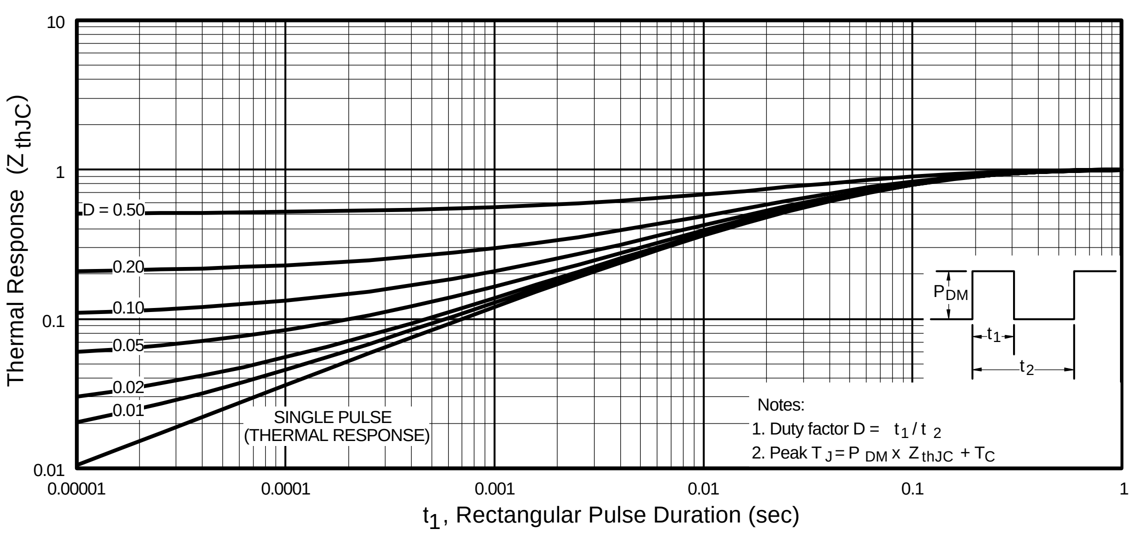



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

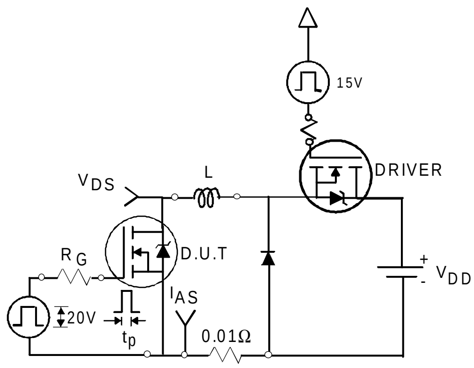



**Fig 12a.** Unclamped Inductive Test Circuit

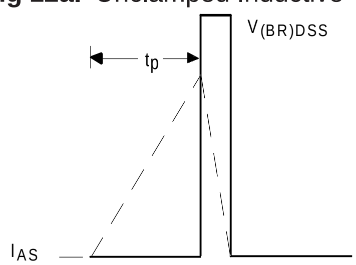



**Fig 12b.** Unclamped Inductive Waveforms

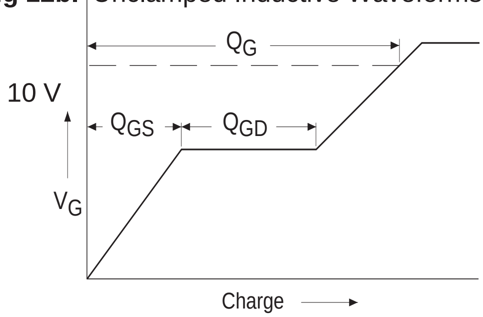



**Fig 13a.** Basic Gate Charge Waveform

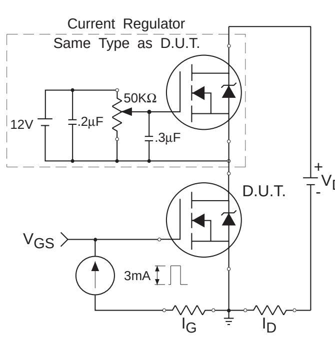



**Fig 13b.** Gate Charge Test Circuit

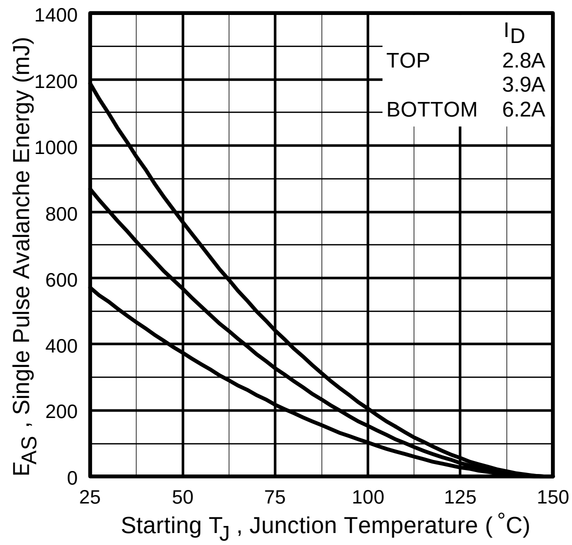



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

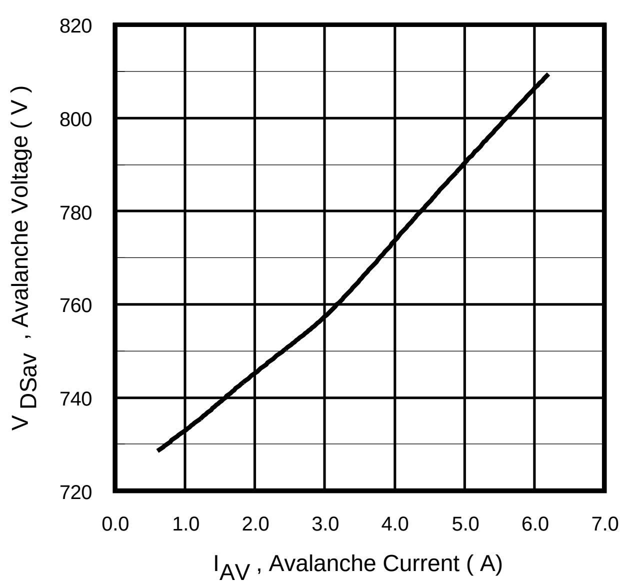
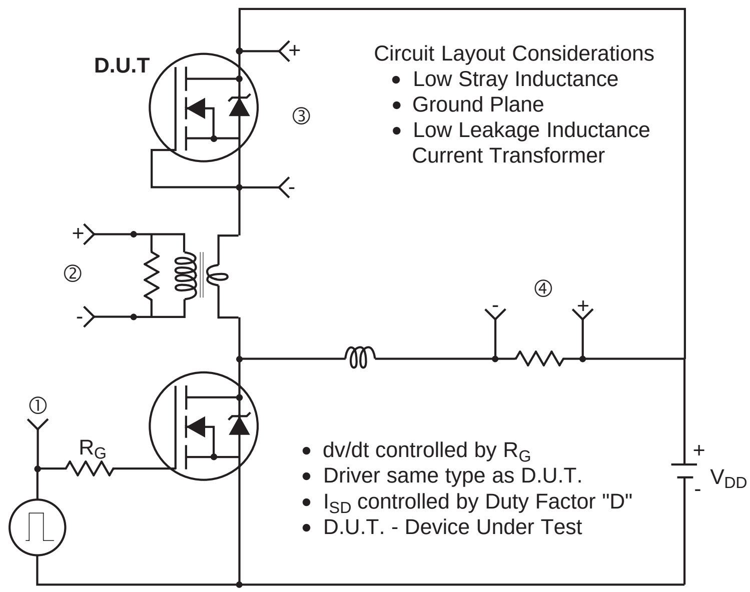
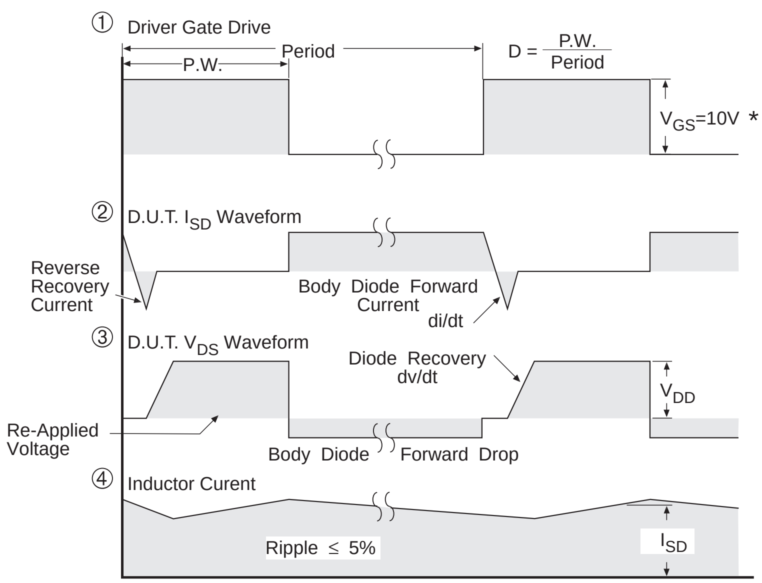



**Fig 12d.** Typical Drain-to-Source Voltage Vs. Avalanche Current

## Peak Diode Recovery dv/dt Test Circuit

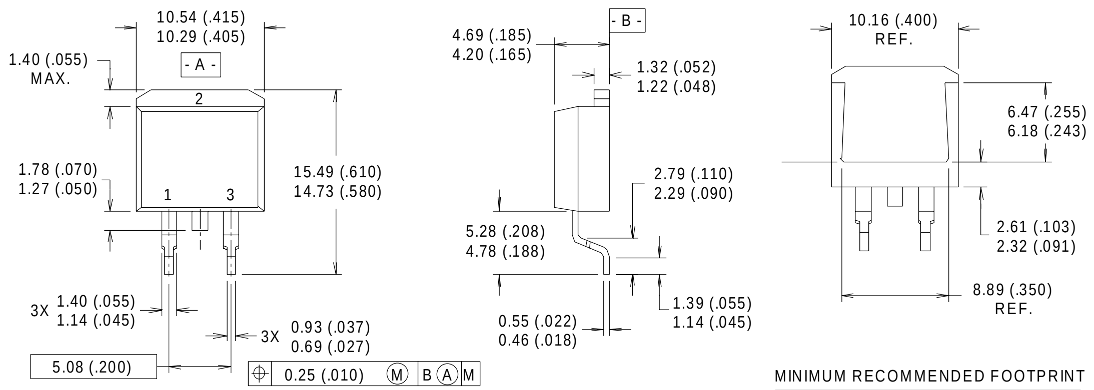


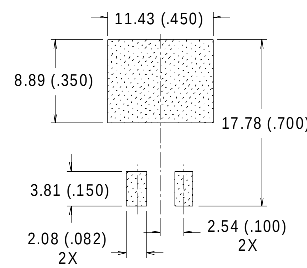

* $V_{GS}$ = 5V for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

# D²Pak Package Outline




MINIMUM RECOMMENDED FOOTPRINT



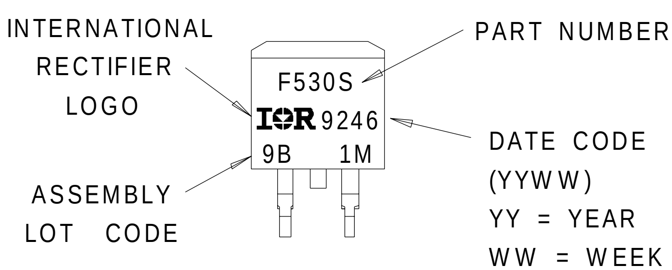

NOTES:

1. DIMENSIONS AFTER SOLDER DIP.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION : INCH.
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

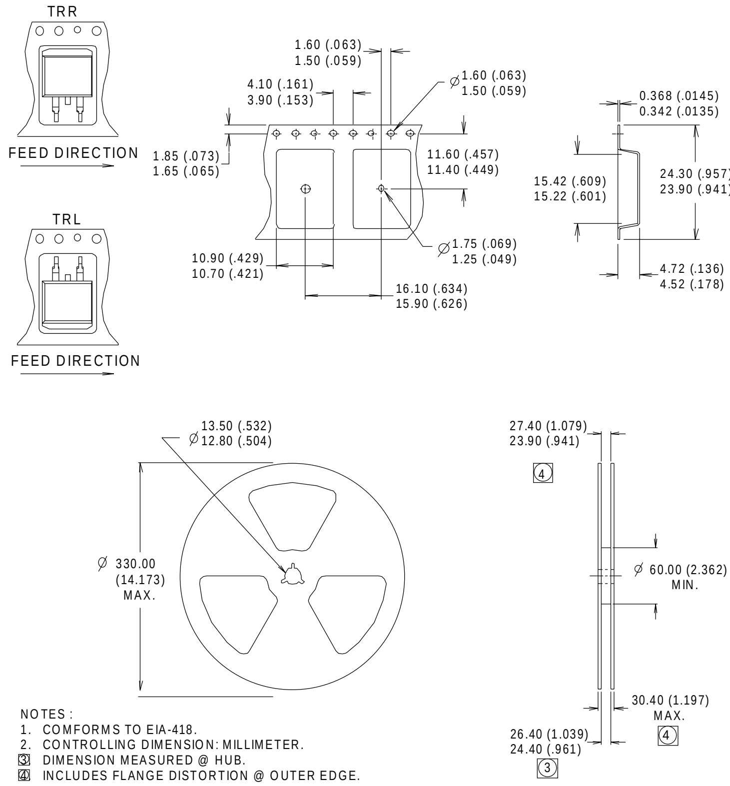
# Part Marking Information

**D²Pak**



# Tape & Reel Information

**D²Pak**




**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )

② Starting $T_J$ = 25°C, L = 29.6mH $R_G$ = 25Ω, $I_{AS}$ = 6.2A. (See Figure 12)

③ $I_{SD} \le 6.2A$, di/dt ≤ 88A/µs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le 150°C$

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ $C_{oss}$ eff. is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$

⑥ Uses IRFBC40A data and test conditions

* When mounted on FR-4 board using minimum recommended footprint.
For recommended footprint and soldering techniques refer to application note #AN-994.

International
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