

IRFD120, IRFD121, IRFD122, IRFD123

1.3A and 1.1A, 80V and 100V, 0.30 and 0.40 Ohm,
N-Channel Power MOSFETs

July 1998

Features

- 1.3A and 1.1A, 80V and 100V
- $r_{DS(ON)} = 0.30\Omega$ and 0.40Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Description

These are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. They can be operated directly from integrated circuits.

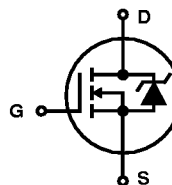
Formerly developmental type TA17401.

Ordering Information

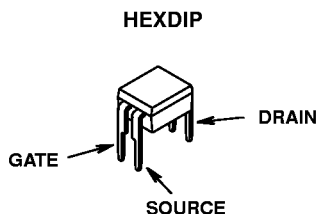
PART NUMBER	PACKAGE	BRAND
IRFD120	HEXDIP	IRFD120
IRFD121	HEXDIP	IRFD121
IRFD122	HEXDIP	IRFD122
IRFD123	HEXDIP	IRFD123

NOTE: When ordering, use the entire part number.

Symbol



Packaging



IRFD120, IRFD121, IRFD122, IRFD123

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	IRFD120	IRFD121	IRFD122	IRFD123	UNITS	
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	100	80	100	80	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	100	80	100	80	V
Continuous Drain Current	I_D	1.3	1.3	1.1	1.1	A
Pulsed Drain Current	I_{DM}	5.2	5.2	4.4	4.4	A
Gate to Source Voltage	V_{GS}	± 20	± 20	± 20	± 20	V
Maximum Power Dissipation	P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 1)		0.008	0.008	0.008	0.008	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 3)	E_{AS}	36	36	36	36	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering						
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	300	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260	260	260	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$ to 125°C .

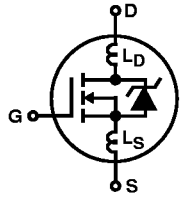
Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage IRFD120, IRFD122	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ (Figure 9)	100	-	-	V
			80	-	-	V
IRFD121, IRFD123						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	25	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V},$ $T_J = 125^\circ\text{C}$	-	-	250	μA
On-State Drain Current (Note 2) IRFD120, IRFD121	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)} \text{ Max}, V_{GS} = 10\text{V}$	1.3	-	-	A
			1.1	-	-	A
IRFD122, IRFD123						
Gate Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 500	nA
Drain Source On Resistance (Note 2) IRFD120, IRFD121	$r_{DS(ON)}$	$I_D = 0.6\text{A}, V_{GS} = 10\text{V}$ (Figures 7, 8)	-	0.25	0.30	Ω
			-	0.30	0.40	Ω
IRFD122, IRFD123						
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)} \text{ Max}, I_D = 0.6\text{A}$	0.9	1.0	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 0.5 \times \text{Rated } BV_{DSS}, I_D \approx 1.3\text{A},$ $V_{GS} = 10\text{V}, R_G = 9.1\Omega$ (Figures 16, 17) $R_L = 38.5\Omega$ for $V_{DD} = 50\text{V}$ $R_L = 30.8\Omega$ for $V_{DD} = 40\text{V}$ MOSFET Switching Times are Essentially Inde- pendent of Operating Temperature	-	20	40	ns
Rise Time	t_r		-	35	70	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	35	70	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = 10\text{V}, I_D = 1.3\text{A}, V_{DS} = 0.8 \times \text{Rated } BV_{DSS},$ $I_{g(REF)} = 1.5\text{mA}$ (Figures 13, 18, 19) Gate Charge is Essentially Independent of Operating Temperature	-	11	15	nC
Gate to Source Charge	Q_{gs}		-	6.0	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	5.0	-	nC
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$ (Figure 10)	-	450	-	pF
Output Capacitance	C_{OSS}		-	200	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF

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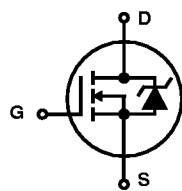
Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Internal Drain Inductance	L_D	Measured From the Drain Lead, 2mm (0.08in) from Package to Center of Die	-	4.0	-	nH
Internal Source Inductance	L_S	Measured From the Source Lead, 2mm (0.08in) from Header to Source Bonding Pad	-	6.0	-	nH
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	120	$^\circ\text{C/W}$



Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode	-	-	1.3	A
Pulse Source to Drain Current (Note 3)	I_{SDM}		-	-	5.2	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^\circ\text{C}$, $I_{SD} = 1.3\text{A}$, $V_{GS} = 0\text{V}$, (Figure 12)	-	-	2.5	V
Reverse Recovery Time	t_{rr}	$T_J = 150^\circ\text{C}$, $I_{SD} = 1.3\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	280	-	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^\circ\text{C}$, $I_{SD} = 1.3\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	1.6	-	μC



NOTES:

2. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. $V_{DD} = 25\text{V}$, starting $T_J = 25^\circ\text{C}$, $L = 32\text{mH}$, $R_G = 25\Omega$, peak $I_{AS} = 1.3\text{A}$. See Figures 14, 15.

Typical Performance Curves Unless Otherwise Specified

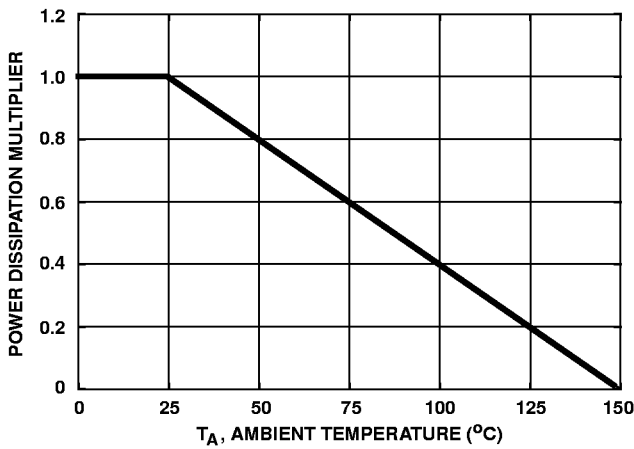


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

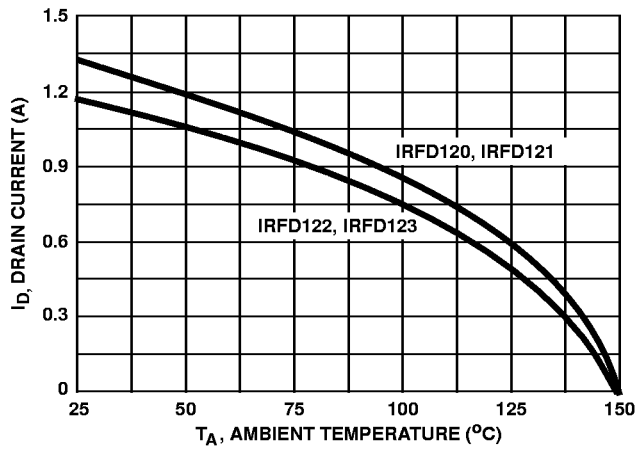


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

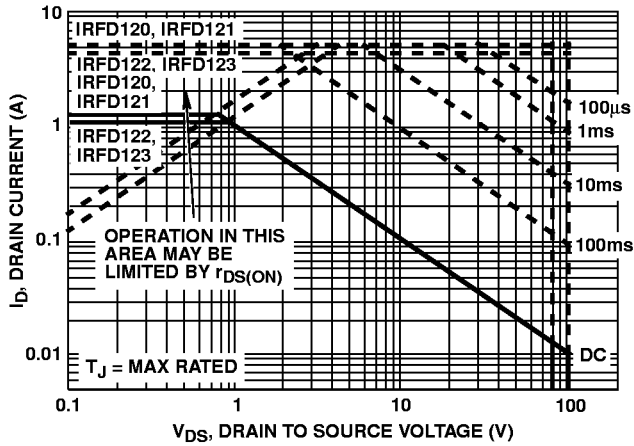


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

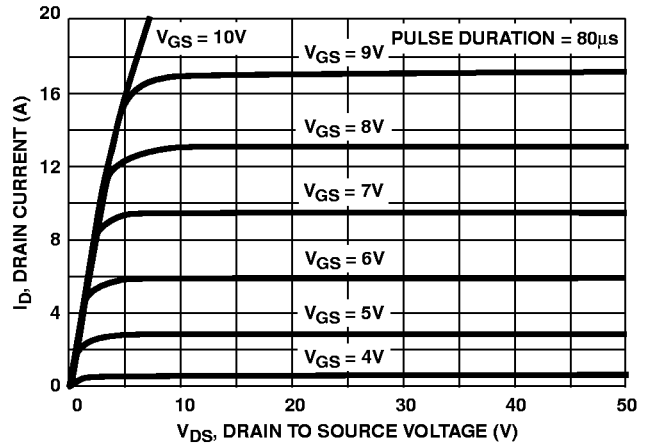


FIGURE 4. OUTPUT CHARACTERISTICS

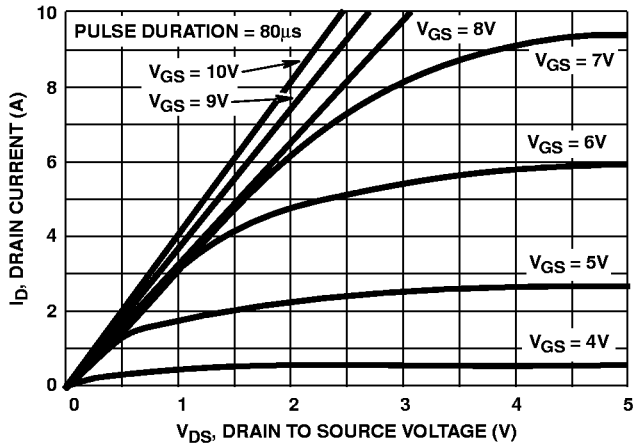


FIGURE 5. SATURATION CHARACTERISTICS

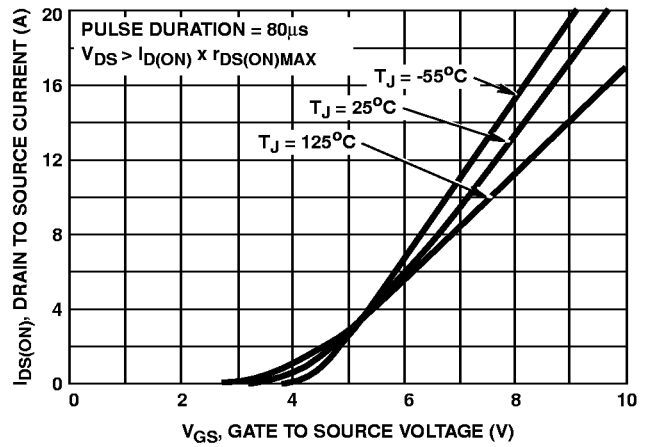
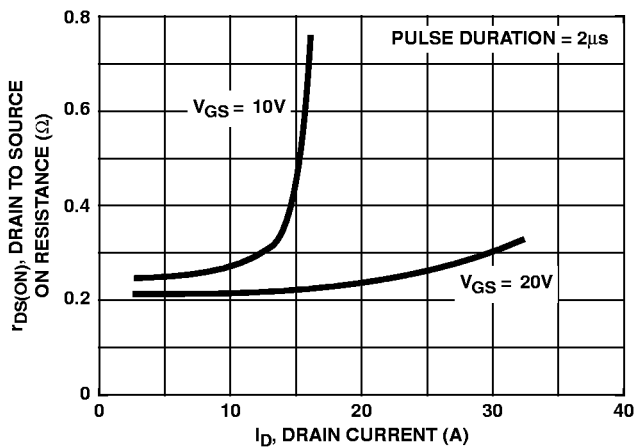


FIGURE 6. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2µs pulse is minimal.

FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

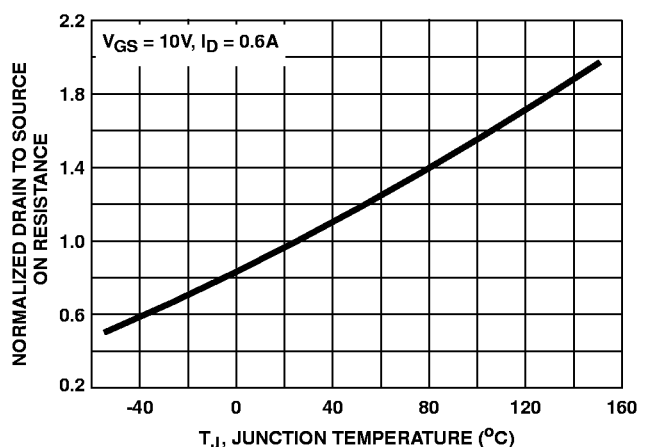


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

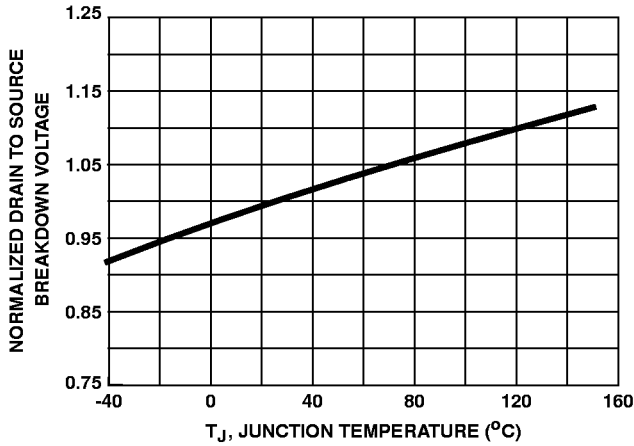


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

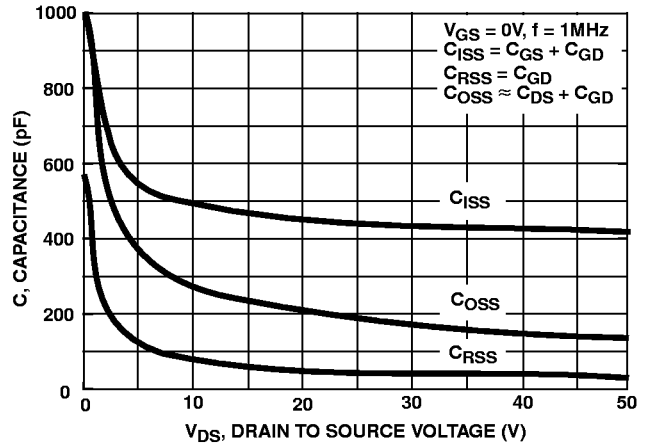


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

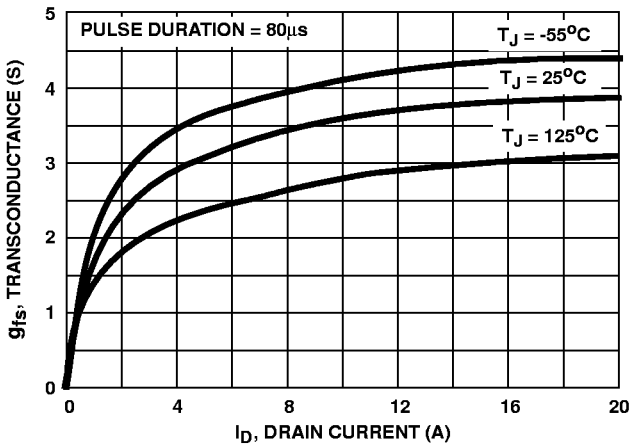


FIGURE 11. TRANSCONDUCTANCE vs DRAIN CURRENT

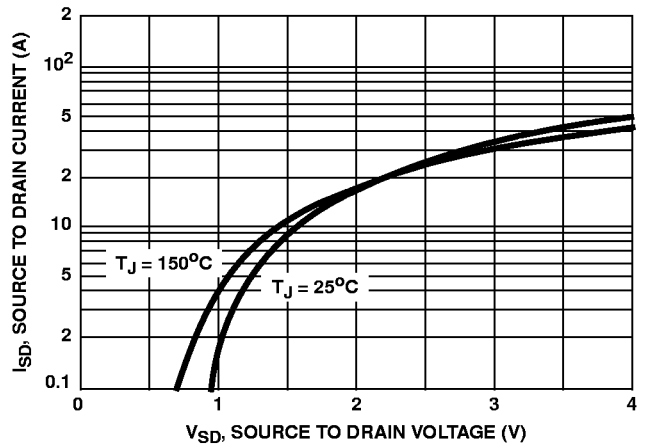


FIGURE 12. SOURCE TO DRAIN DIODE VOLTAGE

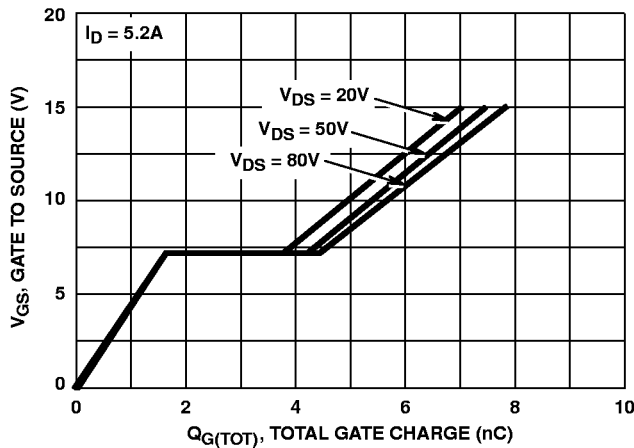


FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

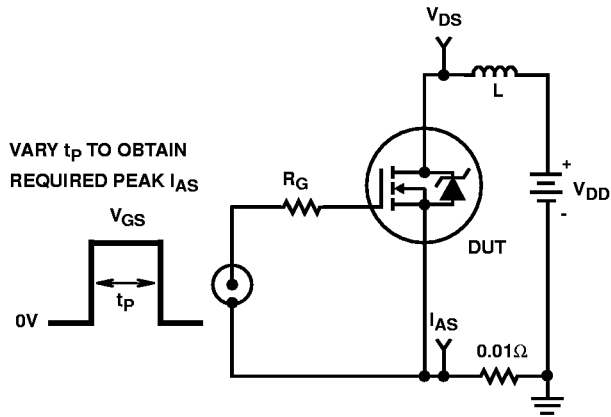


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

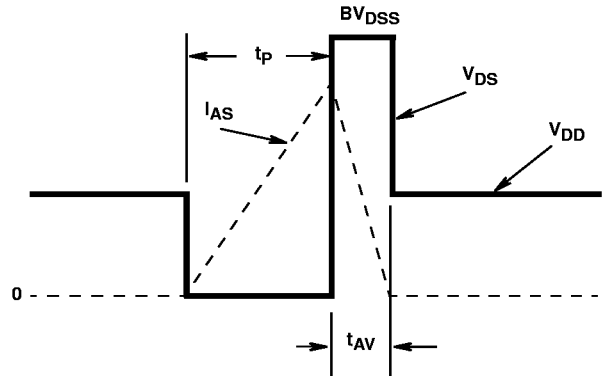


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

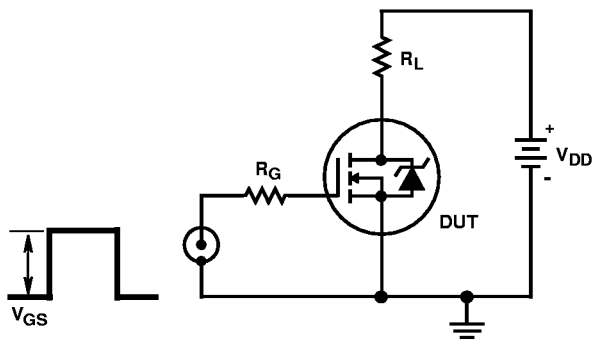


FIGURE 16. SWITCHING TIME TEST CIRCUIT

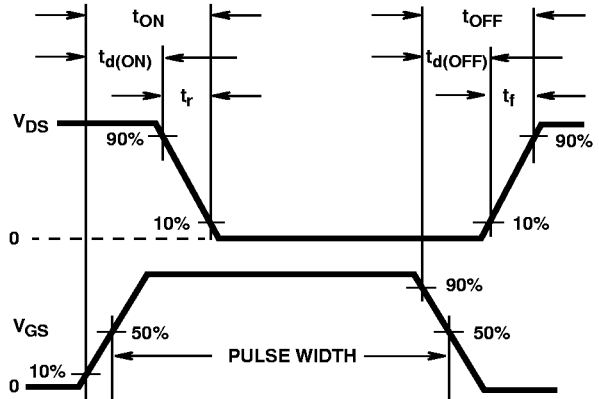


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

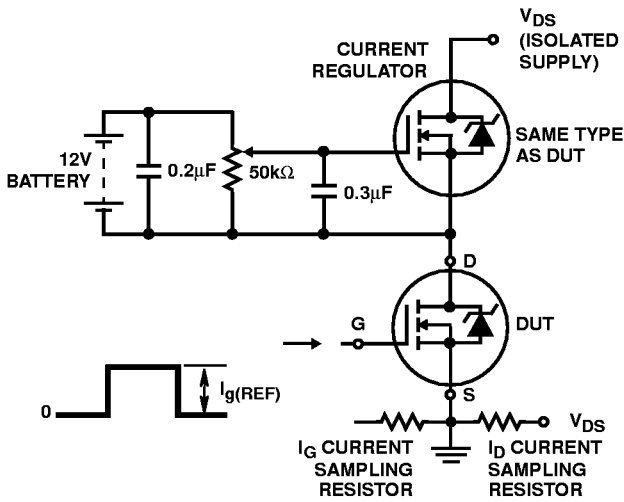


FIGURE 18. GATE CHARGE TEST CIRCUIT

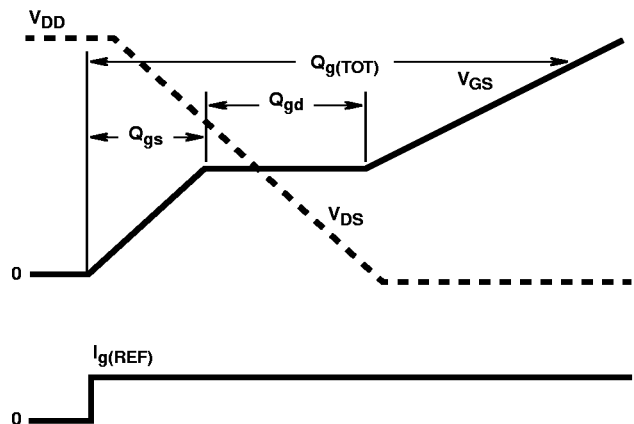


FIGURE 19. GATE CHARGE WAVEFORMS