

IRFD210, IRFD211, IRFD212, IRFD213

0.6A and 0.45A, 150V and 200V, 1.5 and 2.4 Ohm,
N-Channel Power MOSFETs

July 1998

Features

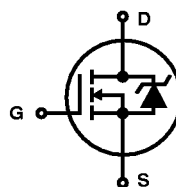
- 0.6A and 0.45A, 150V and 200V
- $r_{DS(ON)} = 1.5\Omega$ and 2.4Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Description

These are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. They can be operated directly from integrated circuits.

Formerly developmental type TA17442.

Symbol

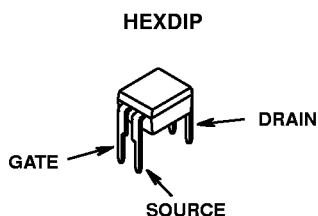


Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFD210	HEXDIP	IRFD210
IRFD211	HEXDIP	IRFD211
IRFD212	HEXDIP	IRFD212
IRFD213	HEXDIP	IRFD213

NOTE: When ordering, use the entire part number.

Packaging



IRFD210, IRFD211, IRFD212, IRFD213

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

	IRFD210	IRFD211	IRFD212	IRFD213	UNITS
Drain to Source Voltage (Note 1)	V_{DS} 200	150	200	150	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR} 200	150	200	150	V
Continuous Drain Current	I_D 0.6	0.6	0.45	0.45	A
Pulsed Drain Current	I_{DM} 2.5	2.5	1.8	1.8	A
Gate to Source Voltage	V_{GS} ± 20	± 20	± 20	± 20	V
Maximum Power Dissipation	P_D 1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 1)	0.008	0.008	0.008	0.008	W/°C
Single Pulse Avalanche Energy Rating	E_{AS} 30	30	30	30	mJ
Operating and Storage Temperature	T_J, T_{STG} -55 to 150	-55 to 150	-55 to 150	-55 to 150	°C
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s	T_L 300	300	300	300	°C
Package Body for 10s, See Techbrief 334	T_{pkg} 260	260	260	260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

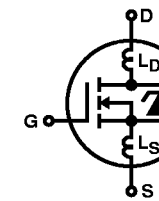
1. $T_J = 25^{\circ}\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

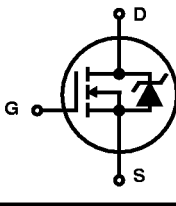
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage IRFD210, IRFD212	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ (Figure 9)	200	-	-	V
IRFD211, IRFD213			150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	25	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$ $T_C = 125^{\circ}\text{C}$	-	-	250	μA
On-State Drain Current (Note 2) IRFD210, IRFD211	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, V_{GS} = 10\text{V}$	0.6	-	-	A
IRFD212, IRFD213			0.45	-	-	A
Gate to Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Drain to Source On Resistance (Note 2) IRFD210, IRFD211	$r_{DS(ON)}$	$I_D = 0.3\text{A}, V_{GS} = 10\text{V}$ (Figures 7, 8)	-	1.0	1.5	Ω
IRFD212, IRFD213			-	1.5	2.4	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, I_D = 0.3\text{A}$	0.5	0.8	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 0.5 \times \text{Rated } BV_{DSS}, I_D \approx 0.6\text{A}, R_L = 9.1\Omega$ $R_L = 165\Omega$ for $BV_{DSS} = 200\text{V}$ $R_L = 124\Omega$ for $BV_{DSS} = 150\text{V}$ (Figures 16, 17) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	8.0	15	ns
Rise Time	t_r		-	15	25	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	10	15	ns
Fall Time	t_f		-	8.0	15	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = 10\text{V}, I_D \approx 0.6\text{A}, V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ $I_{g(REF)} = 1.5\text{mA}$ (Figures 13, 18, 19) Gate Charge is Essentially Independent of Oper- ating Temperature	-	5.0	7.5	nC
Gate to Source Charge	Q_{gs}		-	2.0	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	3.0	-	nC
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$ (Figure 10)	-	135	-	pF
Output Capacitance	C_{OSS}		-	60	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	16	-	pF

IRFD210, IRFD211, IRFD212, IRFD213

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Internal Drain Inductance	L _D	Measured From the Drain Lead, 2mm (0.08in) from Package to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	4.0	-	nH
Internal Source Inductance	L _S	Measured From the Source Lead, 2mm (0.08in) From Header to Source Bonding Pad		-	6.0	-	nH
Thermal Resistance Junction to Ambient	R _{θJA}	Free Air Operation		-	-	120	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Sym- bol Showing the Integral Reverse P-N Junction Diode		-	-	0.6	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	2.5	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = 0.6\text{A}$, $V_{GS} = 0\text{V}$, (Figure 12)		-	-	2.0	V
Reverse Recovery Time	t_{rr}	$T_J = 150^{\circ}\text{C}$, $I_{SD} = 0.6\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		-	290	-	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^{\circ}\text{C}$, $I_{SD} = 0.6\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		-	2.0	-	μC

NOTES:

- Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- $V_{DD} = 20\text{V}$, starting $T_J = 25^\circ\text{C}$, $L = 112.7\mu\text{H}$, $R_G = 50\Omega$, peak $I_{AS} = 2.2\text{A}$. See Figures 14, 15.

Typical Performance Curves Unless Otherwise Specified

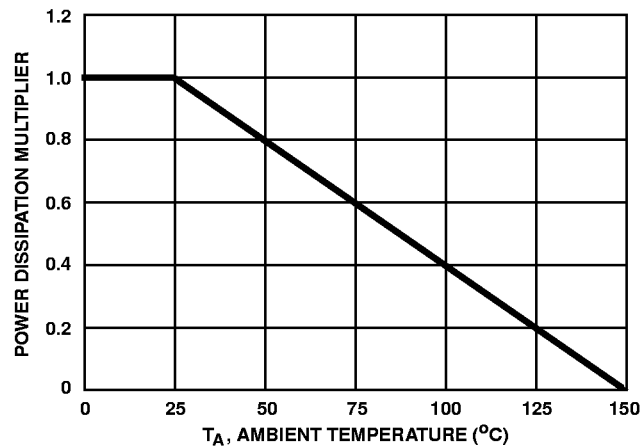


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

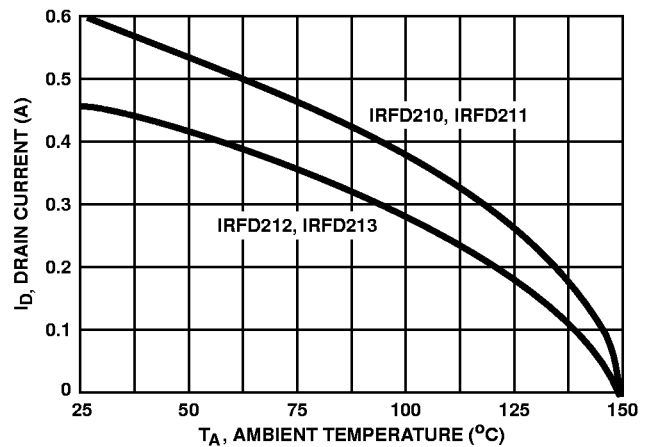


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

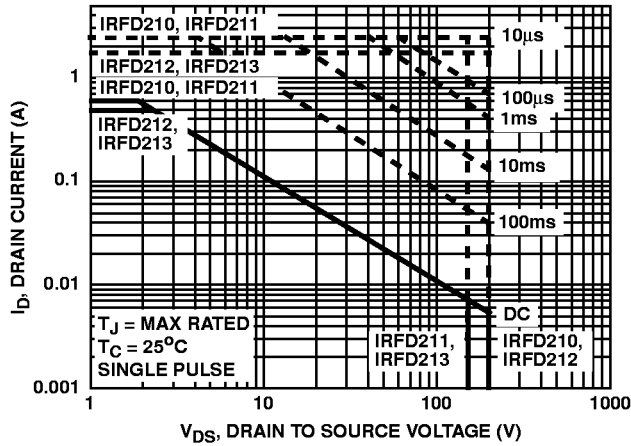


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

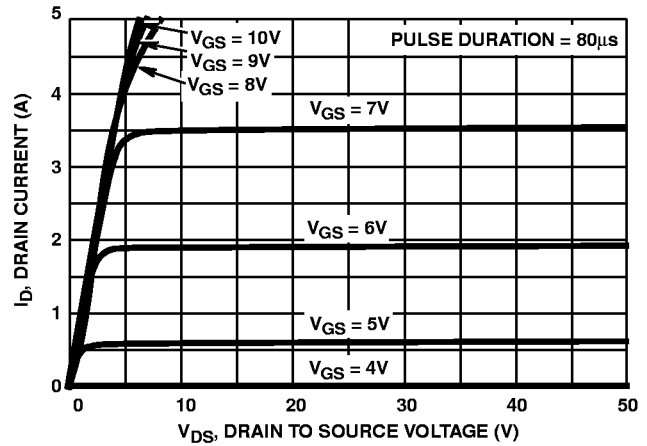


FIGURE 4. OUTPUT CHARACTERISTICS

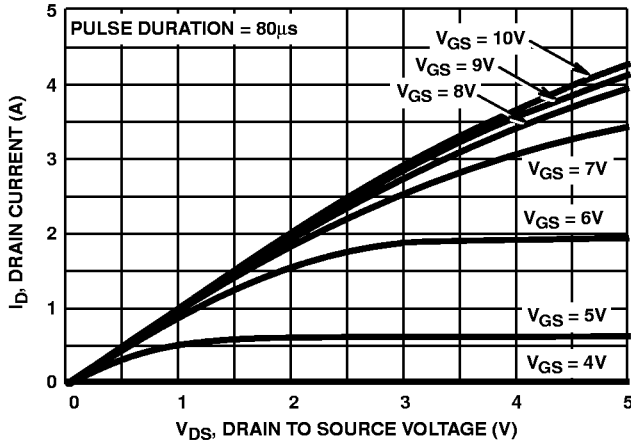


FIGURE 5. SATURATION CHARACTERISTICS

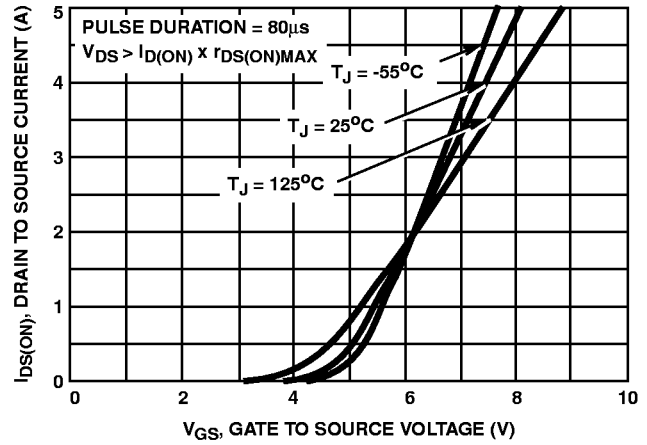
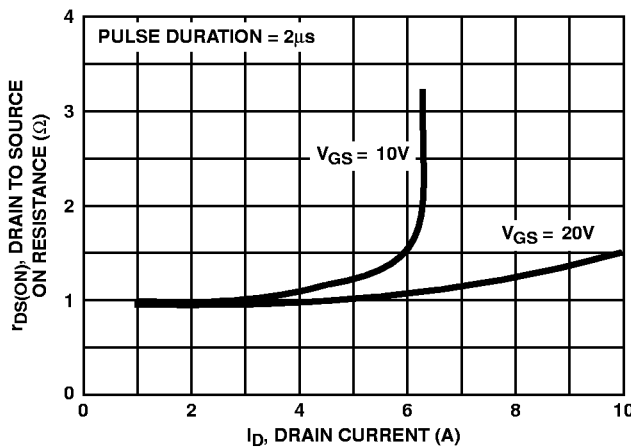


FIGURE 6. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2µs pulse is minimal.

FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

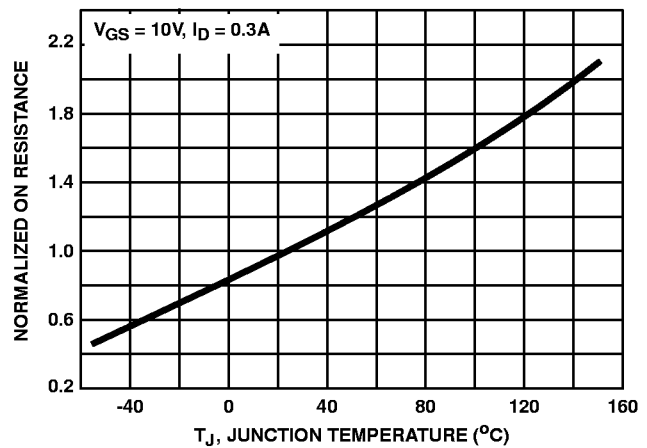


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

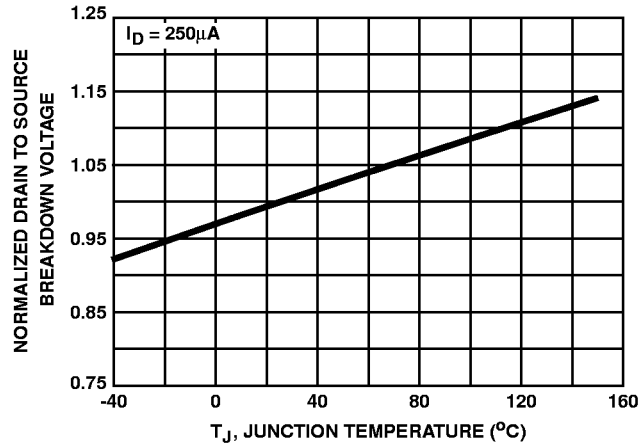


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

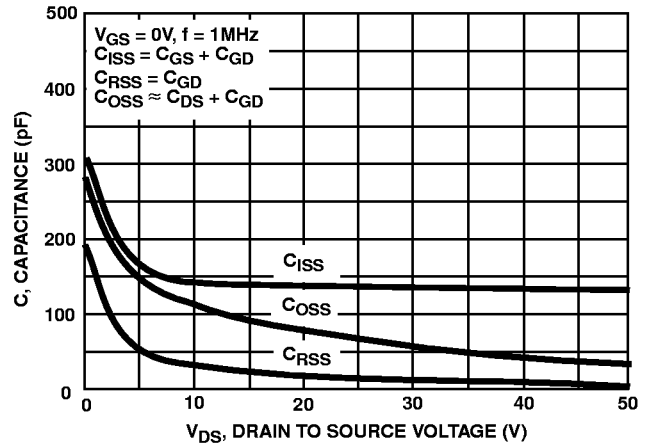


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

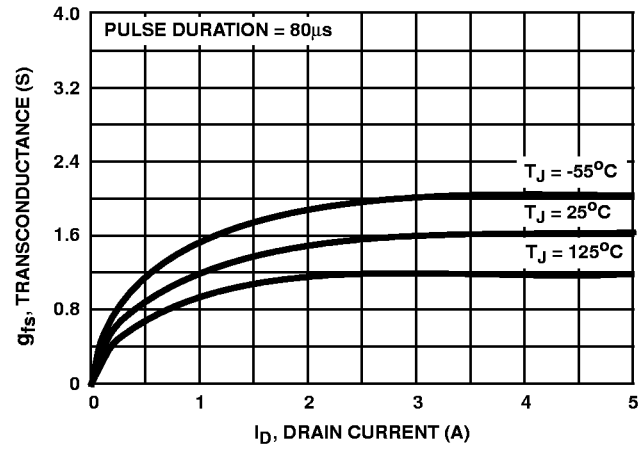


FIGURE 11. TRANSCONDUCTANCE vs DRAIN CURRENT

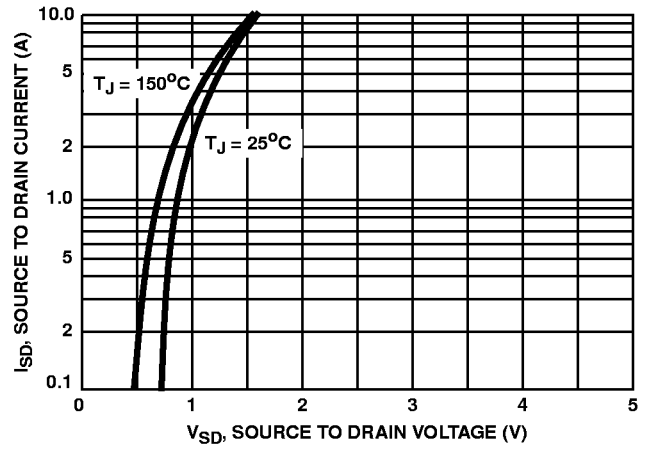


FIGURE 12. SOURCE TO DRAIN DIODE VOLTAGE

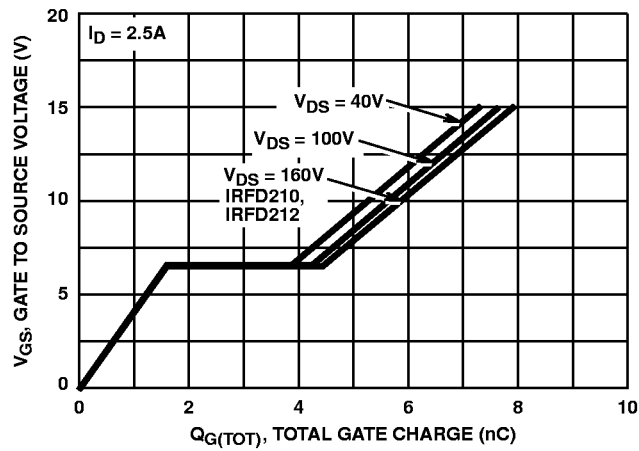


FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

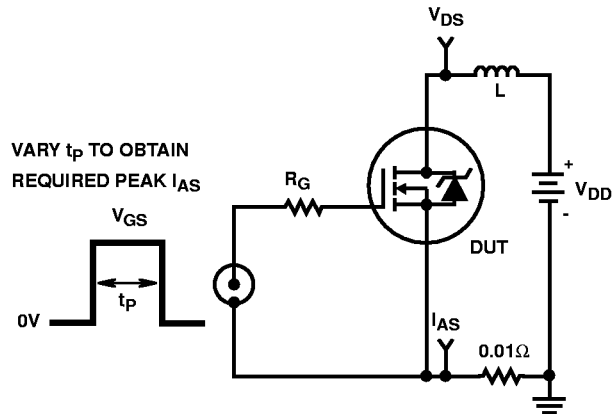


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

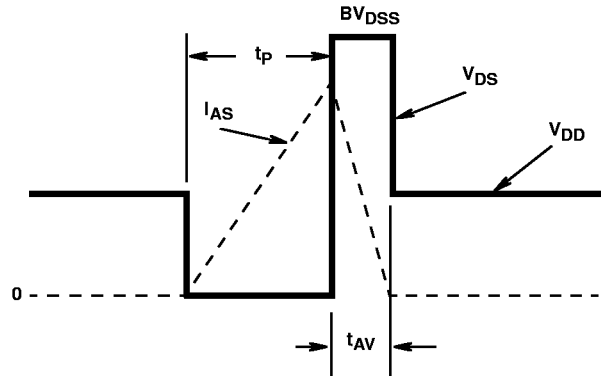


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

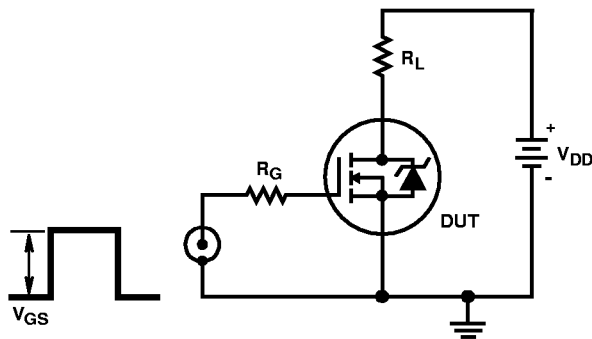


FIGURE 16. SWITCHING TIME TEST CIRCUIT

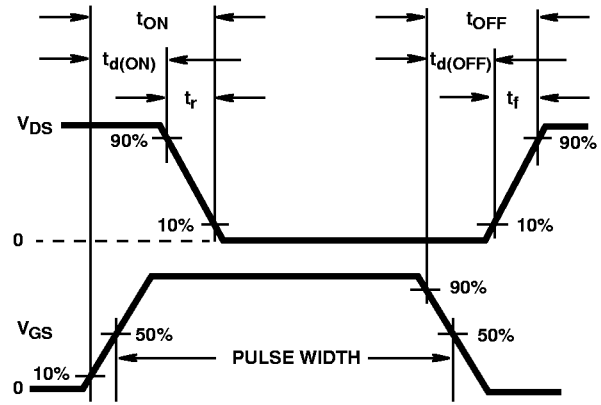


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

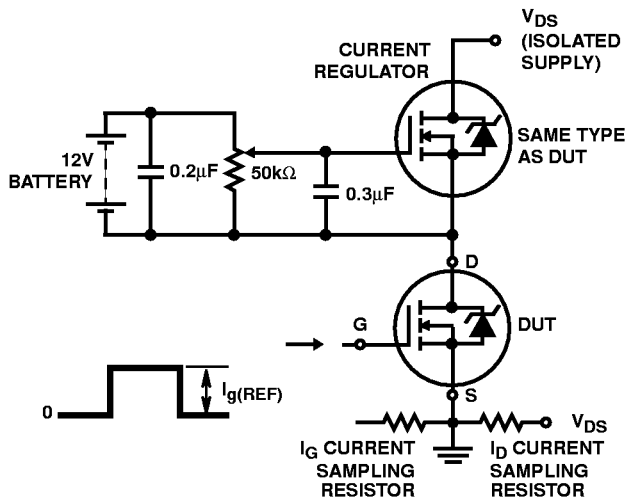


FIGURE 18. GATE CHARGE TEST CIRCUIT

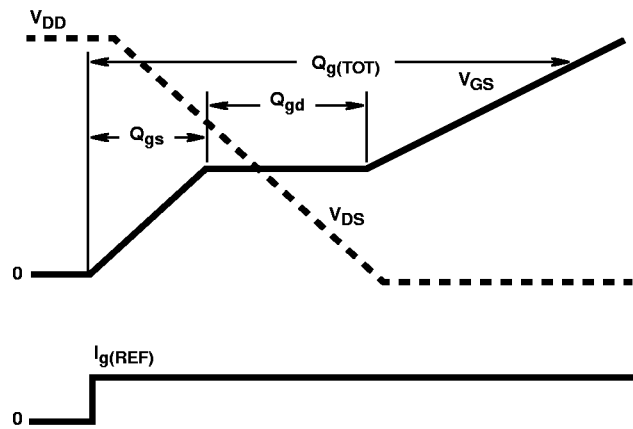


FIGURE 19. GATE CHARGE WAVEFORMS