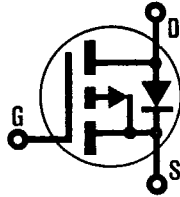


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HEXFET® TRANSISTORS IRFD9020 P-CHANNEL HEXDIP™ IRFD9022

1-WATT RATED POWER MOSFETS
IN A 4-PIN, DUAL-IN-LINE PACKAGE



4-PIN DIP

-50 Volt, 0.28 Ohm, 1-Watt HEXDIP

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for application which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

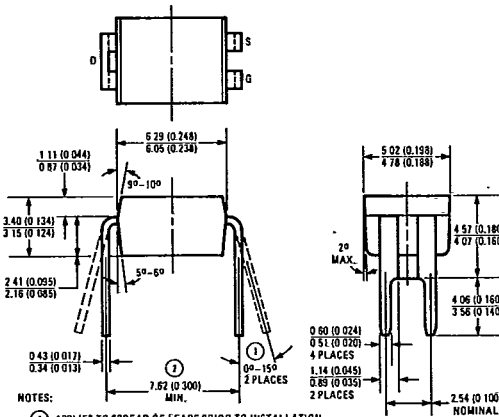
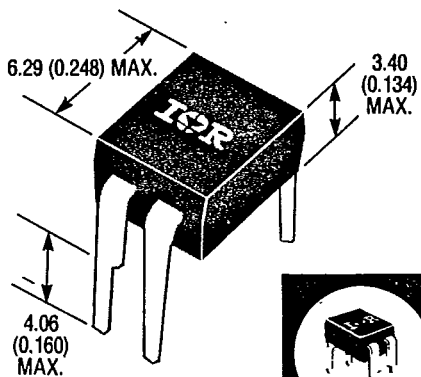
Features

- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- Excellent Temperature Stability
- P-Channel Versatility

Product Summary

Part Number	V _{DS}	R _{DS(on)}	I _D
IRFD9020	-50V	0.28Ω	-1.6
IRFD9022	-50V	0.33Ω	-1.4

CASE STYLE AND DIMENSIONS



- NOTES:
 ① APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION.
 ② APPLIES TO INSTALLED LEAD CENTERS

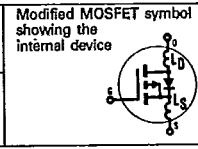
Case Style HD-1 (Similar to JEDEC Outline MO-001AN)
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings

Parameter	IRFD9020	IRFD9022	Units
V _{DS} Drain - Source Voltage ①	-50	-50	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 20 K Ω) ①	-50	-50	V
I _D @ T _C = 25°C Continuous Drain Current	-1.6	-1.4	A
I _D @ T _C = 100°C Continuous Drain Current	-0.99	-1.1	A
I _{DM} Pulsed Drain Current ②	-13	-11	A
V _{GS} Gate - Source Voltage	±20		V
P _D @ T _C = 25°C Max. Power Dissipation	1		W
Linear Derating Factor	0.0080		W/K ③
I _{LM} Inductive Current, Clamped	-13 (See Fig. 14) L = 100 μ H	-11	A
I _L Unclamped Inductive Current (Avalanche Current) ③	(See Fig. 15) -2.2		A
T _J Operating Junction and Storage Temperature Range	-55 to 150		°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain - Source Breakdown Voltage	IRFD9020 IRFD9022	-50	-	-	V	V _{GS} = 0V I _D = -250 μ A
V _{GS(th)} Gate Threshold Voltage	ALL	-2.0	-	-4.0	V	V _{DS} = V _{GS} , I _D = -250 μ A
I _{GSS} Gate-Source Leakage Forward	ALL	-	-	-500	nA	V _{GS} = -20V
I _{GSS} Gate-Source Leakage Reverse	ALL	-	-	500	nA	V _{GS} = 20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	-	-	-250 -1000	μ A	V _{DS} = Max. Rating, V _{GS} = 0V V _{DS} = Max. Rating \times 0.8, V _{GS} = 0V, T _C = 125°C
I _{D(on)} On-State Drain Current ④	IRFD9020 IRFD9022	-1.6 -1.4	-	-	A	V _{DS} > I _{D(on)} \times R _{DSON(max)} , V _{GS} = -10V
R _{DSON} Static Drain-Source On-State Resistance ④	IRFD9020 IRFD9022	-	0.20 0.28	0.28 0.33	Ω	V _{GS} = -10V, I _D = -1.1A
g _{fs} Forward Transconductance ④	ALL	1.3	1.4	-	S(0)	V _{DS} = 2 \times V _{GS} , I _D = -1.1A
C _{iss} Input Capacitance	ALL	-	480	-	pF	V _{GS} = 0V, V _{DS} = -25V, f = 1.0 MHz
C _{oss} Output Capacitance	ALL	-	320	-	pF	See Fig. 10
C _{rss} Reverse Transfer Capacitance	ALL	-	58	-	pF	
t _{d(on)} Turn-On Delay Time	ALL	-	8.2	12	ns	V _{DD} = -25V, I _D = -9.7A, R _G = 18 Ω , R _D = 2.4 Ω
t _r Rise Time	ALL	-	57	86	ns	See Fig. 16
t _{d(off)} Turn-Off Delay Time	ALL	-	12	18	ns	(MOSFET switching times are essentially independent of operating temperature.)
t _f Fall Time	ALL	-	25	38	ns	
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	-	17	26	nC	V _{GS} = -10V, I _D = -9.7A, V _{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _{gs} Gate-Source Charge	ALL	-	4.1	6.2	nC	
Q _{gd} Gate-Drain ("Miller") Charge	ALL	-	5.7	8.6	nC	
L _D Internal Drain Inductance	ALL	-	4.0	-	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L _S Internal Source Inductance	ALL	-	6.0	-	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.



Thermal Resistance

R _{thJA} Junction-to-Ambient	ALL	-	-	120	K/W ⑤	Typical socket mount
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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD9020	-	-	-1.6	A	Modified MOSFET symbol showing the integral reverse PN junction rectifier.
		IRFD9022	-	-	-1.4	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFD9020	-	-	-13	A	
		IRFD9022	-	-	-11	A	
V_{SD}	Diode Forward Voltage ②	ALL	-	-	-6.3	V	$T_C = 25^\circ\text{C}, I_S = -1.6\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	56	110	280	ns	$T_J = 25^\circ\text{C}, I_F = -9.7\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	0.17	0.34	0.85	μC	$T_J = 25^\circ\text{C}, I_F = -9.7\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25^\circ\text{C}$ to 150°C ② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
 ③ $V_{dd} = -25\text{V}, T_J = 25^\circ\text{C}$ ④ Pulse Test: Pulse width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$
 ⑤ $K/W = ^\circ\text{C}/\text{W}$ $L = 100 \mu\text{H}, R_G = 25\Omega$

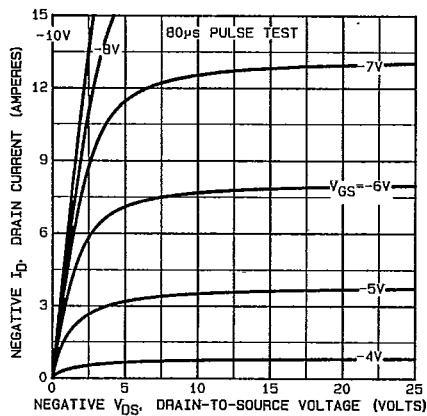


Fig. 1 — Typical Output Characteristics

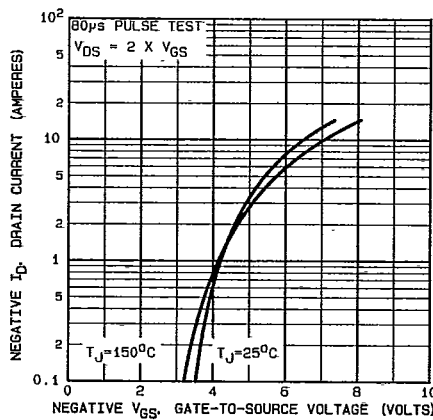


Fig. 2 — Typical Transfer Characteristics

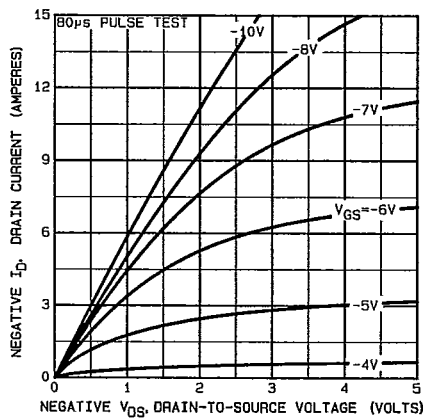


Fig. 3 — Typical Saturation Characteristics

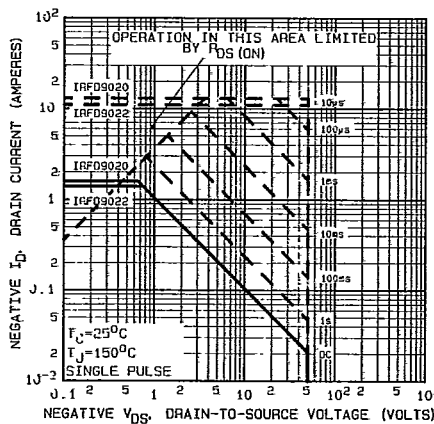
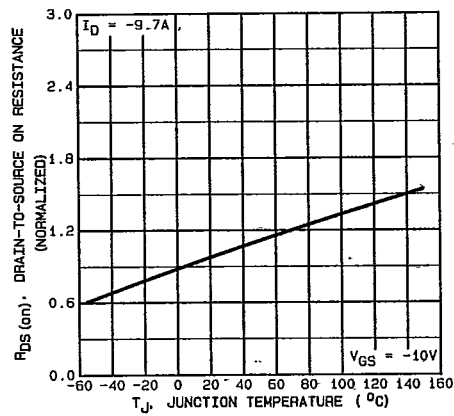
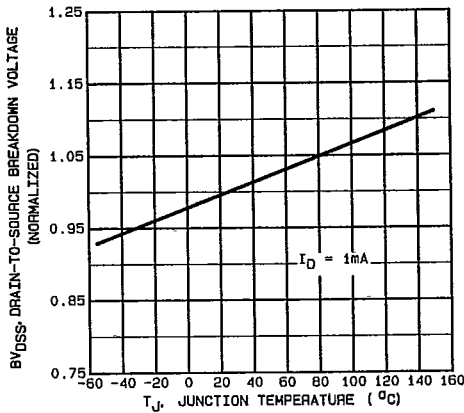
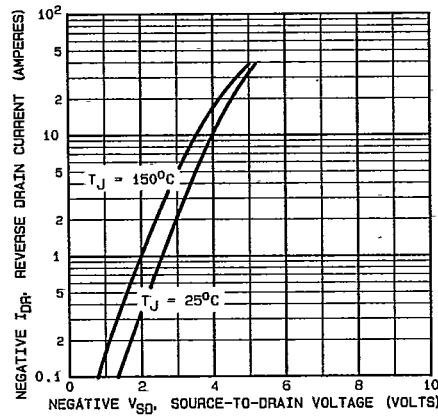
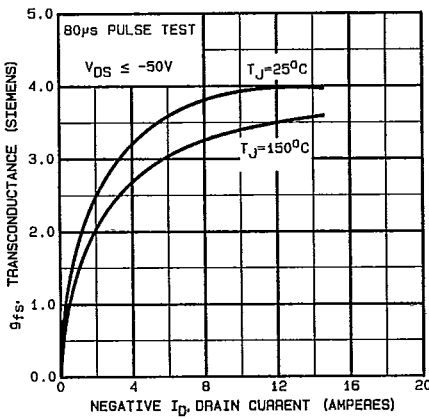
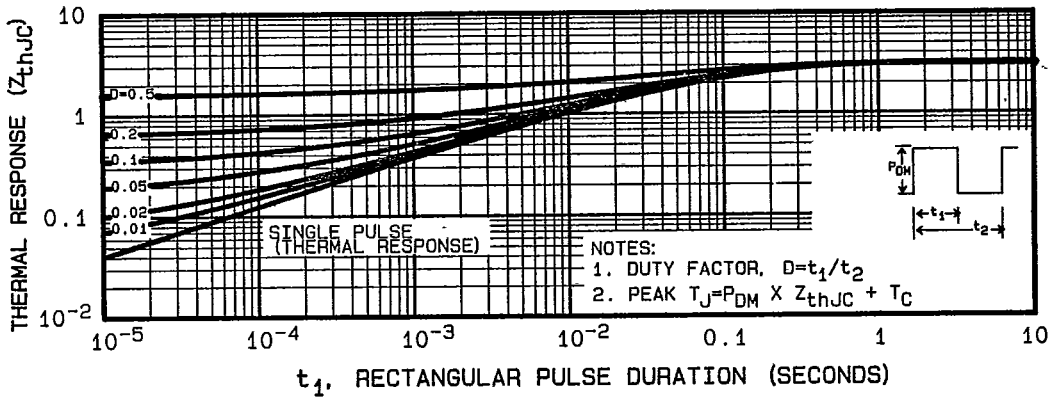


Fig. 4 — Maximum Safe Operating Area





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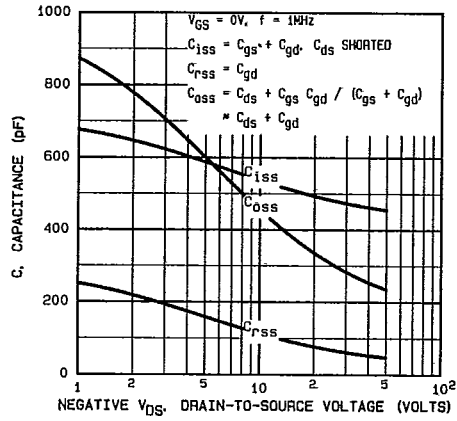


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

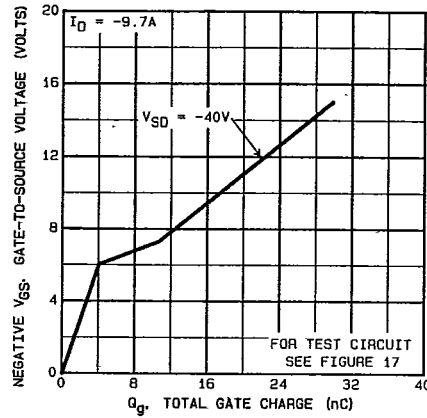


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

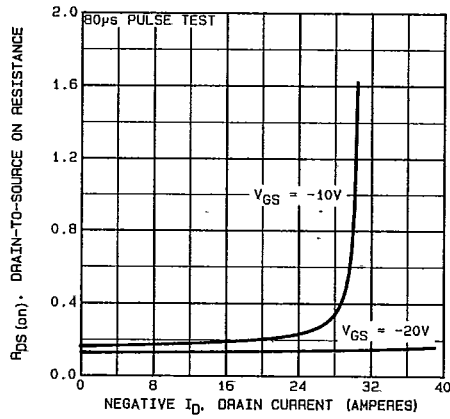


Fig. 12 — Typical On-Resistance Vs. Drain Current

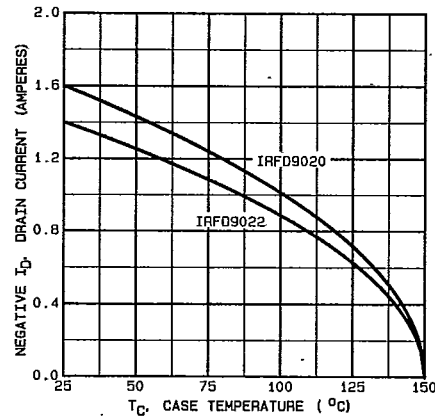


Fig. 13 — Maximum Drain Current Vs. Case Temperature

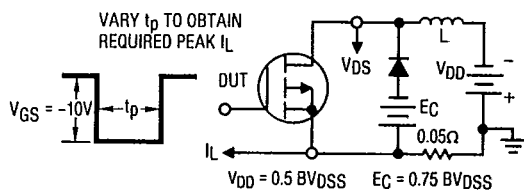


Fig. 14a — Clamped Inductive Test Circuit

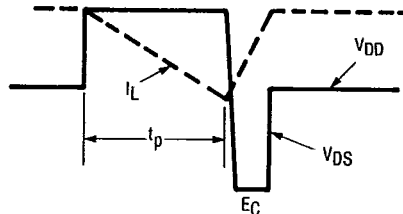


Fig. 14b — Clamped Inductive Waveforms

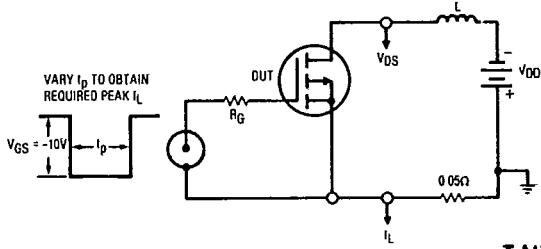


Fig. 15a — Unclamped Inductive Test Circuit

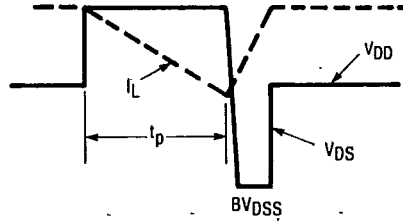


Fig. 15b — Unclamped Inductive Load Test Waveforms

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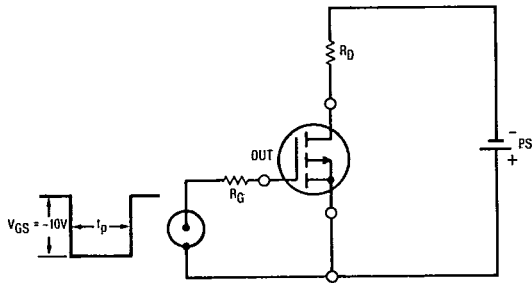


Fig. 16 — Switching Time Test Circuit

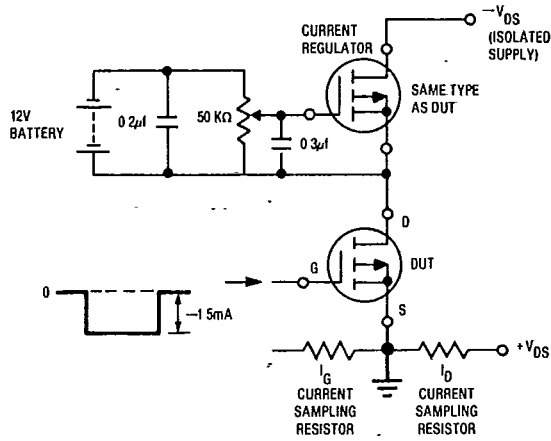
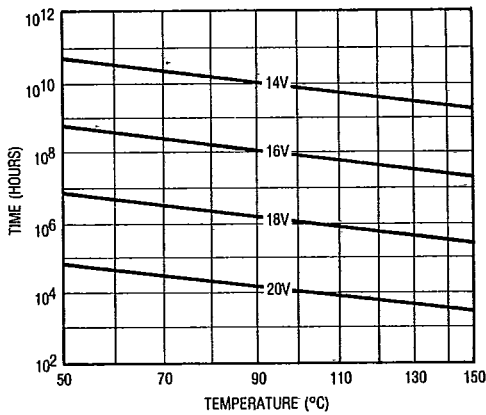
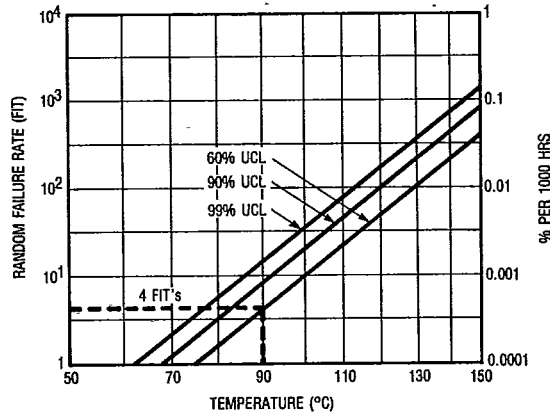


Fig. 17 — Gate Charge Test Circuit



*Fig. 18 — Typical Time to Accumulated 1% Gate Failure



*Fig. 19 — Typical High Temperature Reverse Bias (HTRB) Failure Rate

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.