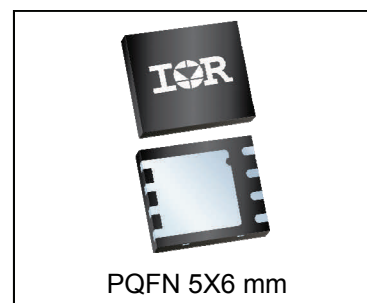
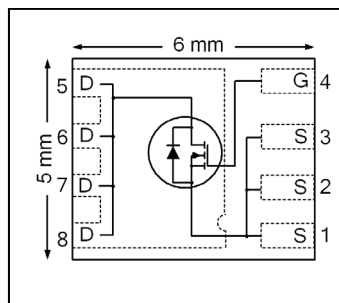


HEXFET® Power MOSFET

V_{DSS}	100	V
R_{DS(on)} max (@ V _{GS} = 10V)	3.9	mΩ
Q_g (typical)	49	nC
R_g (typical)	0.9	Ω
I_D (@T _{C (Bottom)} = 25°C)	157	A



Applications

- Optimized for Secondary Side Synchronous Rectification
- Primary Switch for High Frequency 48V/60V Telecom DC-DC Power Supplies
- Hot Swap and Active O-Ring
- BLDC Motor Drive

Features

Low R _{DS(ON)} (<3.9mΩ)
Low Thermal Resistance to PCB (<0.64°C/W)
100% R _g Tested
Low Profile (<1.05 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant, Halogen-Free
MSL1

results in
⇒

Benefits

Lower Conduction Losses
Increased Power Density
Increased Reliability
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH7182PbF	PQFN 5mm x 6 mm	Tape and Reel	4000	IRFH7182TRPbF

Absolute Maximum Ratings

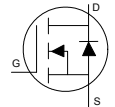
	Parameter	Max.	Units
V _{GS}	Gate-to-Source Voltage	± 20	V
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	23	A
I _D @ T _{C(Bottom)} = 25°C	Continuous Drain Current, V _{GS} @ 10V	157	
I _D @ T _{C(Bottom)} = 100°C	Continuous Drain Current, V _{GS} @ 10V	99	
I _{DM}	Pulsed Drain Current ①	320	
P _D @ T _A = 25°C	Power Dissipation	4.0	W
P _D @ T _{C(Bottom)} = 25°C	Power Dissipation	195	
	Linear Derating Factor	0.03	W/°C
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		

Notes ① through ⑤ are on page 8

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	62	—	mV/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.1	3.9	m Ω	$V_{GS} = 10V, I_D = 50A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	3.6	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-5.3	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 80V, V_{GS} = 0V$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	135	—	—	S	$V_{DS} = 25V, I_D = 50A$
Q_g	Total Gate Charge	—	49	74	nC	$V_{DS} = 50V$ $V_{GS} = 10V$ $I_D = 50A$
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	9.3	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	3.1	—		
Q_{gd}	Gate-to-Drain Charge	—	15.8	—		
Q_{godr}	Gate Charge Overdrive	—	21	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	19	—	nC	$V_{DS} = 50V, V_{GS} = 0V$
Q_{oss}	Output Charge	—	160	—		
R_G	Gate Resistance	—	0.9	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	6.1	—	ns	$V_{DD} = 50V, V_{GS} = 10V$ $I_D = 50A$ $R_G = 1.0\Omega$
t_r	Rise Time	—	6.2	—		
$t_{d(off)}$	Turn-Off Delay Time	—	15	—		
t_f	Fall Time	—	5.3	—		
C_{iss}	Input Capacitance	—	3120	—	pF	$V_{GS} = 0V$ $V_{DS} = 50V$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	1440	—		
C_{rss}	Reverse Transfer Capacitance	—	14	—		

Diode Characteristics

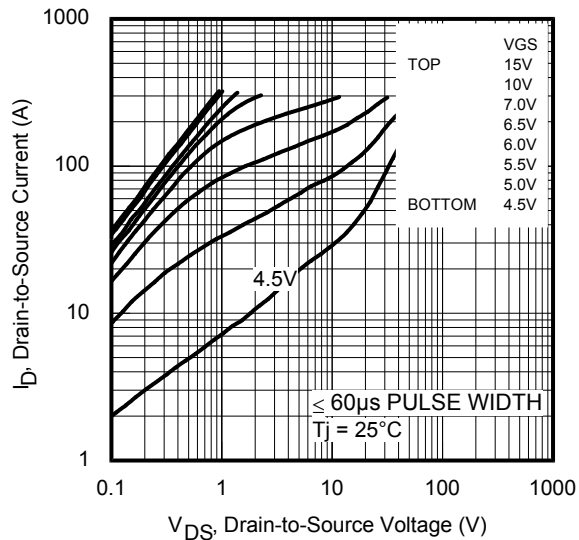
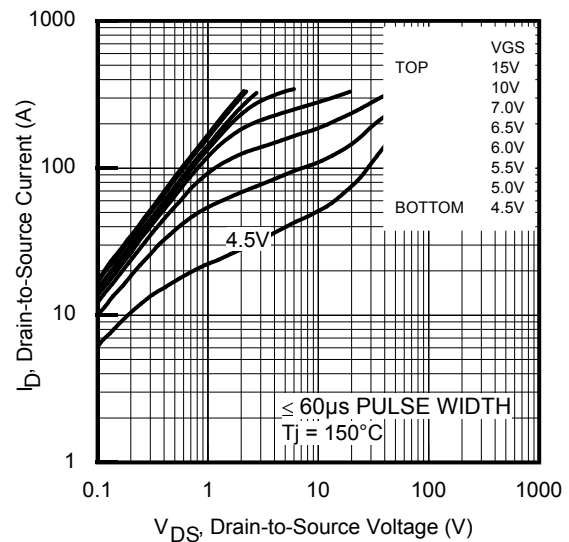
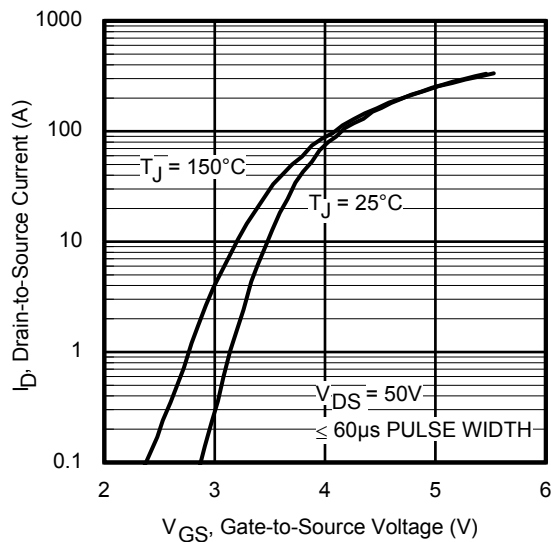
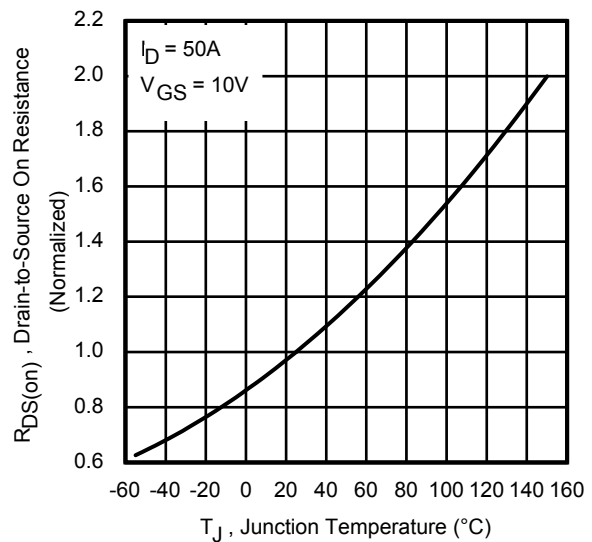
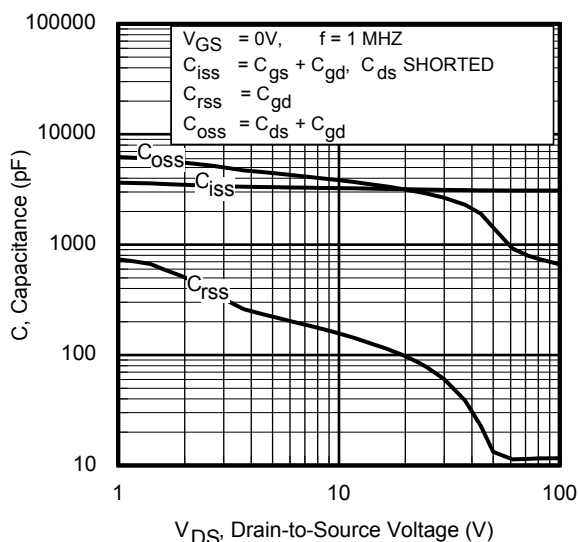
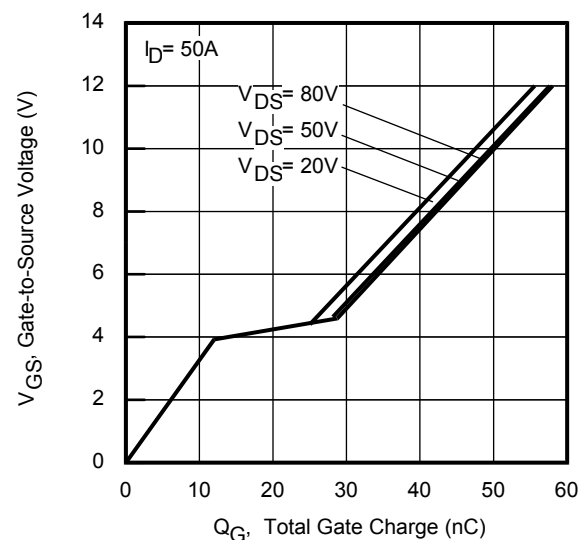
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	157	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	320		
V_{SD}	Diode Forward Voltage	—	0.8	1.3	V	$T_J = 25^\circ\text{C}, I_S = 50A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	65	98	ns	$T_J = 25^\circ\text{C}, I_F = 50A, V_{DD} = 50V$ $di/dt = 100A/\mu s$ ③
Q_{rr}	Reverse Recovery Charge	—	113	170	nC	

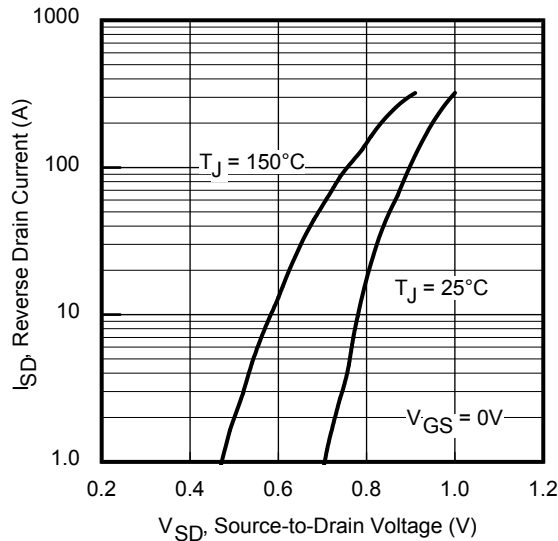
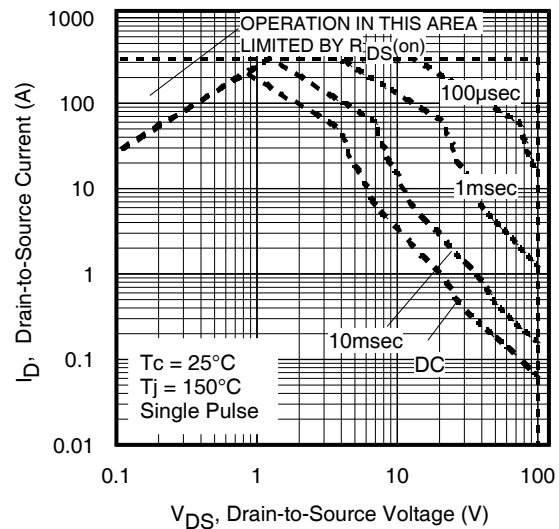
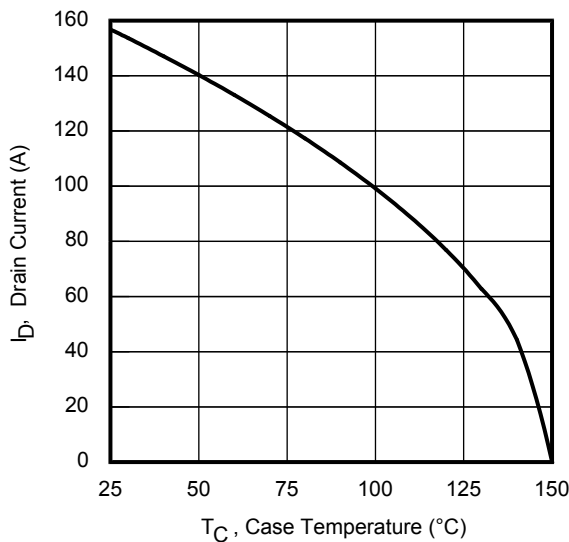
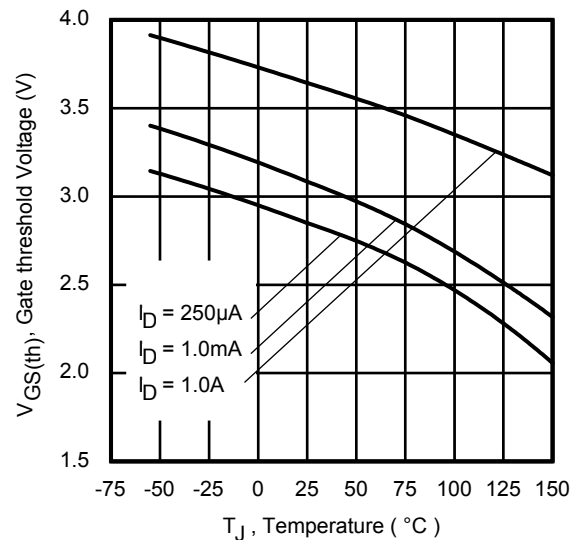
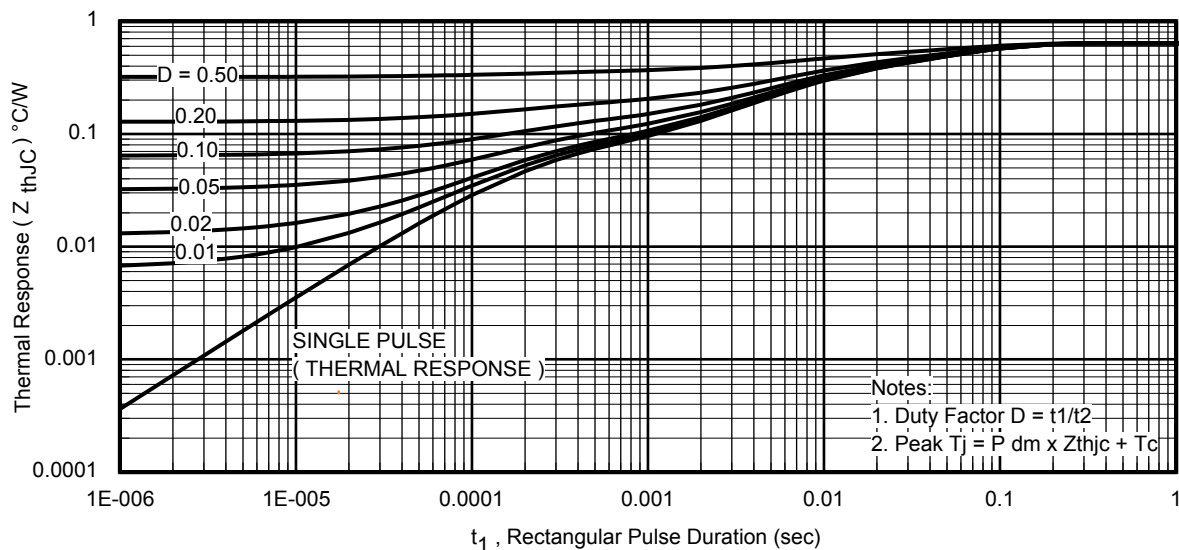
Avalanche Characteristics

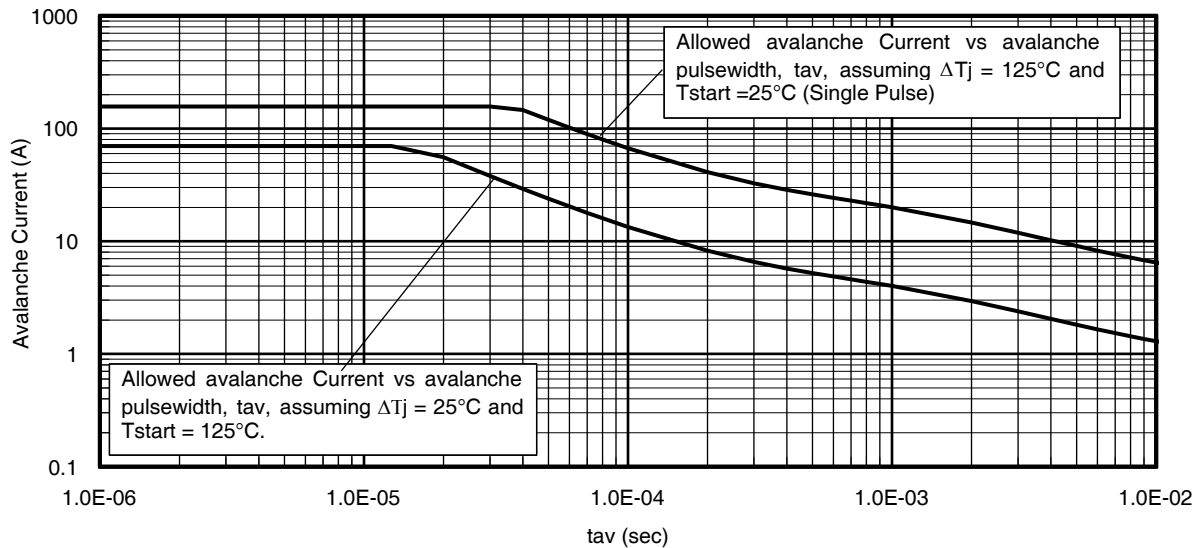
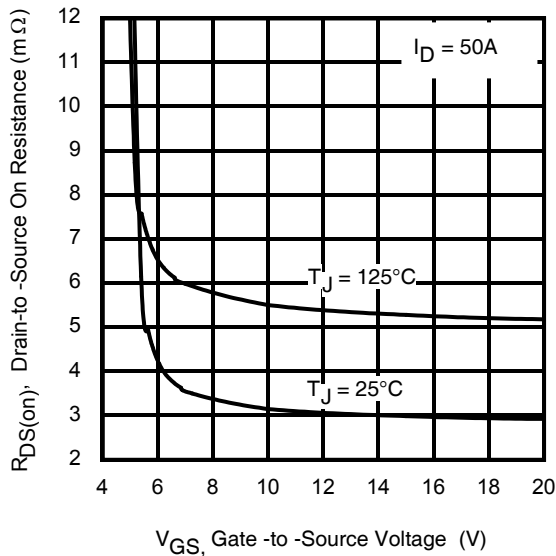
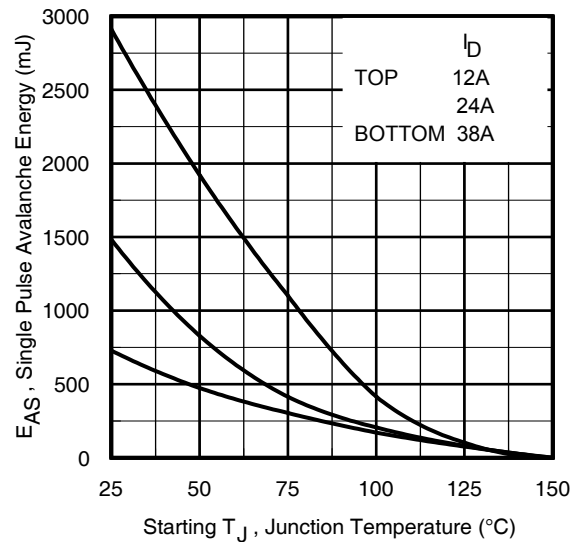
	Parameter	Typ.	Max.	Units
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	—	728	mJ
I_{AR}	Avalanche Current ①	—	38	A

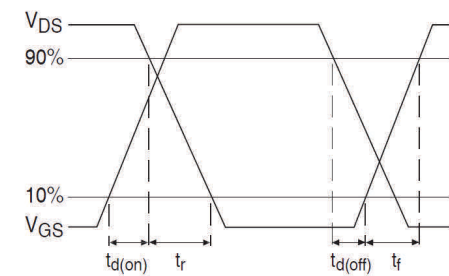
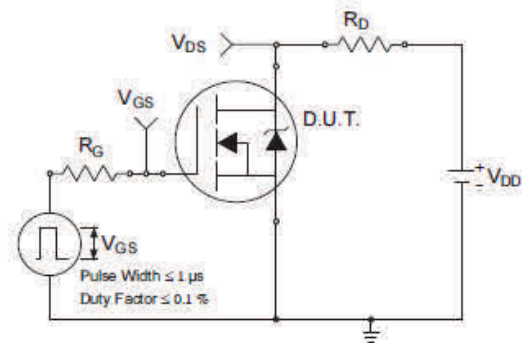
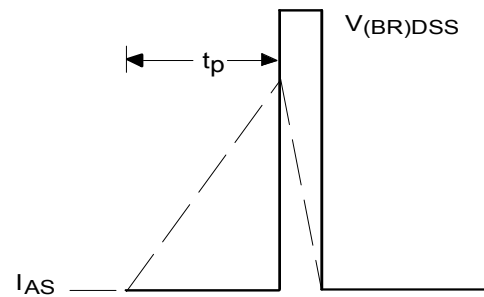
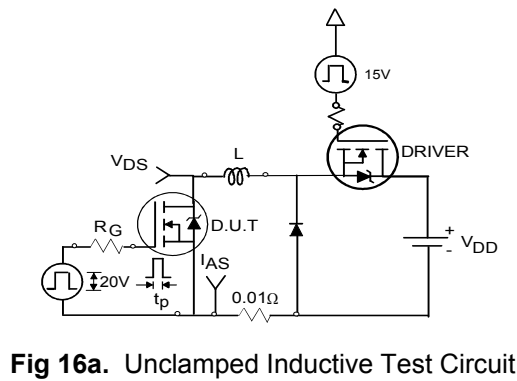
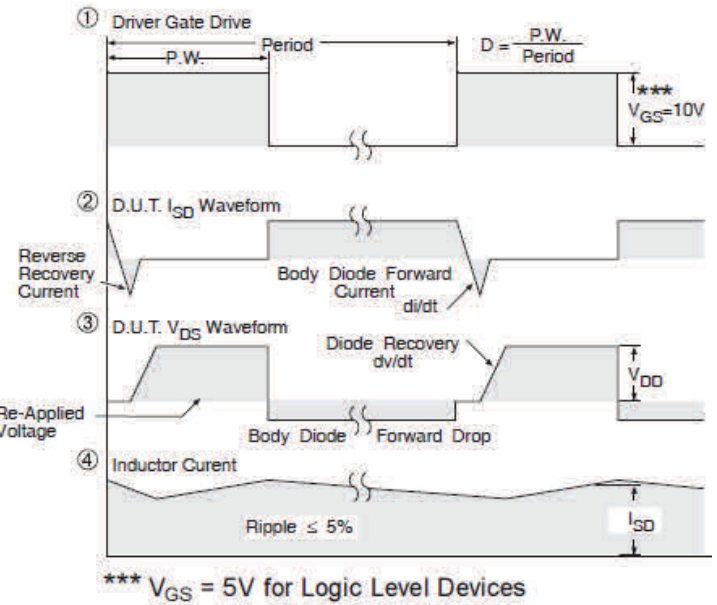
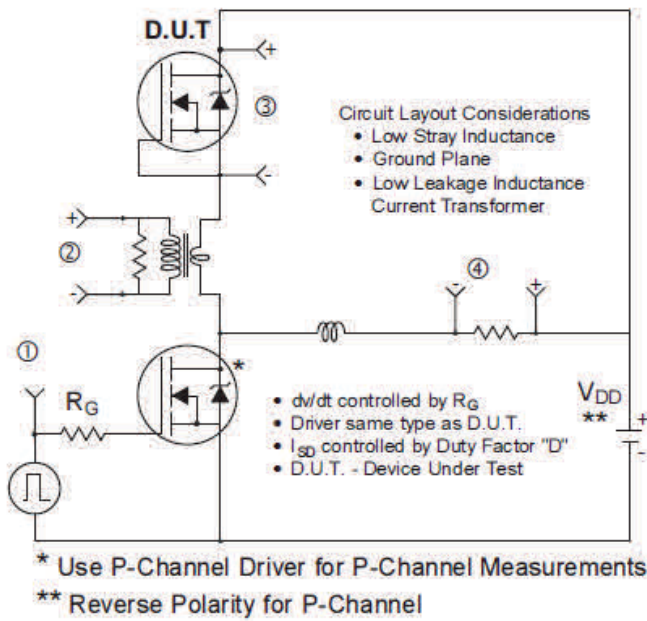
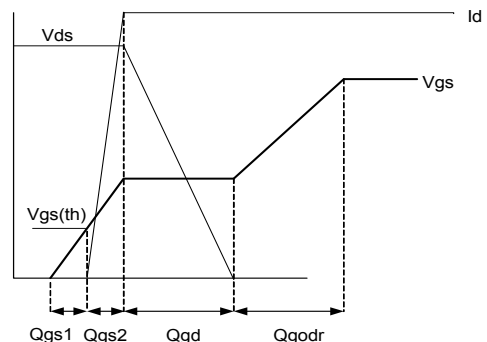
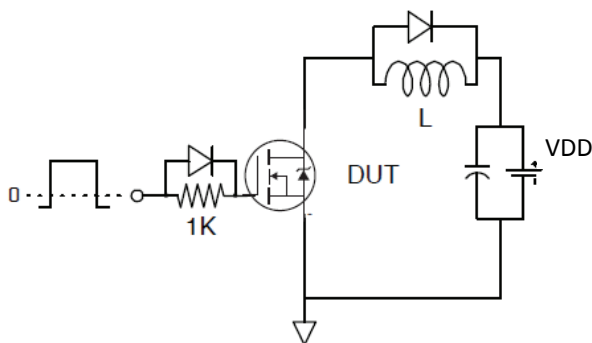
Thermal Resistance

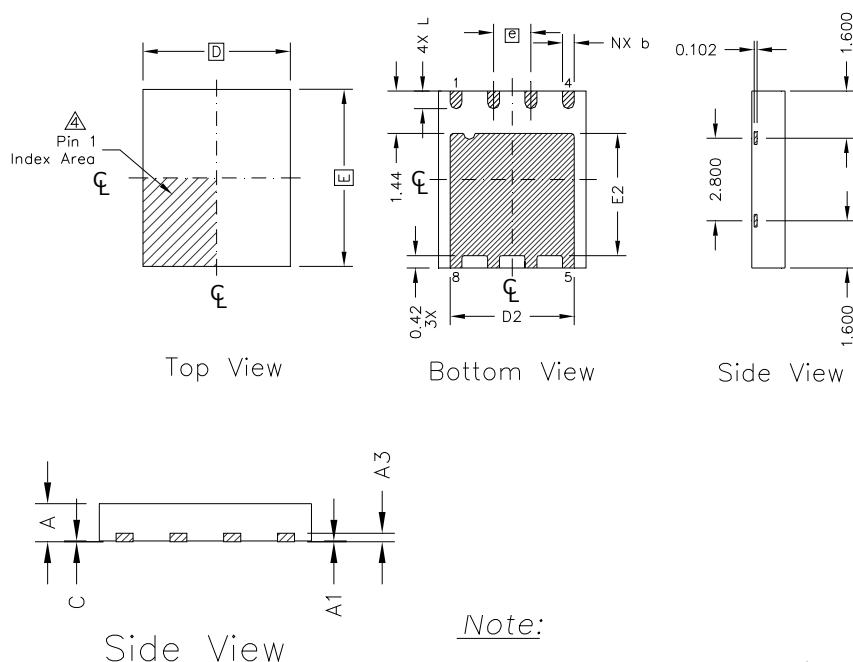
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ④	—	0.64	$^\circ\text{C}/W$
$R_{\theta JC}$ (Top)	Junction-to-Case ④	—	15	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	31	
$R_{\theta JA} (<10s)$	Junction-to-Ambient ⑤	—	19	


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12. Typical Avalanche Current vs. Pulse Width

Fig 13. On-Resistance vs. Gate Voltage

Fig 14. Maximum Avalanche Energy vs. Drain Current


Fig 17a. Switching Time Test Circuit
Fig 17b. Switching Time Waveforms

Fig 18. Gate Charge Test Circuit
Fig 19. Gate Charge Waveform

PQFN 5x6 Outline "F" Package Details


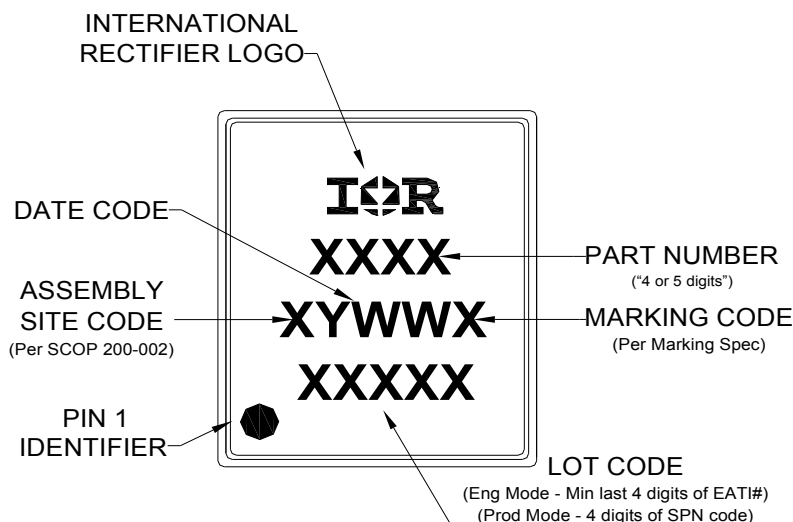
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.000	0.02	0.05
A3	0.203 Ref		
b	0.30	0.40	0.50
D	5.00 BSC		
E	6.00 BSC		
e	1.27 BSC		
D2	4.06	4.21	4.31
E2	3.988	4.138	4.238
L	0.50	0.60	0.70
aaa	0.05		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
N	8		
ND	4		

Note:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND refers to the maximum number of terminals on D side.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization.

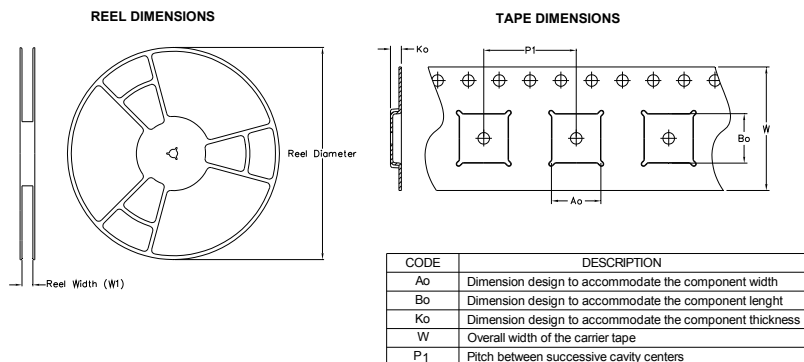
For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

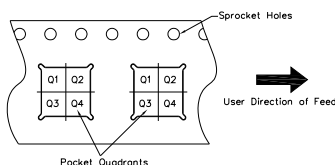
PQFN 5x6 Outline "F" Part Marking


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

PQFN 5x6 Outline "F" Tape and Reel



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F ^{††} guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D ^{††})
RoHS Compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

^{††} Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^{\circ}\text{C}$, $L = 1\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 38\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_{θ} is measured at T_J of approximately 90°C .
- ⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:
<http://www.irf.com/technical-info/appnotes/an-994.pdf>

International
 Rectifier

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To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>