

## FEATURES

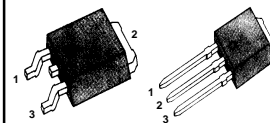
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- 175°C Operating Temperature
- Lower Leakage Current : 10  $\mu$ A (Max.) @  $V_{DS} = 60V$
- Lower  $R_{DS(ON)}$  : 0.050  $\Omega$  (Typ.)

$$BV_{DSS} = 60 V$$

$$R_{DS(on)} = 0.07 \Omega$$

$$I_D = 17 A$$

**D<sup>2</sup>-PAK I<sup>2</sup>-PAK**



1. Gate 2. Drain 3. Source

## Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	60	V
$I_D$	Continuous Drain Current ( $T_C=25^\circ C$ )	17	A
	Continuous Drain Current ( $T_C=100^\circ C$ )	12	
$I_{DM}$	Drain Current-Pulsed ①	68	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy ②	149	mJ
$I_{AR}$	Avalanche Current ①	17	A
$E_{AR}$	Repetitive Avalanche Energy ①	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
$P_D$	Total Power Dissipation ( $T_A=25^\circ C$ )*	3.8	W
	Total Power Dissipation ( $T_C=25^\circ C$ )	44	W
	Linear Derating Factor	0.29	W/ $^\circ C$
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +175	$^\circ C$
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8 " from case for 5-seconds	300	

## Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	3.43	$^\circ C / W$
$R_{\theta JA}$	Junction-to-Ambient *	--	40	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

\* When mounted on the minimum pad size recommended (PCB Mount).

### Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$BV_{DSS}$	Drain-Source Breakdown Voltage	60	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.064	--	V/ $^\circ\text{C}$	$I_D=250\mu A$ <b>See Fig 7</b>
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	$V_{DS}=5V, I_D=250\mu A$
$I_{GSS}$	Gate-Source Leakage, Forward	--	--	100	nA	$V_{GS}=20V$
	Gate-Source Leakage, Reverse	--	--	-100		$V_{GS}=-20V$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	10	$\mu A$	$V_{DS}=60V$
		--	--	100		$V_{DS}=48V, T_C=150^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.07	$\Omega$	$V_{GS}=10V, I_D=8.5A$ ④
$g_{fs}$	Forward Transconductance	--	10.8	--	$\text{S}$	$V_{DS}=30V, I_D=8.5A$ ④
$C_{iss}$	Input Capacitance	--	600	780	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ <b>See Fig 5</b>
$C_{oss}$	Output Capacitance	--	210	240		
$C_{rss}$	Reverse Transfer Capacitance	--	83	95		
$t_{d(on)}$	Turn-On Delay Time	--	13	30	ns	$V_{DD}=30V, I_D=17A,$ $R_G=18\Omega$ <b>See Fig 13</b> ④⑤
$t_r$	Rise Time	--	19	40		
$t_{d(off)}$	Turn-Off Delay Time	--	46	100		
$t_f$	Fall Time	--	48	100		
$Q_g$	Total Gate Charge	--	24	32	nC	$V_{DS}=48V, V_{GS}=10V,$ $I_D=17A$ <b>See Fig 6 &amp; Fig 12</b> ④⑤
$Q_{gs}$	Gate-Source Charge	--	4.3	--		
$Q_{gd}$	Gate-Drain( "Miller " ) Charge	--	10.8	--		

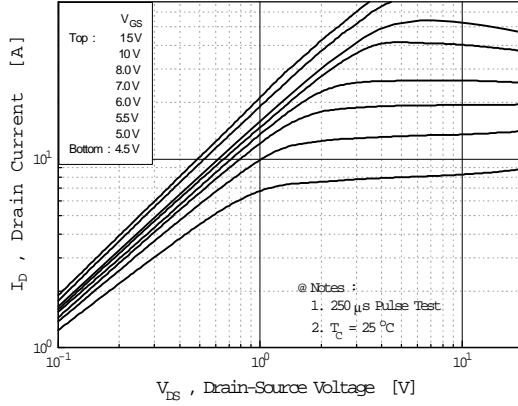
### Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$I_S$	Continuous Source Current	--	--	17	A	Integral reverse pn-diode in the MOSFET
$I_{SM}$	Pulsed-Source Current ①	--	--	68		
$V_{SD}$	Diode Forward Voltage ④	--	--	1.5	V	$T_J=25^\circ\text{C}, I_S=17A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	--	60	--	ns	$T_J=25^\circ\text{C}, I_F=17A$
$Q_{rr}$	Reverse Recovery Charge	--	0.12	--	$\mu\text{C}$	$di_F/dt=100A/\mu s$ ④

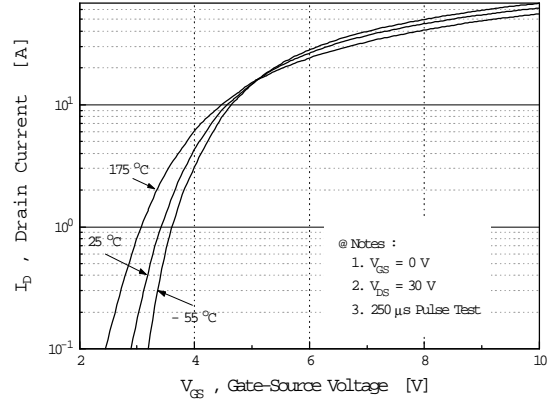
#### Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ②  $L=0.6\text{mH}, I_{AS}=17A, V_{DD}=25V, R_G=27\Omega,$  Starting  $T_J=25^\circ\text{C}$
- ③  $I_{SD}\leq 17A, di/dt\leq 250A/\mu s, V_{DD}\leq BV_{DSS},$  Starting  $T_J=25^\circ\text{C}$
- ④ Pulse Test : Pulse Width = 250  $\mu s,$  Duty Cycle  $\leq 2\%$
- ⑤ Essentially Independent of Operating Temperature

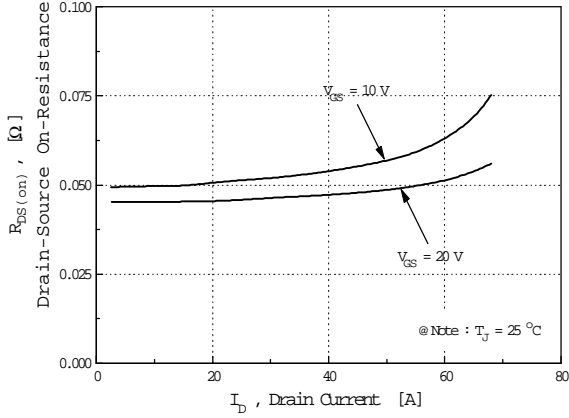
**Fig 1. Output Characteristics**



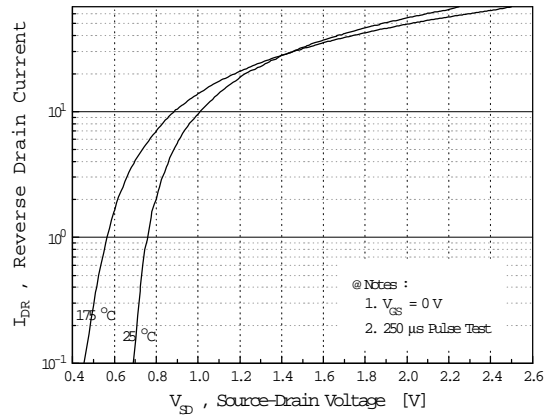
**Fig 2. Transfer Characteristics**



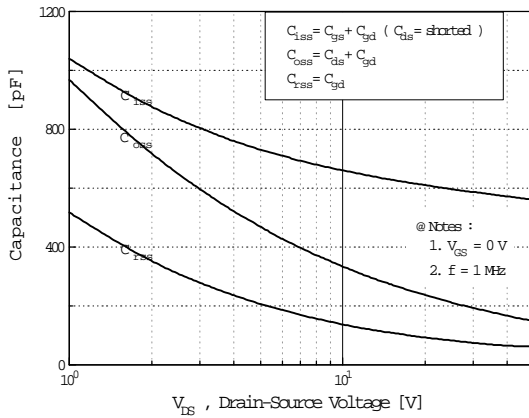
**Fig 3. On-Resistance vs. Drain Current**



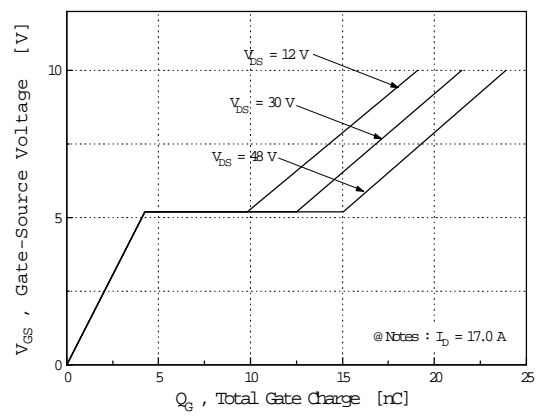
**Fig 4. Source-Drain Diode Forward Voltage**



**Fig 5. Capacitance vs. Drain-Source Voltage**



**Fig 6. Gate Charge vs. Gate-Source Voltage**



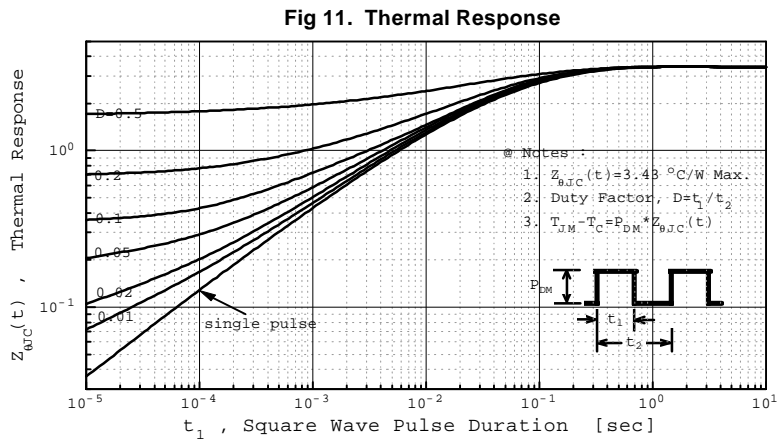
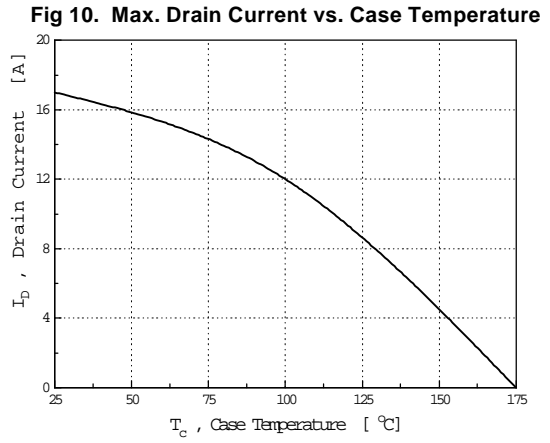
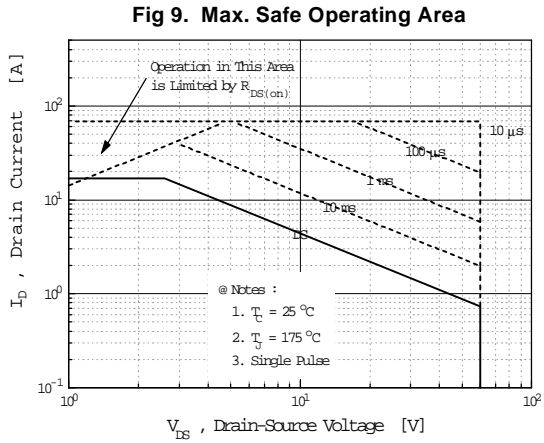
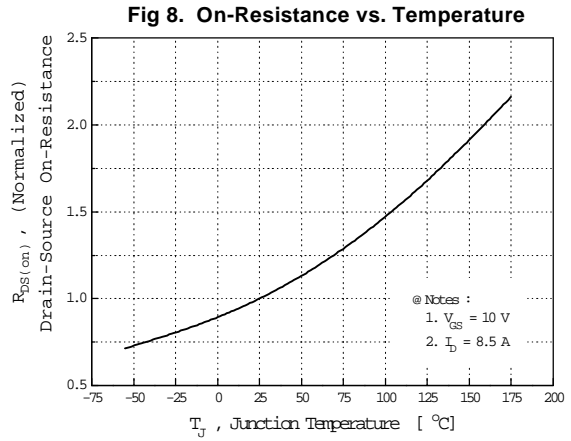
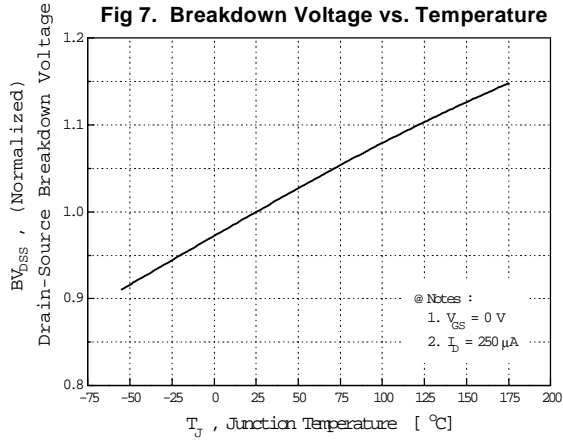


Fig 12. Gate Charge Test Circuit & Waveform

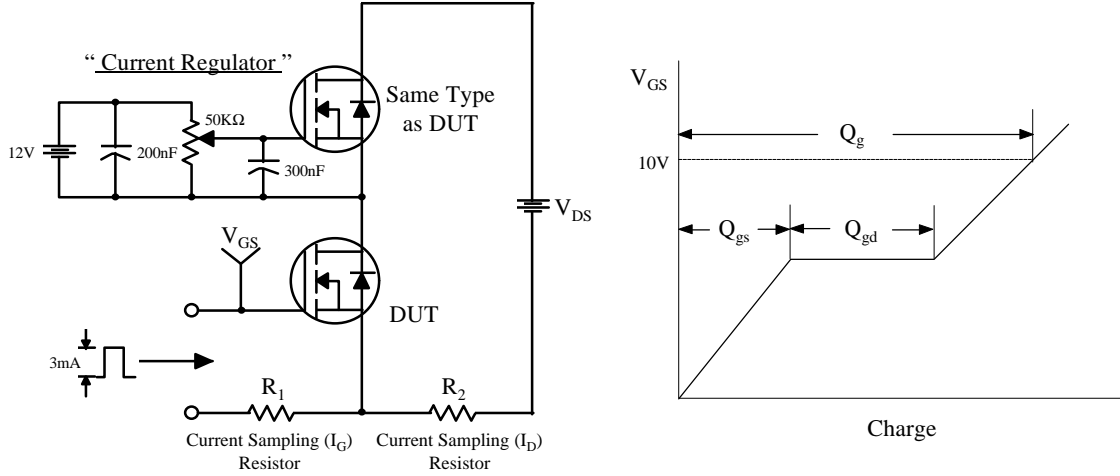


Fig 13. Resistive Switching Test Circuit & Waveforms

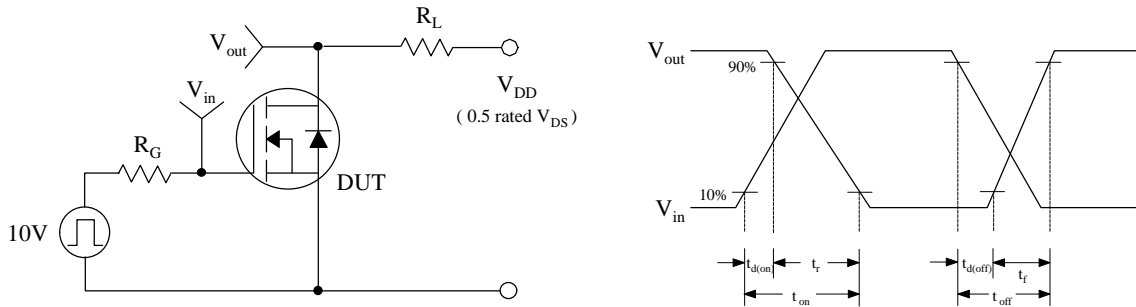


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

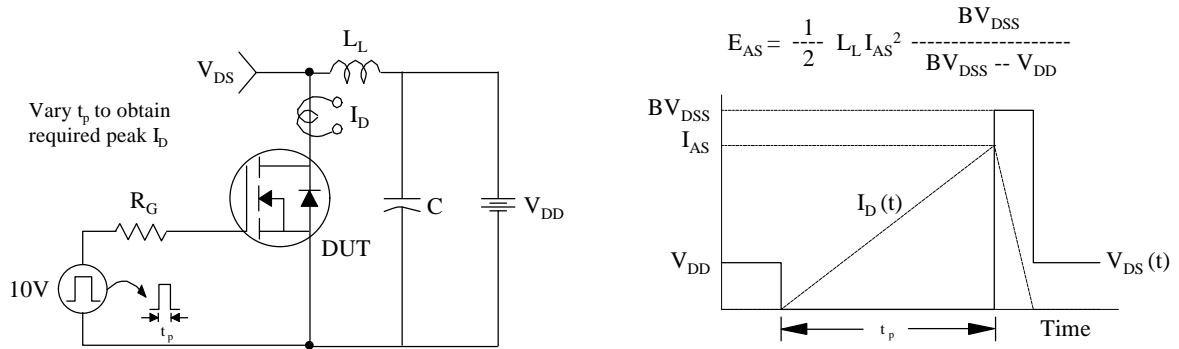


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

