

IRFIZ46NPbF

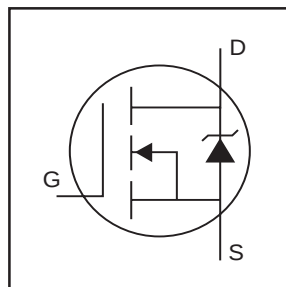
HEXFET® Power MOSFET

- Advanced Process Technology
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated
- Lead-Free

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

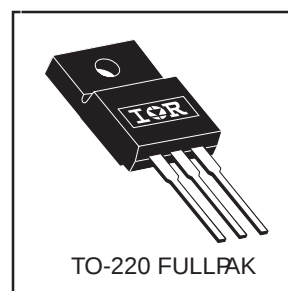
The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



$$V_{DS} = 55V$$

$$R_{DS(on)} = 0.020\Omega$$

$$I_D = 33A$$



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	33	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ 10V	23	
I_{DM}	Pulsed Drain Current ① ⑥	180	
P_D @ $T_C = 25^\circ C$	Power Dissipation	45	W
	Linear Derating Factor	0.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ② ⑥	230	mJ
I_{AR}	Avalanche Current ① ⑥	16	A
E_{AR}	Repetitive Avalanche Energy ① ⑥	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③ ⑥	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

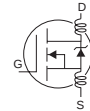
	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.017	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.020	Ω	$V_{GS} = 10V, I_D = 19A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	16	—	—	S	$V_{DS} = 25V, I_D = 28A$ ⑥
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	61	nC	$I_D = 28A$
Q_{gs}	Gate-to-Source Charge	—	—	13		$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	24		$V_{GS} = 10V$, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD} = 28V$
t_r	Rise Time	—	80	—		$I_D = 28A$
$t_{d(off)}$	Turn-Off Delay Time	—	43	—		$R_G = 12\Omega$
t_f	Fall Time	—	52	—		$R_D = 0.98\Omega$, See Fig. 10 ④⑥
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1500	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	450	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	160	—		$f = 1.0MHz$, See Fig. 5⑥
C	Drain to Sink Capacitance	—	12	—		$f = 1.0MHz$



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	33	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	180		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 19A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	72	110	ns	$T_J = 25^\circ\text{C}, I_F = 28A$
Q_{rr}	Reverse Recovery Charge	—	210	310	nC	$di/dt = 100A/\mu s$ ④⑥

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

③ $I_{SD} \leq 28A, di/dt \leq 240A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$

⑤ $t=60s, f=60Hz$

② $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}, L = 410\mu H$
 $R_G = 25\Omega, I_{AS} = 28A$. (See Figure 12)

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑥ Uses IRFZ46N data and test conditions

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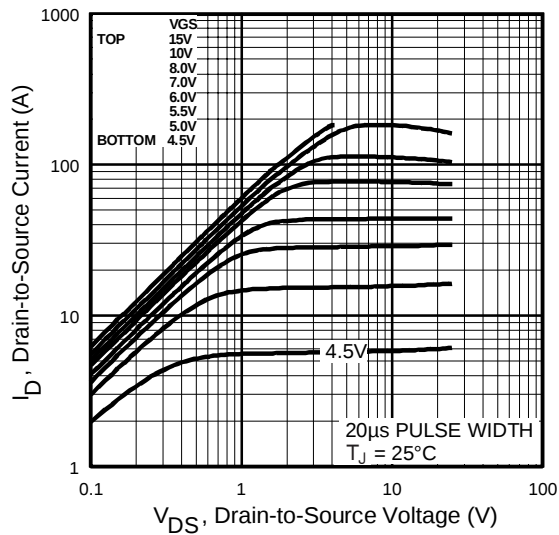


Fig 1. Typical Output Characteristics

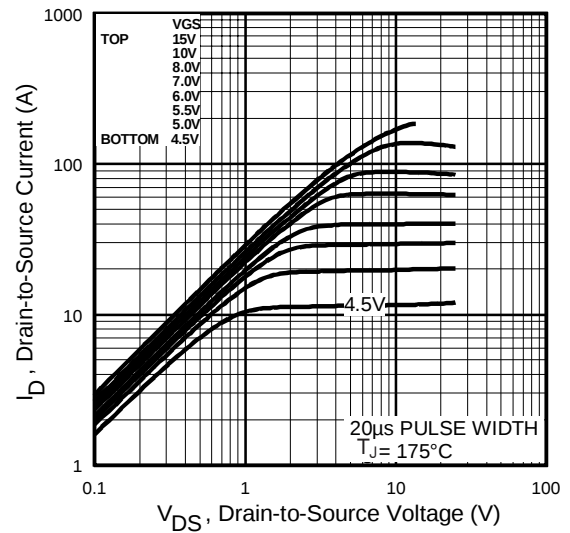


Fig 2. Typical Output Characteristics

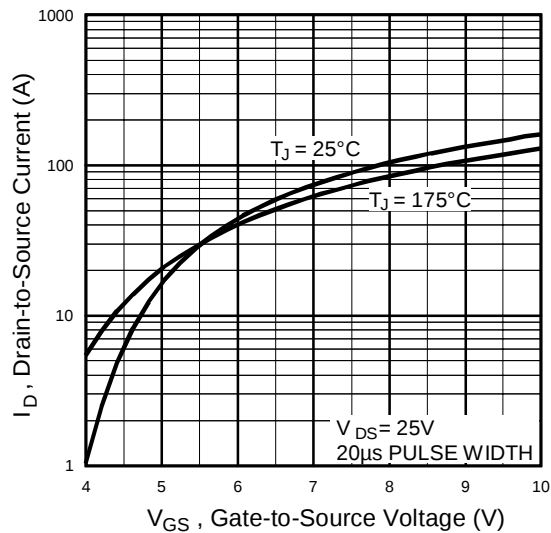


Fig 3. Typical Transfer Characteristics

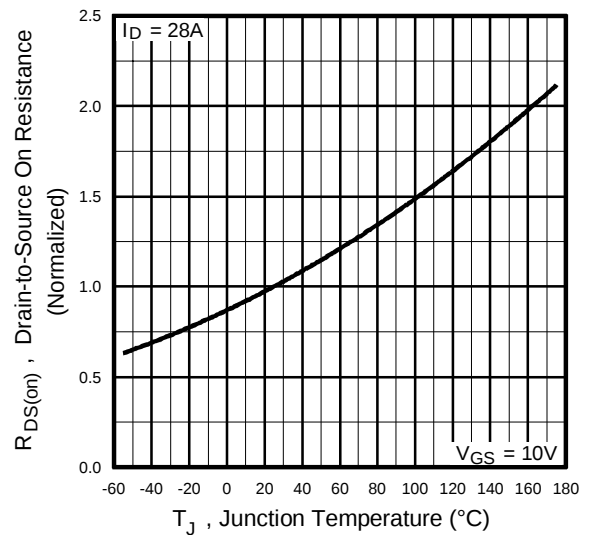


Fig 4. Normalized On-Resistance
Vs. Temperature

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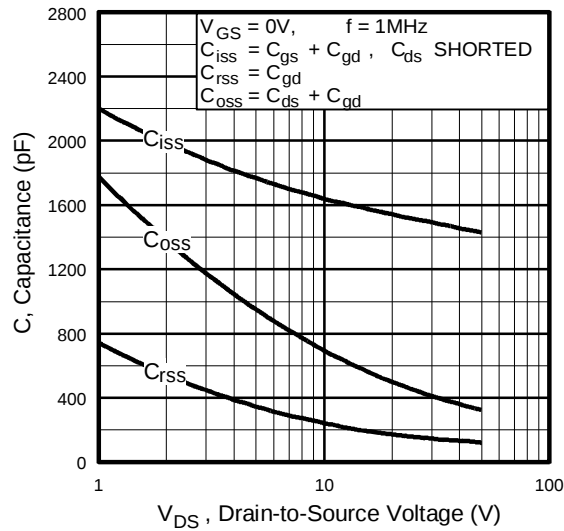


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

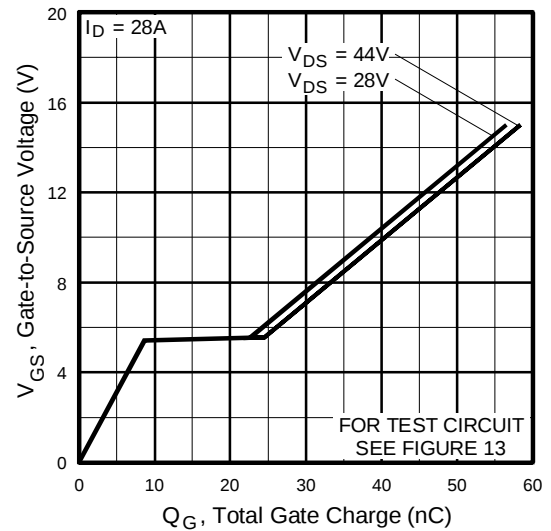


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

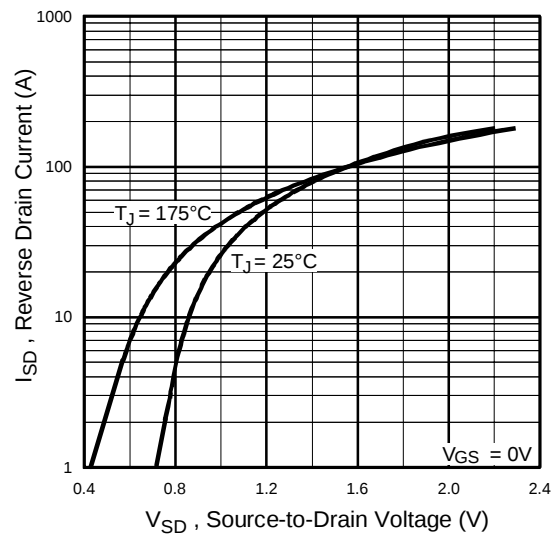


Fig 7. Typical Source-Drain Diode Forward Voltage

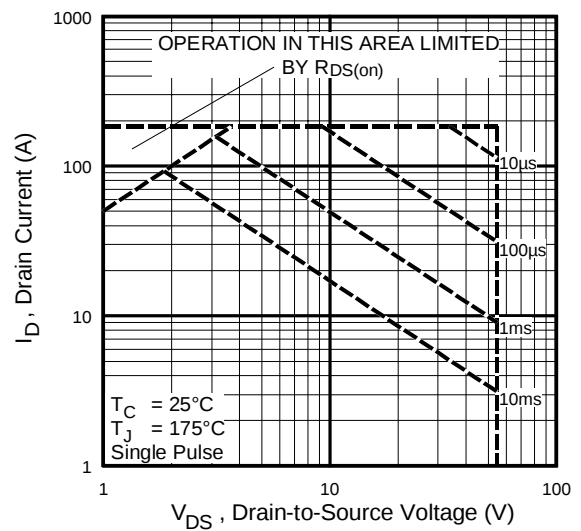


Fig 8. Maximum Safe Operating Area

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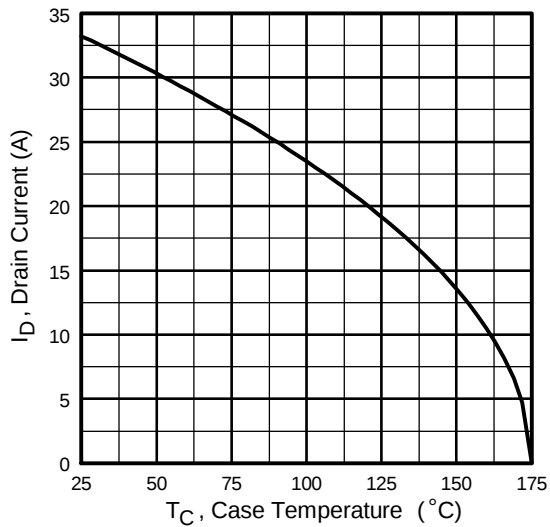


Fig 9. Maximum Drain Current Vs. Case Temperature

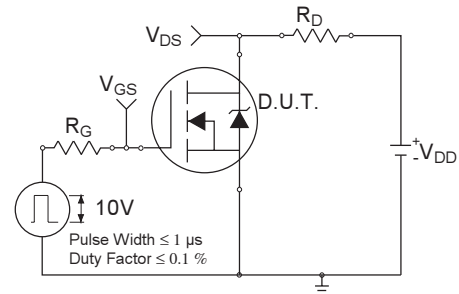


Fig 10a. Switching Time Test Circuit

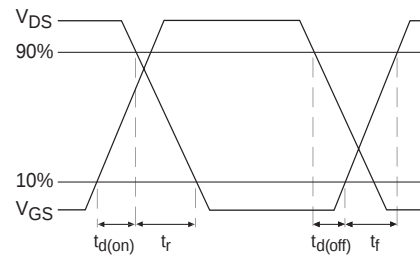


Fig 10b. Switching Time Waveforms

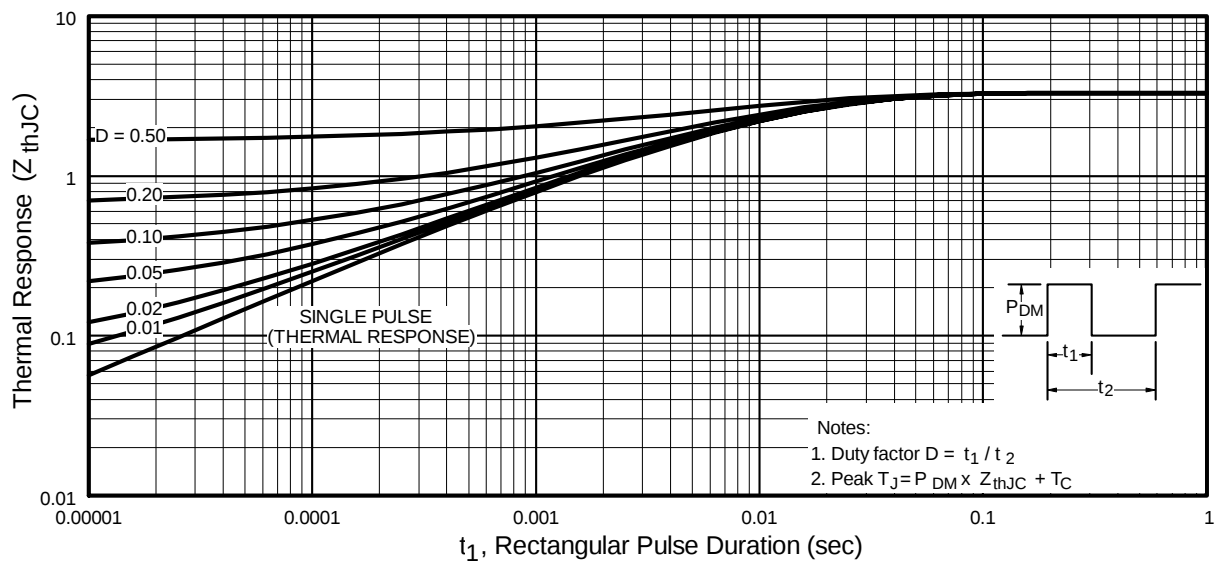


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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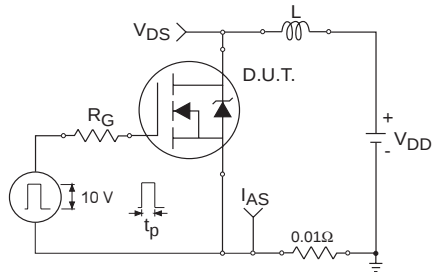


Fig 12a. Unclamped Inductive Test Circuit

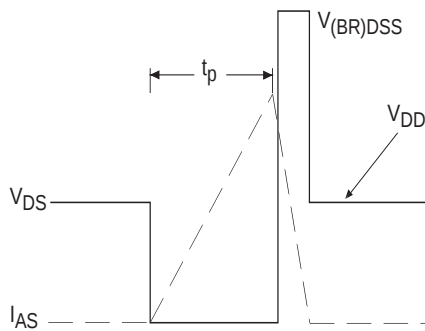


Fig 12b. Unclamped Inductive Waveforms

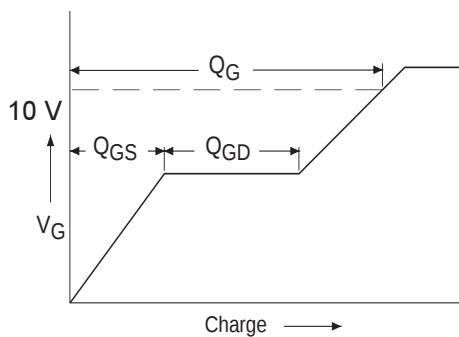


Fig 13a. Basic Gate Charge Waveform

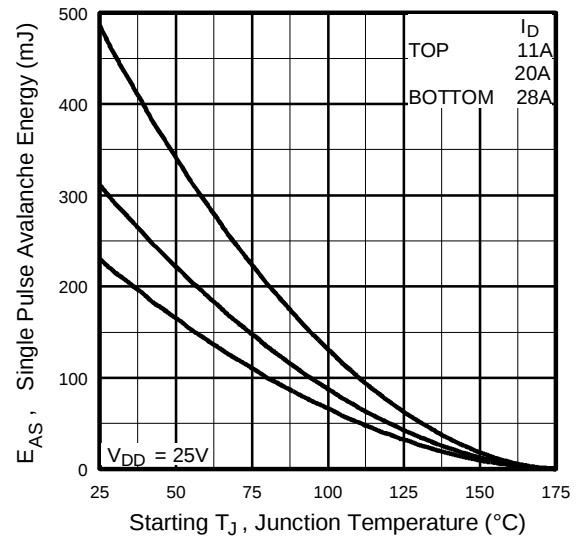


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

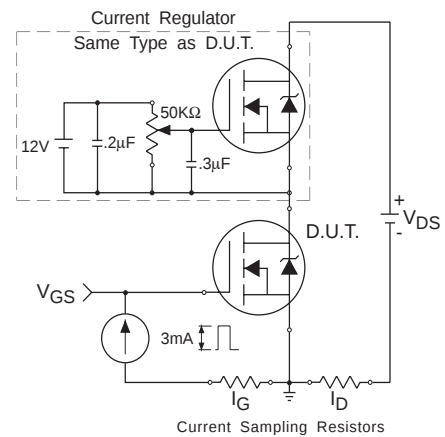
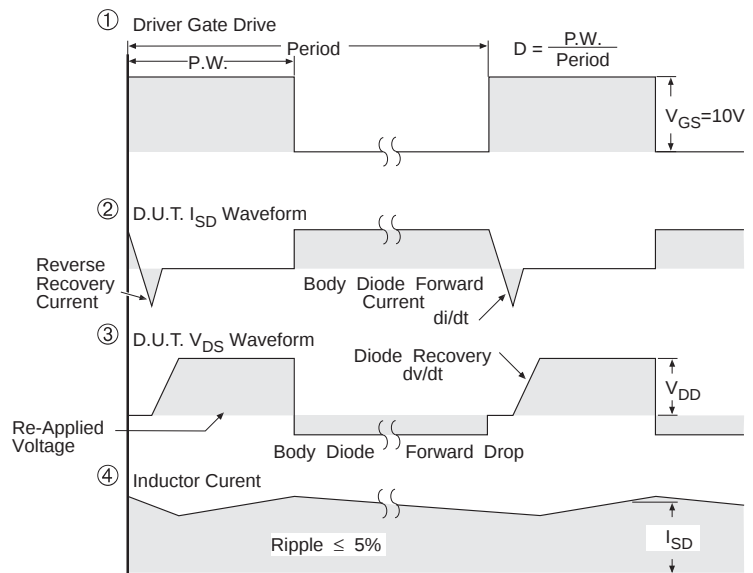
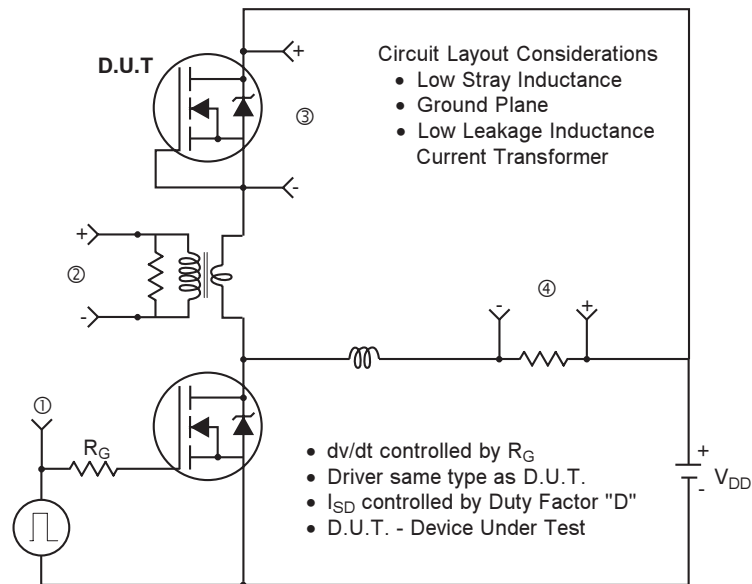


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

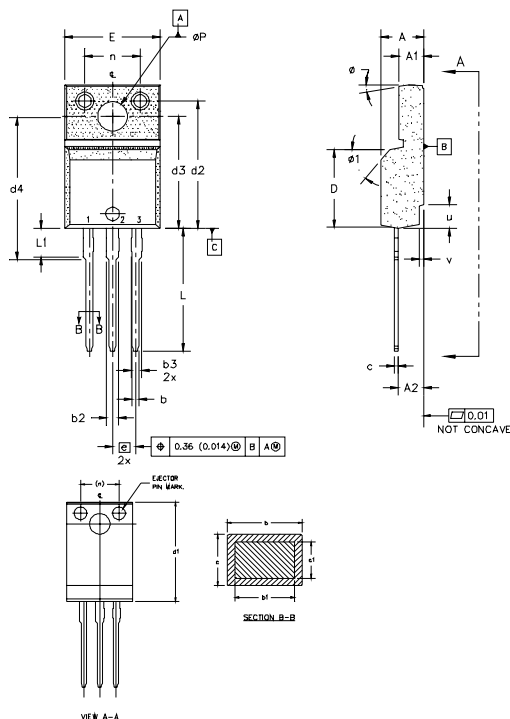
Fig 14. For N-Channel HEXFETS

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TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



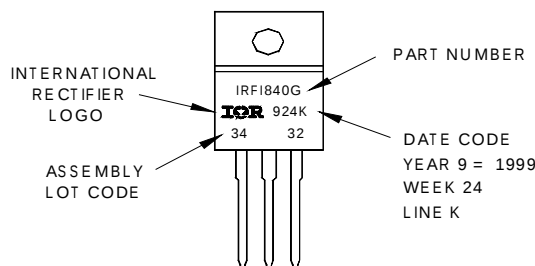
- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
 - 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 - 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
 - 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 5.0 DIMENSION b1 APPLY TO BASE METAL ONLY.
 - 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
 - 7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES	LEAD ASSIGNMENTS
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.57	4.83	0.180	0.190	5	HEXFET 1- GATE 2- DRAIN 3- SOURCE
A1	2.57	2.83	0.101	0.114		
A2	2.51	2.85	0.099	0.112		
b	0.622	0.89	0.024	0.035		
b1	0.622	0.838	0.024	0.033		
b2	1.229	1.400	0.048	0.055	4	IGBTs, CoPACK 1- GATE 2- COLLECTOR 3- EMITTER
b3	1.229	1.400	0.048	0.055		
c	0.440	0.629	0.017	0.025		
c1	0.440	0.584	0.017	0.023		
D	8.65	9.80	0.341	0.386		
d1	16.80	16.12	0.622	0.635	4	
d2	13.97	14.22	0.550	0.560		
d3	12.30	12.92	0.484	0.509		
d4	8.64	9.91	0.340	0.390		
E	10.36	10.63	0.408	0.419		
e	2.54 BSC		0.100 BSC		3	
L	13.20	13.73	0.520	0.541		
L1	3.10	3.50	0.122	0.138		
n	6.05	6.15	0.238	0.242		
φP	3.05	3.45	0.120	0.136		
u	2.40	2.50	0.094	0.098	6	
v	0.40	0.50	0.016	0.020	6	
w	3"	7"	3"	7"	6	
φ1		45°		45°		

TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRF1840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line
position indicates "Lead-Free"



Data and specifications subject to change without notice.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

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