

## 1. Description

This Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating.

## 2.2 Features

- Advanced Process Technology
- Ultra Low On-Resistance

## 2.1 Features

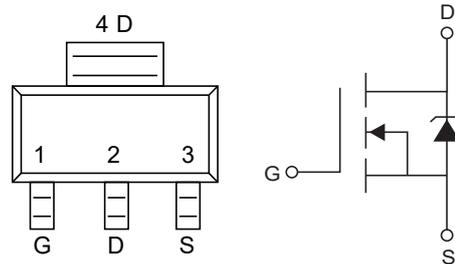
- $V_{DS(V)}=55V$
- $I_D=5.1A(V_{GS}=10V)$
- $R_{DS(ON)}\leq 57.5m\Omega(V_{GS}=10V)$

- 150°C Operating Temperature
- Fast Switching

## 3. Pinning information

Pin	Symbol	Description
1	G	GATE
2,4	D	DRAIN
3	S	SOURCE

SOT-223  
top view



## 4. Absolute Maximum Ratings

Parameter		Symbol	Max.	Units
Continuous Drain Current, $V_{GS}$ @ 10V(Silicon Limited) ⑦	$T_A=25^\circ C$	$I_D$	5.1	A
Continuous Drain Current, $V_{GS}$ @ 10V ⑦	$T_A=70^\circ C$		4.1	A
Pulsed Drain Current ①		$I_{DM}$	41	A
Power Dissipation ⑦	$T_A=25^\circ C$	$P_D$	2.8	
Power Dissipation ⑧	$T_A=25^\circ C$		1	W
Linear Derating Factor ⑦			0.02	W/°C
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V
Single Pulse Avalanche Energy ②		$E_{AS}$ (Thermally limited)	13	mJ
Single Pulse Avalanche Energy Tested Value ⑥		$E_{AS}$ (Tested)	32	mJ



Avalanche Current ①	$I_{AR}$	See Fig.16a, 16b, 13, 15	A
Repetitive Avalanche Energy ⑤	$E_{AR}$		mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	°C

## 5. Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Junction-to-Ambient (PCB mount, steady state) ⑦	$R_{thJA}$		45	°C/W
Junction-to-Ambient (PCB Mount, steady state) ⑧	$R_{thJA}$		120	°C/W



## 6. Electrical Characteristic (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	55			V
Breakdown Voltage Temp. Coefficient	ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Reference to 25°C, I <sub>D</sub> =1mA		0.053		V/°C
Static Drain-to-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =3.1A ③		46.2	57.5	mΩ
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2		4	V
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =25V, I <sub>D</sub> =3.1A	6.2			S
Drain-to-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =55V, V <sub>GS</sub> =0V			20	μA
		V <sub>DS</sub> =55V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C			250	μA
Gate-to-Source Forward Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =20V			200	nA
Gate-to-Source Reverse Leakage		V <sub>GS</sub> =-20V			-200	nA
Total Gate Charge	Q <sub>g</sub>	I <sub>D</sub> =3.1A, V <sub>DS</sub> =44V, V <sub>GS</sub> =10V ③		9.1	14	nC
Gate-to-Source Charge	Q <sub>gs</sub>		1.9		nC	
Gate-to-Drain ("Miller") Charge	Q <sub>gd</sub>		3.9		nC	
Turn-On Delay Time	t <sub>D(on)</sub>	V <sub>DD</sub> =28V, I <sub>D</sub> =3.1A R <sub>G</sub> =53Ω, V <sub>GS</sub> =10V ③		7.8		ns
Rise Time	t <sub>r</sub>		21		ns	
Turn-Off Delay Time	t <sub>D(off)</sub>		30		ns	
Fall Time	t <sub>f</sub>		23		ns	
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz		340		pF
Output Capacitance	C <sub>oss</sub>		68		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		39		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =1V, f=1MHz		210		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =44V, f=1MHz		55		pF
Effective Output Capacitance	C <sub>oss,eff.</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V to 44V ④		93		pF



Diode Characteristics						
Continuous Source Current (Body Diode)	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode.			5.1	A
Pulsed Source Current (Body Diode) ①	$I_{SM}$				41	A
Diode Forward Voltage	$V_{SD}$	$T_J=25^\circ\text{C}, I_S=3.1\text{A}, V_{GS}=0\text{V}$ ③			1.3	V
Reverse Recovery Time	$t_{rr}$	$T_J=25^\circ\text{C}, I_F=3.1\text{A}, V_{DD}=28\text{V}$		15	23	ns
Reverse Recovery Charge	$Q_{rr}$	$di/dt=100\text{A}/\mu\text{s}$ ③		9.8	15	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

## Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature(See fig. 14).
- ② Limited by  $T_{Jmax}$ , starting  $T_J=25^\circ\text{C}$ ,  $L=2.8\text{mH}$ ,  $R_G=25\Omega$ ,  $I_{AS}=3.1\text{A}$ ,  $V_{GS}=10\text{V}$ . Part not recommended for use above this value.
- ③ Pulse width  $\leq 1\text{ms}$ ; duty cycle  $\leq 2\%$ .
- ④  $C_{oss}$  eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑤ Limited by  $T_{Jmax}$ , see Fig.16a, 16b, 13, 15 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ When mounted on 1 inch square copper board.
- ⑧ When mounted on FR-4 board using minimum recommended footprint.



## 7.1 Typical Characteristics

<p>Figure 1: Typical On-Resistance vs. Gate Voltage</p>	<p>Figure 2: Typical Output Characteristics</p>
<p>Figure 3: Typical Output Characteristics</p>	<p>Figure 4: Typical Forward Transconductance Vs. Drain Current</p>
<p>Figure 5: Typical Capacitance vs. Drain-to-Source Voltage</p>	<p>Figure 6: Typical Gate Charge Vs. Gate-to-Source Voltage</p>



## 7.2 Typical Characteristics

<p><math>I_{SD}</math>, Reverse Drain Current (A)</p> <p><math>V_{SD}</math>, Source-to-Drain Voltage (V)</p> <p><math>T_J = 150^\circ\text{C}</math></p> <p><math>T_J = 25^\circ\text{C}</math></p> <p><math>V_{GS} = 0\text{V}</math></p>	<p><math>I_D</math>, Drain-to-Source Current (A)</p> <p><math>V_{DS}</math>, Drain-to-Source Voltage (V)</p> <p>OPERATION IN THIS AREA LIMITED BY <math>R_{DS(on)}</math></p> <p><math>T_A = 25^\circ\text{C}</math></p> <p><math>T_J = 150^\circ\text{C}</math></p> <p>Single Pulse</p> <p>100µsec</p> <p>1msec</p> <p>10msec</p>
<p>Figure 7: Typical Capacitance vs. Drain-to-Source Voltage</p>	<p>Figure 8: Maximum Safe Operating Area</p>
<p><math>I_D</math>, Drain Current (A)</p> <p><math>T_A</math>, Ambient Temperature (<math>^\circ\text{C}</math>)</p>	<p><math>R_{DS(on)}</math>, Drain to Source On-Resistance (Normalized)</p> <p><math>T_J</math>, Junction Temperature (<math>^\circ\text{C}</math>)</p> <p><math>I_D = 3.1\text{A}</math></p> <p><math>V_{GS} = 10\text{V}</math></p>
<p>Figure 9: Maximum Drain Current Vs. Ambient Temperature</p>	<p>Figure 10: Normalized On-Resistance Vs. Temperature</p>
<p><math>E_{AS}</math>, Single Pulse Avalanche Energy (mJ)</p> <p>Starting <math>T_J</math>, Junction Temperature (<math>^\circ\text{C}</math>)</p> <p><math>I_D</math></p> <p>TOP 0.77A</p> <p>0.89A</p> <p>BOTTOM 3.1A</p>	<p><math>V_{GS(th)}</math>, Gate threshold Voltage (V)</p> <p><math>T_J</math>, Temperature (<math>^\circ\text{C}</math>)</p> <p><math>I_D = 250\mu\text{A}</math></p>
<p>Figure 11: Typical On-Resistance vs. Drain Current</p>	<p>Figure 12: Threshold Voltage Vs. Temperature</p>



## 7.3 Typical Characteristics

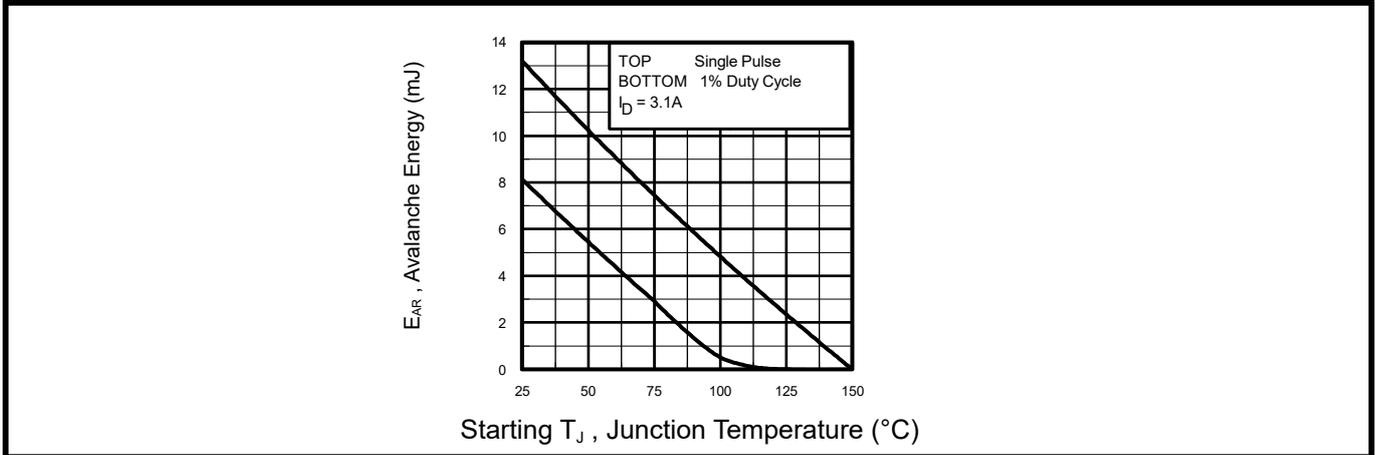


Figure 13: Maximum Avalanche Energy vs. Temperature

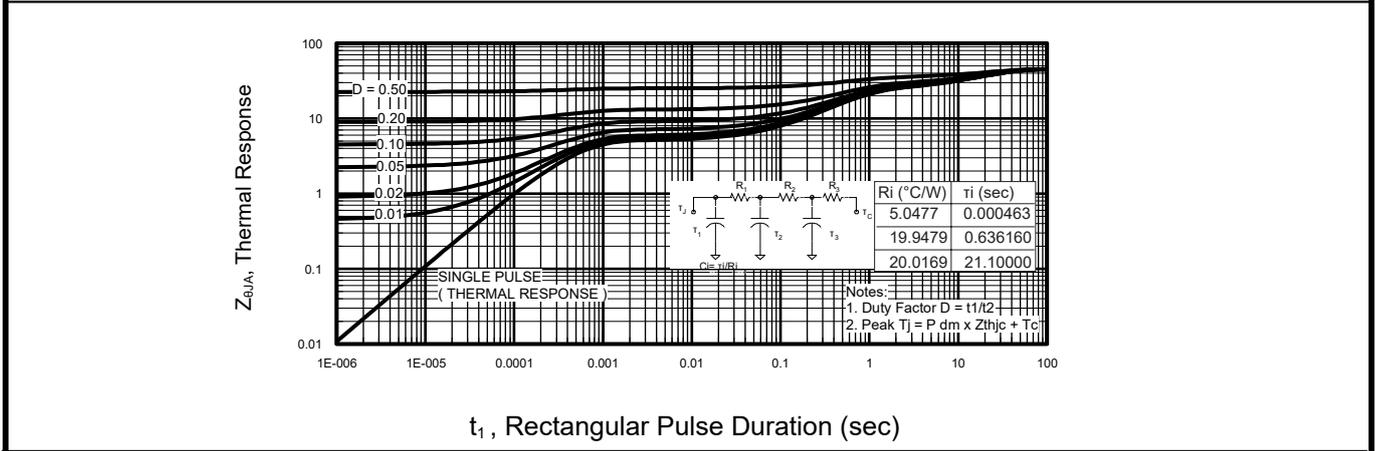


Figure 14: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

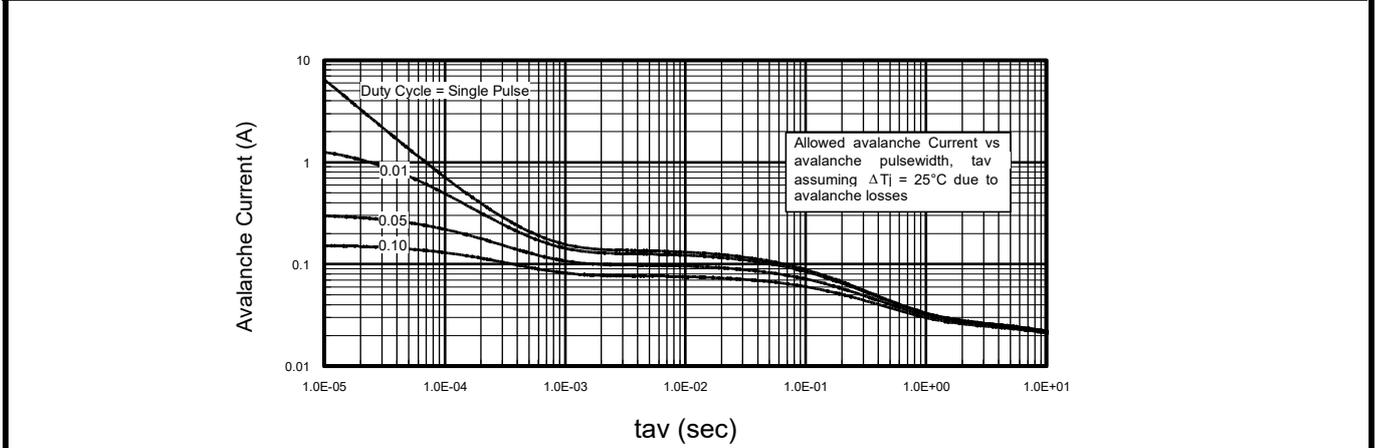


Figure 15: Typical Avalanche Current vs. Pulse width



## 7.4 Typical Characteristics

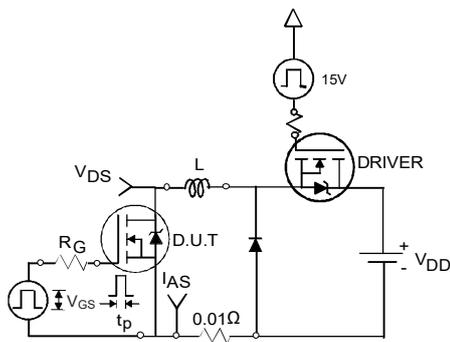


Figure 16a: Unclamped Inductive Test Circuit

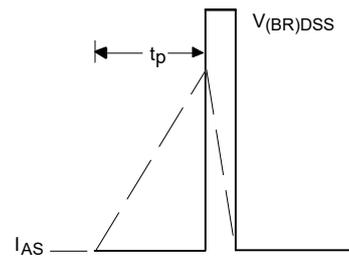


Figure 16b: Unclamped Inductive Waveforms

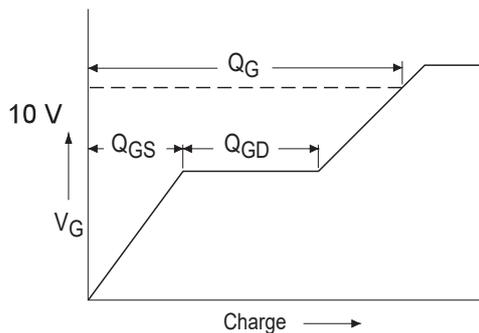


Figure 17a: Gate Charge Test Circuit

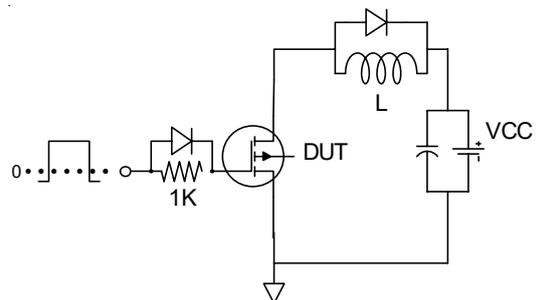
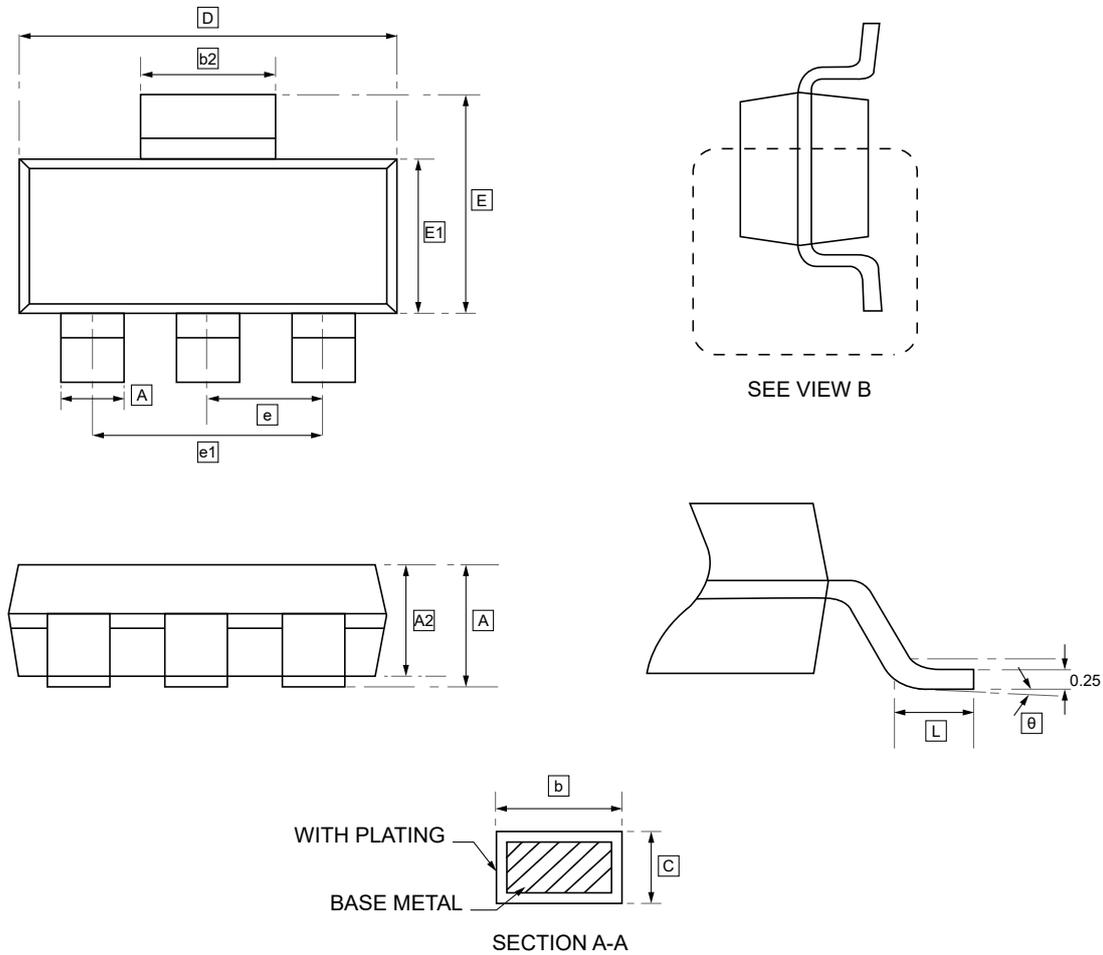


Figure 17b: Threshold Voltage Vs. Temperature



## 8.SOT-223 Package Outlie Dimensions

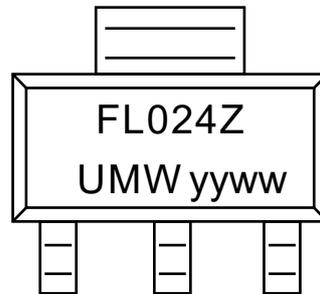


### DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	b2	c	D	E	E1	e	e1	L	θ
Min		0.02	1.55	0.66	2.90	0.23	6.30	6.70	3.30	2.30	4.60	0.90	0°
Max	1.80	0.10	1.65	0.84	3.10	0.33	6.70	7.30	3.70	BSC	BSC		8°



## 9. Ordering information



yy: Year Code  
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRFL024ZTR	SOT-223	2500	Tape and reel



## 10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.