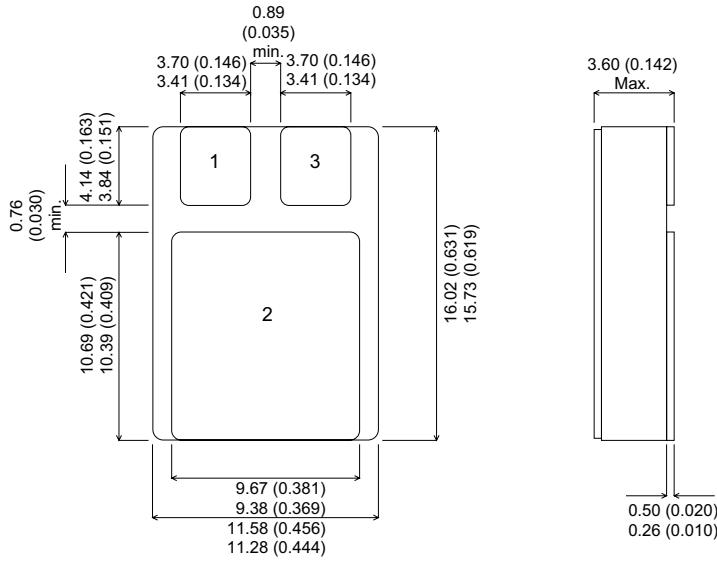


MECHANICAL DATA



SMD1

Pad 1 – Source

Pad 2 – Drain

Pad 3 – Gate

N-CHANNEL
POWER MOSFET V_{DSS} 60V $I_{D(cont)}$ 34A $R_{DS(on)}$ 0.040 Ω

FEATURES

- HERMETICALLY SEALED SURFACE MOUNT PACKAGE
- SMALL FOOTPRINT – EFFICIENT USE OF PCB SPACE.
- SIMPLE DRIVE REQUIREMENTS
- LIGHTWEIGHT
- HIGH PACKING DENSITIES

Note: IRFxxxSM also available with pins 1 and 3 reversed.

ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$ unless otherwise stated)

V_{GS}	Gate – Source Voltage	$\pm 20V$
I_D	Continuous Drain Current ($V_{GS} = 0$, $T_{case} = 25^{\circ}C$)	34A
I_D	Continuous Drain Current ($V_{GS} = 0$, $T_{case} = 100^{\circ}C$)	21A
I_{DM}	Pulsed Drain Current ¹	136A
P_D	Power Dissipation @ $T_{case} = 25^{\circ}C$	75W
	Linear Derating Factor	0.6W/ $^{\circ}C$
E_{AS}	Single Pulse Avalanche Energy ²	340mJ
dv/dt	Peak Diode Recovery ³	4.5V/ns
T_J, T_{stg}	Operating and Storage Temperature Range	-55 to $150^{\circ}C$
T_L	Package Mounting Surface Temperature (for 5 sec)	$300^{\circ}C$
$R_{\theta JC}$	Thermal Resistance Junction to Case	1.67 $^{\circ}C/W$
$R_{\theta J-PCB}$	Thermal Resistance Junction to PCB (Typical)	4 $^{\circ}C/W$

Notes

1) Pulse Test: Pulse Width $\leq 300ms$, $\delta \leq 2\%$

2) @ $V_{DD} = 25V$, $L \geq 0.3mH$, $R_G = 25\Omega$, Peak $I_L = 34A$, Starting $T_J = 25^{\circ}C$

3) @ $I_{SD} \leq 34A$, $di/dt \leq 100A/\mu s$, $V_{DD} \leq BV_{DSS}$, $T_J \leq 150^{\circ}C$, SUGGESTED $R_G = 9.1\Omega$

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ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
STATIC ELECTRICAL RATINGS					
BV_{DSS} Drain – Source Breakdown Voltage	$V_{GS} = 0$ $I_D = 1\text{mA}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$ Temperature Coefficient of Breakdown Voltage	Reference to 25°C $I_D = 1\text{mA}$		0.68		$\text{V}/^{\circ}\text{C}$
$R_{DS(on)}$ Static Drain – Source On–State Resistance ¹	$V_{GS} = 10\text{V}$ $I_D = 21\text{A}$			0.040	Ω
	$V_{GS} = 10\text{V}$ $I_D = 34\text{A}$			0.050	
$V_{GS(th)}$ Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\mu\text{A}$	2		4	V
g_{fs} Forward Transconductance ¹	$V_{DS} \geq 15\text{V}$ $I_{DS} = 21\text{A}$	17			$\text{S}(\bar{v})$
I_{DSS} Zero Gate Voltage Drain Current	$V_{GS} = 0$ $V_{DS} = 0.8BV_{DSS}$ $T_J = 125^{\circ}\text{C}$			25	μA
				250	
I_{GSS} Forward Gate – Source Leakage	$V_{GS} = 20\text{V}$			100	nA
I_{GSS} Reverse Gate – Source Leakage	$V_{GS} = -20\text{V}$			-100	
DYNAMIC CHARACTERISTICS					
C_{iss} Input Capacitance	$V_{GS} = 0$		2400		pF
C_{oss} Output Capacitance	$V_{DS} = 25\text{V}$		1100		
C_{rss} Reverse Transfer Capacitance	$f = 1\text{MHz}$		230		
Q_g Total Gate Charge ¹	$V_{GS} = 10\text{V}$ $I_D = 34\text{A}$ $V_{DS} = 0.5BV_{DSS}$	39		88	nC
Q_{gs} Gate – Source Charge ¹	$I_D = 34\text{A}$	6.7		15	nC
Q_{gd} Gate – Drain (“Miller”) Charge ¹	$V_{DS} = 0.5BV_{DSS}$	18		52	
$t_{d(on)}$ Turn–On Delay Time	$V_{DD} = 30\text{V}$ $I_D = 34\text{A}$ $R_G = 9.1\Omega$			23	ns
t_r Rise Time				130	
$t_{d(off)}$ Turn–Off Delay Time				81	
t_f Fall Time				79	
SOURCE – DRAIN DIODE CHARACTERISTICS					
I_S Continuous Source Current				34	A
I_{SM} Pulse Source Current ²				136	
V_{SD} Diode Forward Voltage	$I_S = 34\text{A}$ $T_J = 25^{\circ}\text{C}$ $V_{GS} = 0$			2.5	V
t_{rr} Reverse Recovery Time	$I_F = 34\text{A}$ $T_J = 25^{\circ}\text{C}$			220	ns
Q_{rr} Reverse Recovery Charge	$d_i / d_t \leq 100\text{A}/\mu\text{s}$ $V_{DD} \leq 50\text{V}$			1.6	μC
t_{on} Forward Turn–On Time		Negligible			
PACKAGE CHARACTERISTICS					
L_D Internal Drain Inductance (from centre of drain pad to die)			0.8		nH
L_S Internal Source Inductance (from centre of source pad to end of source bond wire)			2.8		

Notes

- 1) Pulse Test: Pulse Width $\leq 300\text{ms}$, $\delta \leq 2\%$
- 2) Repetitive Rating – Pulse width limited by maximum junction temperature.