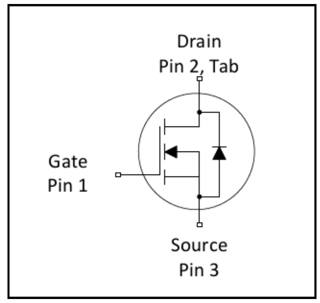
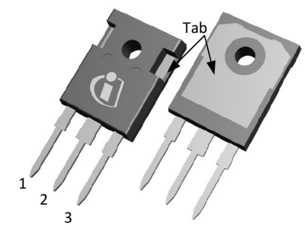
IRFP2907PbF

$V_{(BR)DSS}$	75V
$R_{DS(on)}$ max.	4.5mΩ
I_D	209A⑥





TO-247AC

Typical Applications
- Telecom applications requiring soft start

Features
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free

Description

This Stripe Planar design of HEXFET Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in a wide variety of applications

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP2907PbF	TO-247AC	Tube	25	IRFP2907PbF

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	209⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	148⑥	
I_{DM}	Pulsed Drain Current ①	840	
P_D @T_C = 25°C	Power Dissipation	470	W
	Linear Derating Factor	3.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	1970	mJ
I_{AR}	Avalanche Current	See Fig.12a, 12b, 15,16	A
E_{AR}	Repetitive Avalanche Energy ⑦		mJ
dv/dt	Peak Diode Recovery dv/dt③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

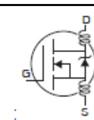
Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.32	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient	——	40	

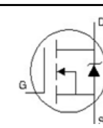
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.085	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	3.6	4.5	mΩ	V_{GS} = 10V, I_D = 125A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
gfs	Forward Trans conductance	130	——	——	S	V_{DS} = 25V, I_D = 125A
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 75V, V_{GS} = 0V
		——	——	250		V_{DS} = 60V,V_{GS} = 0V,T_J =150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	——	410	620	nC	I_D = 125A
Q_{gs}	Gate-to-Source Charge	——	92	140		V_{DS} = 60V
Q_{gd}	Gate-to-Drain Charge	——	140	210		V_{GS} = 10V ④
$t_{d(on)}$	Turn-On Delay Time	——	23	——	ns	V_{DD} = 38V
t_r	Rise Time	——	190	——		I_D = 125A
$t_{d(off)}$	Turn-Off Delay Time	——	130	——		R_G= 1.2Ω
t_f	Fall Time	——	130	——		V_{GS} = 10V ④
L_D	Internal Drain Inductance	——	5.0	——	nH	Between lead, 6mm (0.25in.)
L_S	Internal Source Inductance	——	13	——		from package and center of die contact 
C_{iss}	Input Capacitance	——	13000	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	2100	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	500	——		f = 1.0MHz, See Fig 5
C_{oss}	Output Capacitance	——	9780	——		V_{GS} = 0V, V_{DS} =1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	1360	——		V_{GS} = 0V, V_{DS} =60V, f = 1.0MHz
$C_{oss\ eff.}$	Effective Output Capacitance⑤	——	2320	——		V_{GS} = 0V, V_{DS} =0V to 60V

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	209⑥	A	MOSFET symbol showing the
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	840		integral reverse p-n junction diode. 
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C,I_S = 125A,V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	140	210	ns	T_J = 25°C ,I_F = 125A
Q_{rr}	Reverse Recovery Charge	——	880	1320	nC	di/dt = 100A/μs ④

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
② Starting T_J = 25°C, L = 0.25mH, R_G = 25Ω, I_{AS} = 125A.(See Fig. 12)
③ $I_{SD} \leq$ 125A, di/dt $\leq$ 260A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C.
④ Pulse width $\leq$ 400μs; duty cycle $\leq$ 2%.
⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 90A.
⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

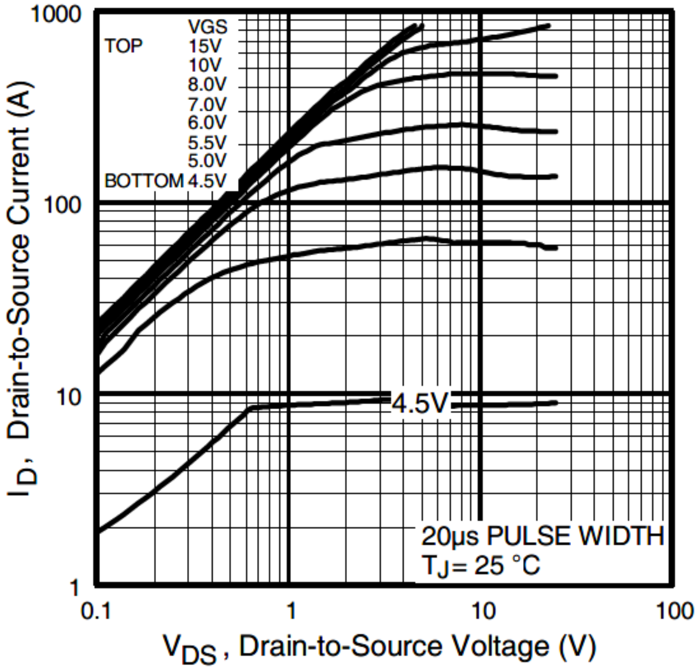


Fig. 1 Typical Output Characteristics

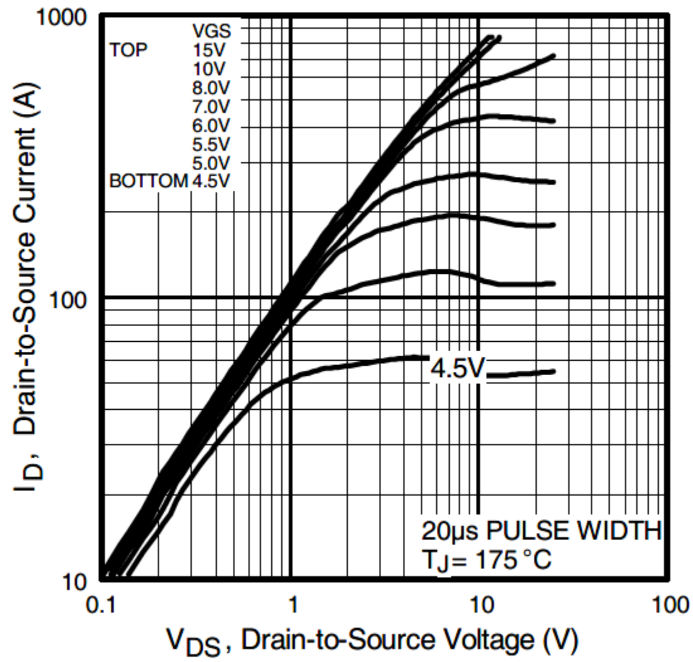


Fig. 2 Typical Output Characteristics

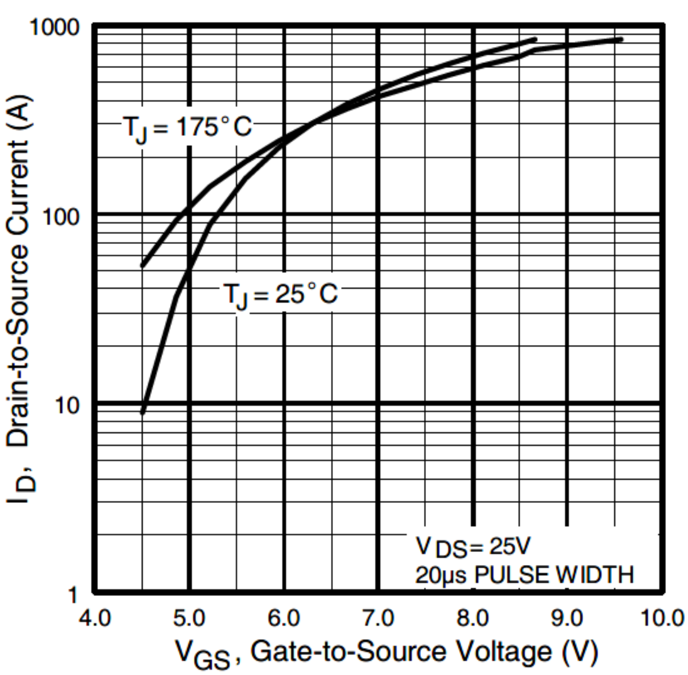


Fig. 3 Typical Transfer Characteristics

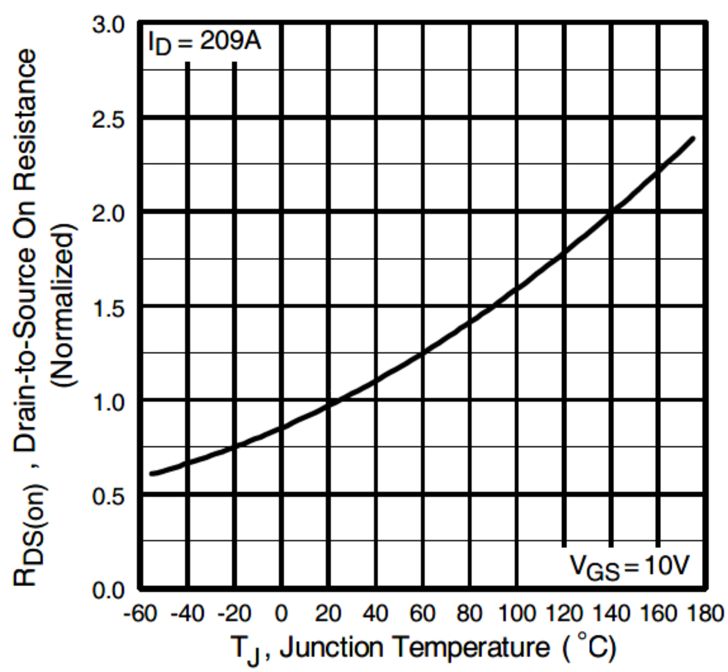


Fig. 4 Normalized On-Resistance vs. Temperature

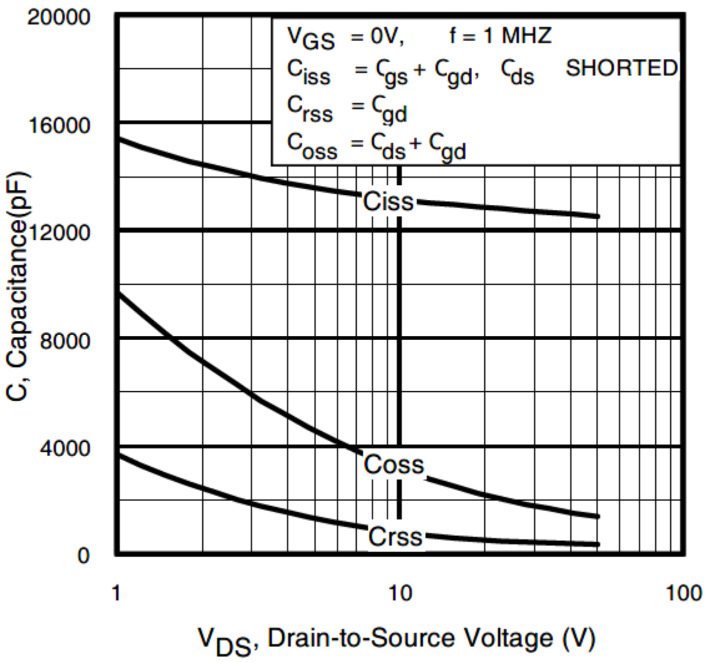


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

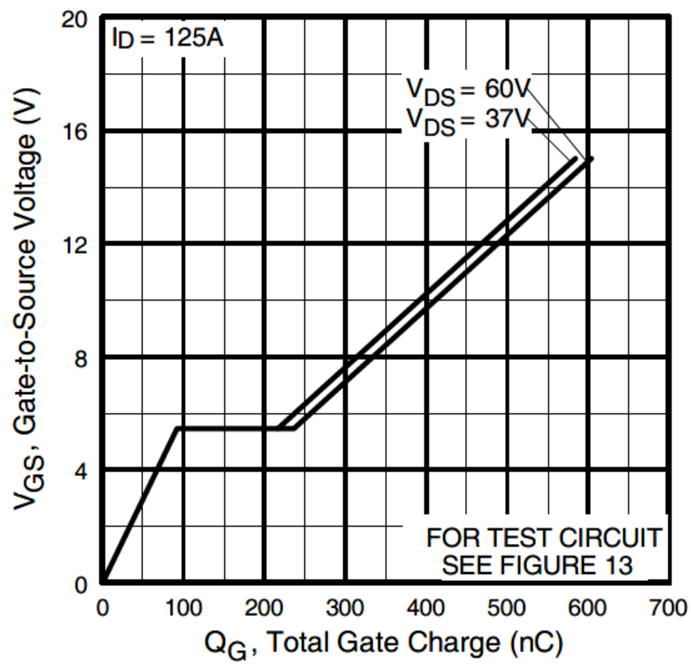


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

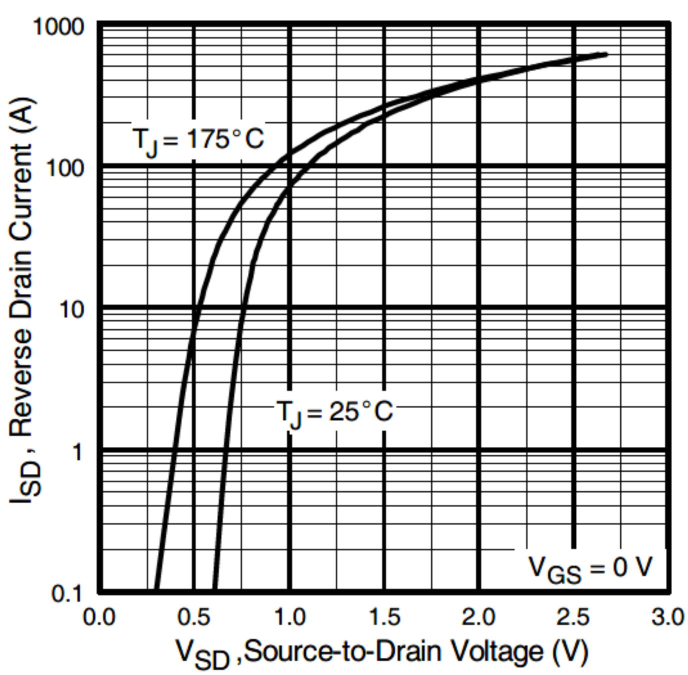


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

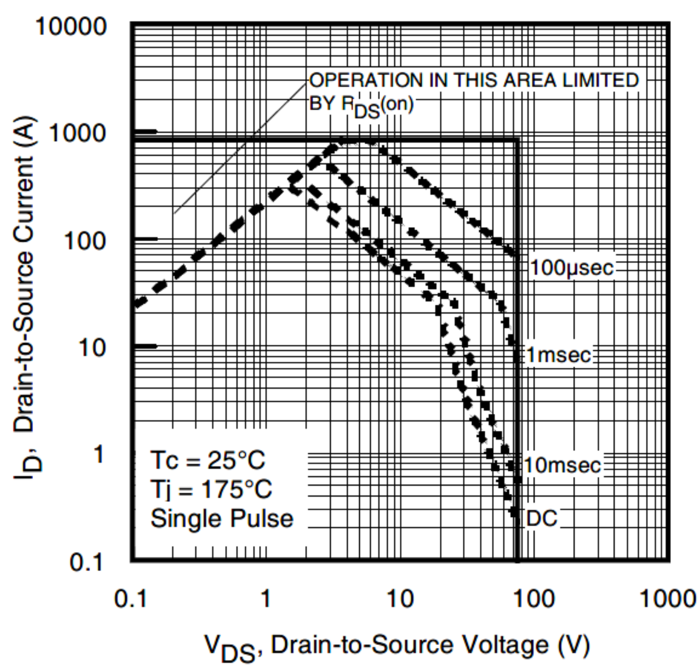


Fig 8. Maximum Safe Operating Area

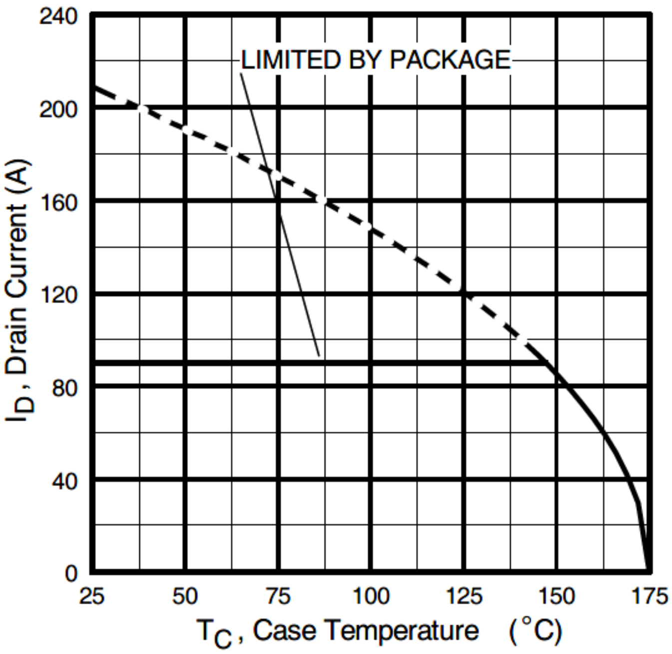


Fig 9. Maximum Drain Current vs. Case Temperature

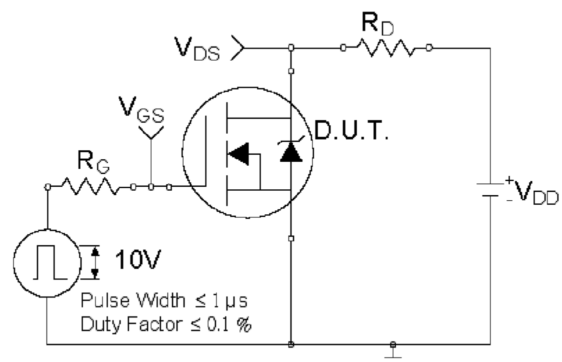


Fig 10a. Switching Time Test Circuit

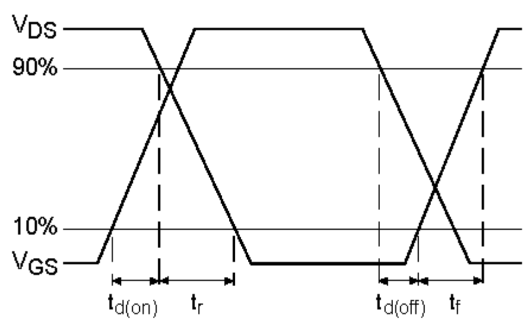


Fig 10a. Switching Time Waveforms

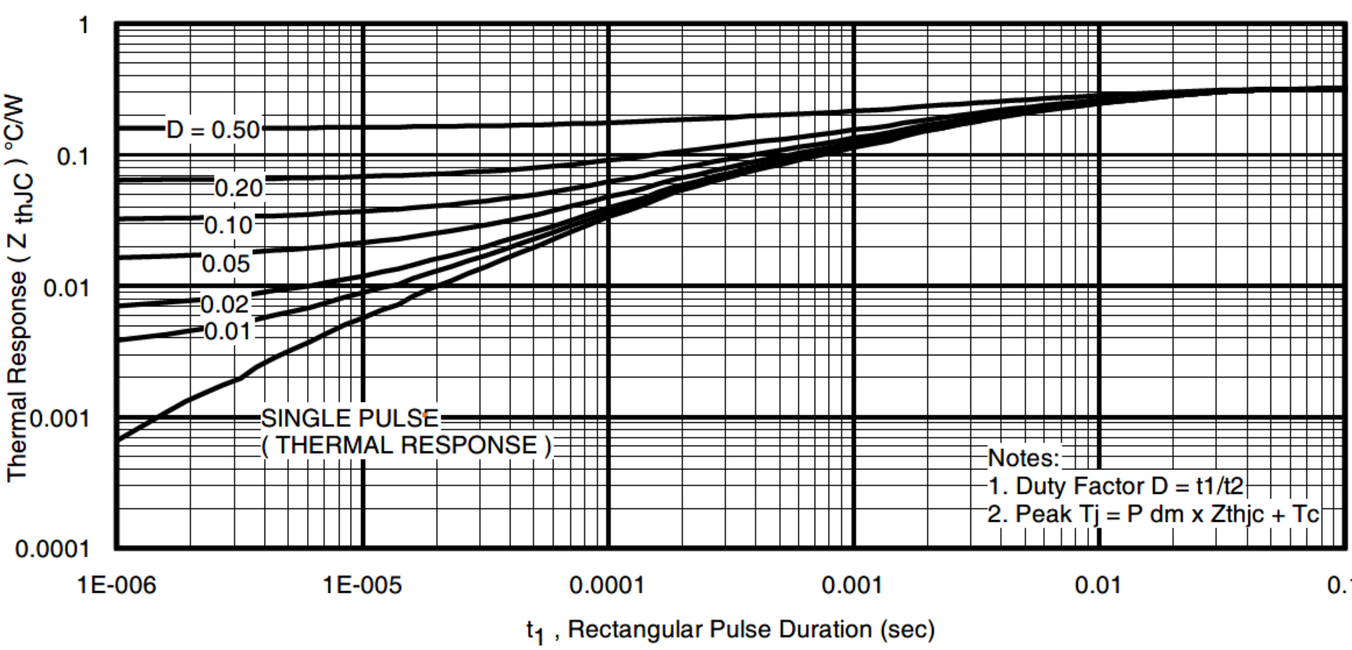


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

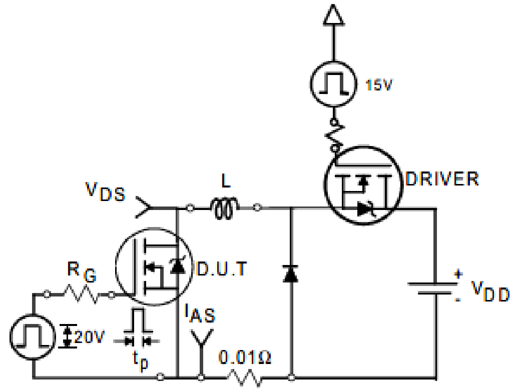


Fig. 12a. Unclamped Inductive Test Circuit

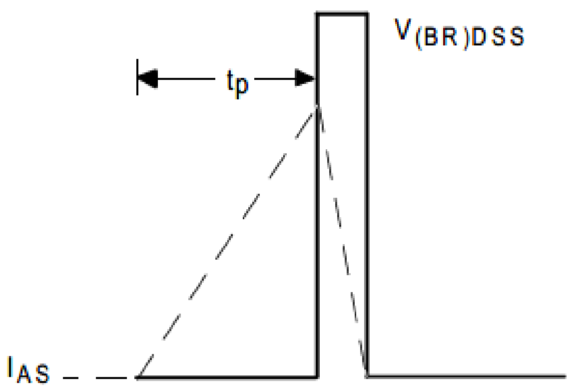


Fig. 12b. Unclamped Inductive Waveforms

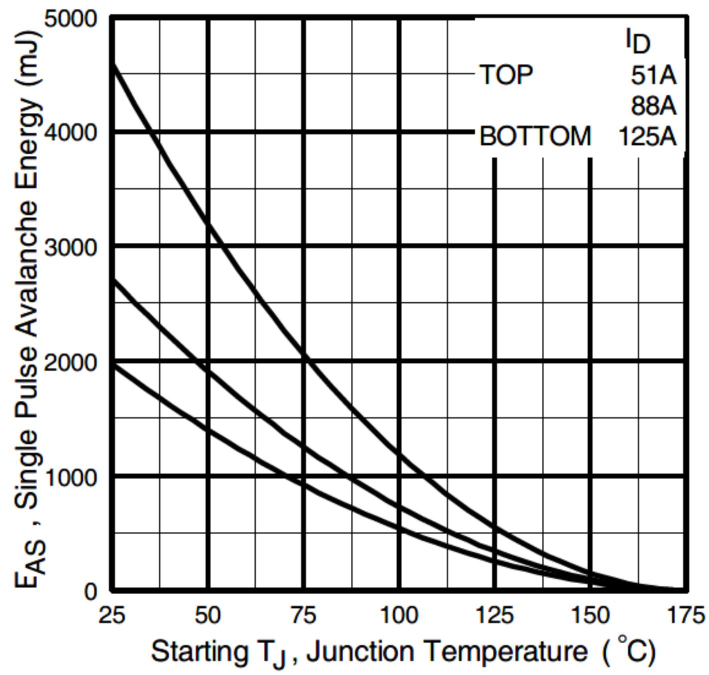


Fig 12c. Maximum Avalanche Energy vs. Drain Current

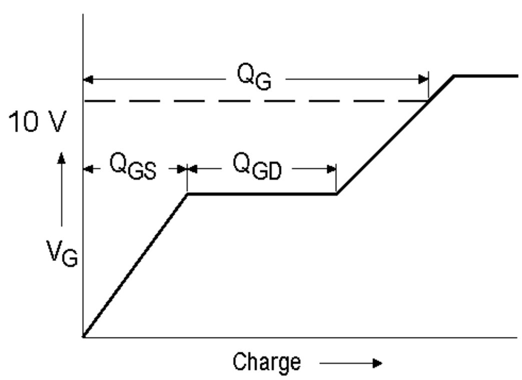


Fig 13a. Basic Gate Charge Waveform

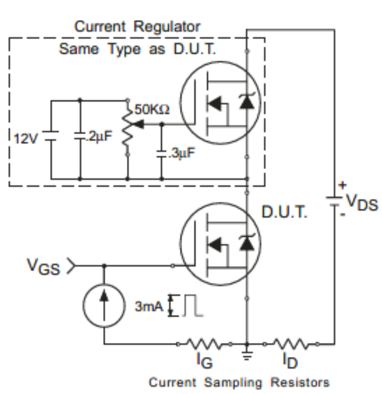


Fig 13b. Gate Charge Test Circuit

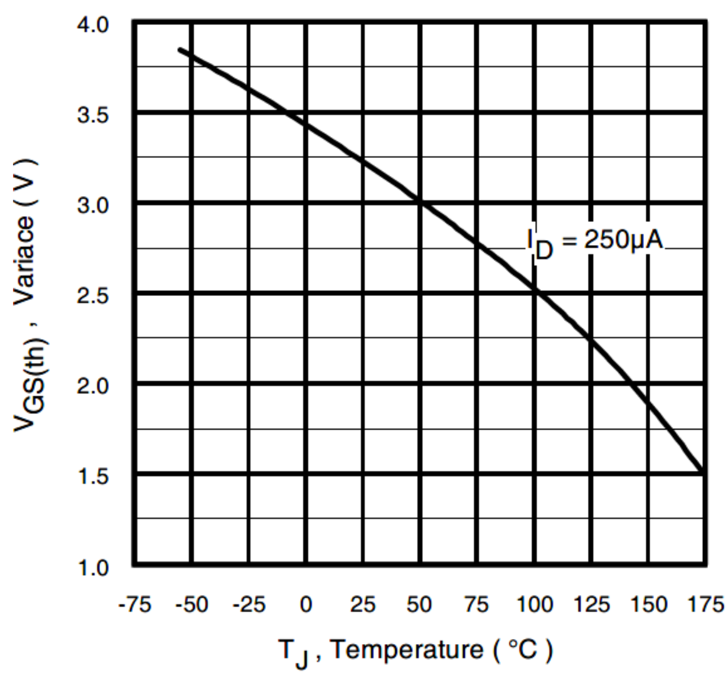


Fig 14 Threshold Voltage Vs. Temperature

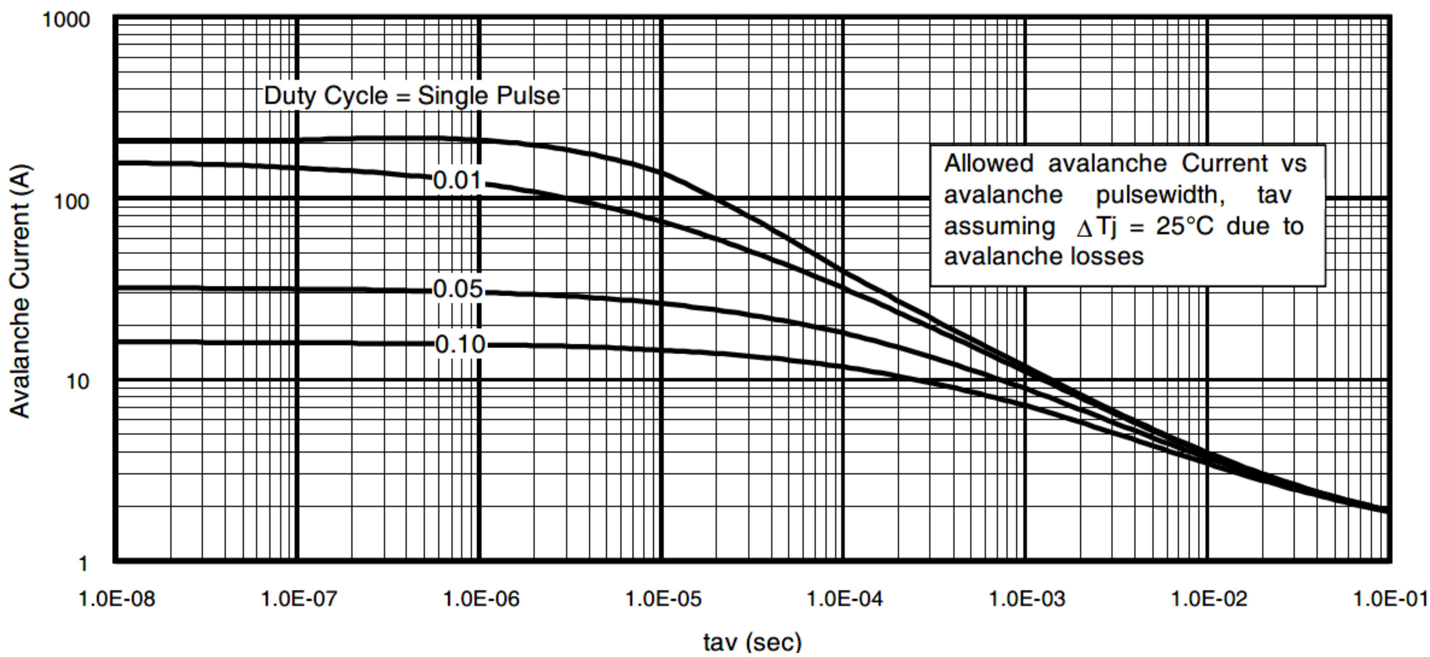


Fig 15. Typical Avalanche Current vs. Pulsewidth

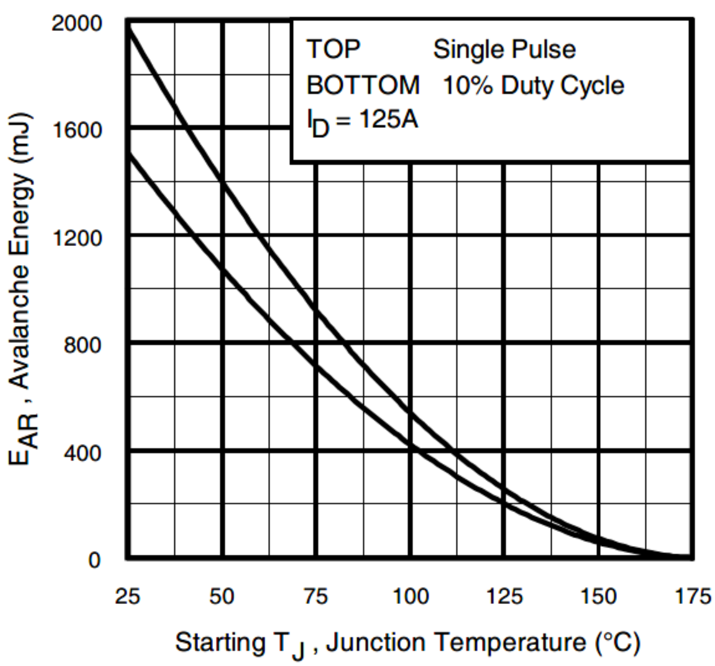
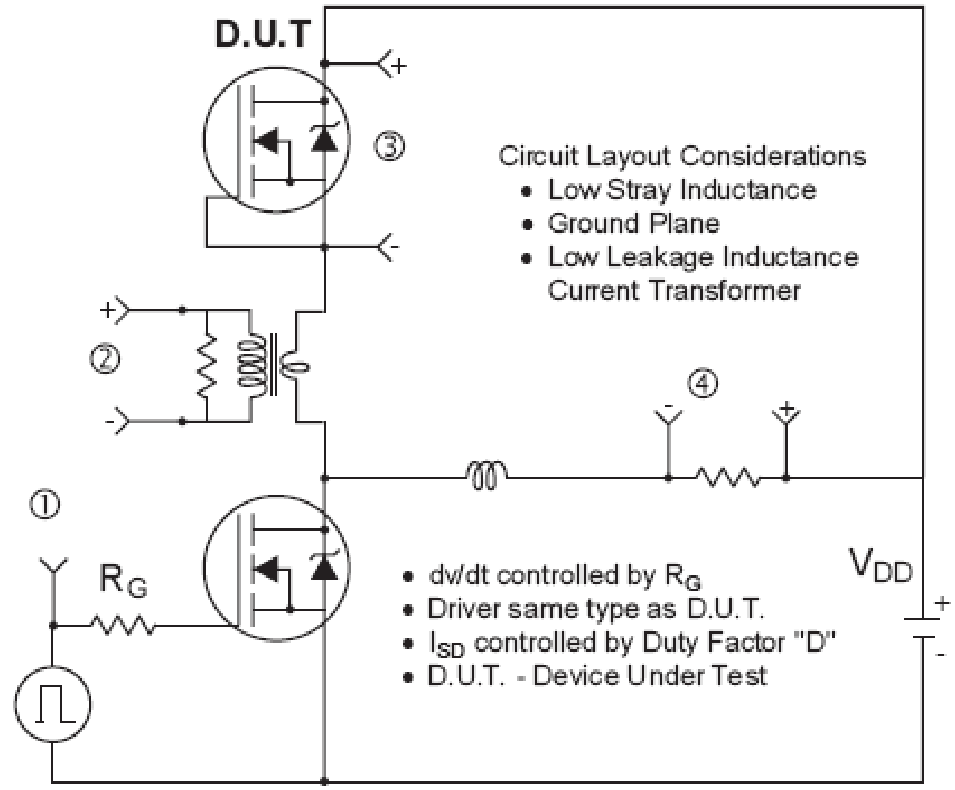


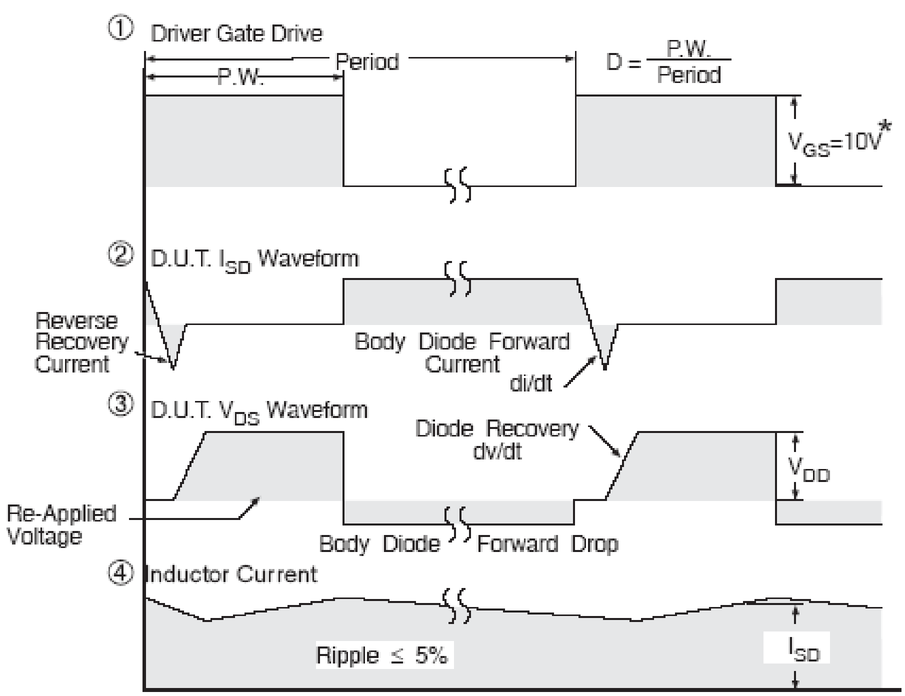
Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of Tjmax. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as Tjmax is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed Tjmax (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = tav ·f
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

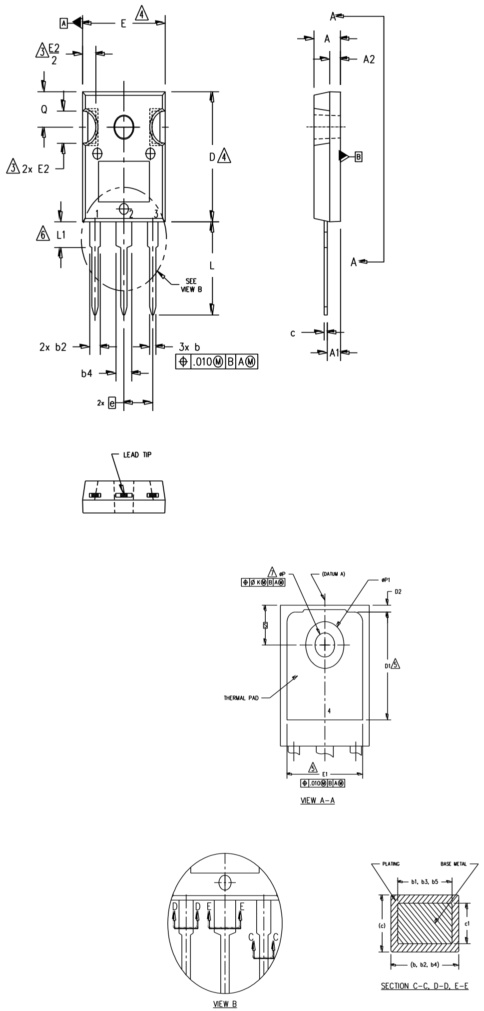




* V_{GS} = 5V for Logic Level Devices

Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

TO-247AC Package Outline (Dimensions are



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

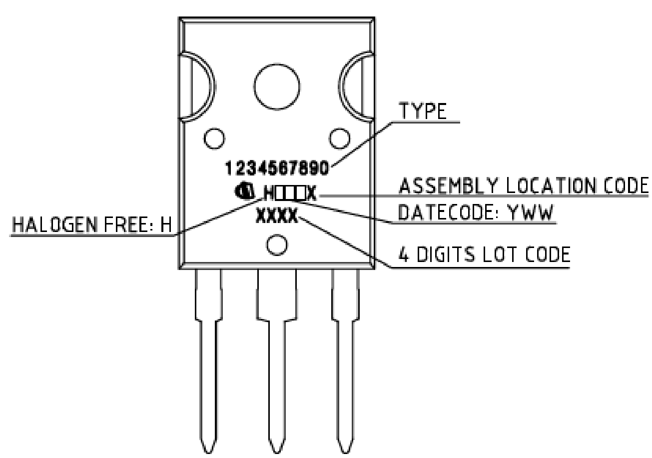
IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

DIODES

1.- ANODE/OPEN
2.- CATHODE
3.- ANODE

TO-247AC Part Marking Information



TO-247AC package is not recommended for Surface Mount Application.

Revision History

Date	Rev.	Comments
2024-10-15	2.1	• Update datasheet to Infineon format • Updated Part marking –page 9 • Added disclaimer on last page.

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