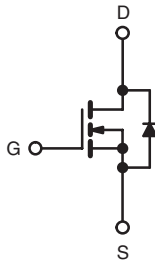


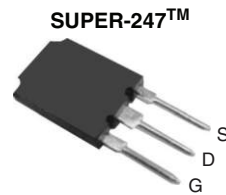
## Power MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	600	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.175
$Q_g$ (Max.) (nC)	220	
$Q_{gs}$ (nC)	67	
$Q_{gd}$ (nC)	96	
Configuration	Single	



N-Channel MOSFET



### FEATURES

- Super Fast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simpler Drive Requirements
- Enhances dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offer Improved Noise Immunity
- Lead (Pb)-free Available


**RoHS\***  
COMPLIANT

### APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control Applications

### ORDERING INFORMATION

Package	SUPER-247™
Lead (Pb)-free	IRFPS29N60LPbF
	SiHFPS29N60L-E3
SnPb	IRFPS29N60L
	SiHFPS29N60L

### ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	110	
Linear Derating Factor		3.8	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	570	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	29	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	48	mJ
Maximum Power Dissipation	$P_D$	480	W
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	15	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	
		1.1	N · m

#### Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1.5\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 29\text{ A}$  (see fig.12a).
- $I_{SD} \leq 29\text{ A}$ ,  $dI/dt \leq 830\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain) <sup>a</sup>	$R_{thJC}$	-	0.26	

### Note

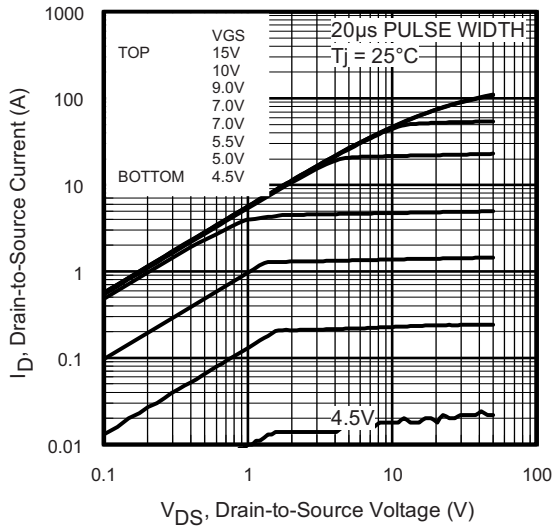
a.  $R_{th}$  is measured at  $T_J$  approximately 90 °C.

SPECIFICATIONS $T_J = 25\text{ °C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1\text{ mA}$		-	0.53	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	50	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$		-	-	2.0	mA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 17\text{ A}^b$	-	0.175	0.21	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 17\text{ A}^b$		15	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5 <sup>b</sup>		-	6160	-	pF
Output Capacitance	$C_{oss}$			-	530	-	
Reverse Transfer Capacitance	$C_{rss}$			-	44	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to } 480\text{ V}^c$		-	250	-	pF
Effective Output Capacitance (Energy Related)	$C_{oss\text{ eff. (ER)}}$			-	190	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 29\text{ A}, V_{DS} = 480\text{ V}$ , see fig. 7 and 15 <sup>b</sup>	-	-	220	nC
Gate-Source Charge	$Q_{gs}$			-	-	67	
Gate-Drain Charge	$Q_{gd}$			-	-	96	
Internal Gate Resistance	$R_G$	$f = 1\text{ MHz}$ , open drain		-	0.86	-	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 29\text{ A}, R_G = 4.3\text{ }\Omega, V_{GS} = 10\text{ V}$ , see fig. 11a and 11b <sup>b</sup>		-	34	-	ns
Rise Time	$t_r$			-	100	-	
Turn-Off Delay Time	$t_{d(off)}$			-	66	-	
Fall Time	$t_f$			-	54	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	29	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	110	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ °C}, I_S = 29\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ °C}, I_F = 29\text{ A}$ $T_J = 125\text{ °C}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	130	190	ns
				-	240	360	
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	630	950	$\mu\text{C}$
				-	1820	2720	
Body Diode Recovery Current	$I_{RRM}$	$T_J = 25\text{ °C}$		-	9.4	14	A
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

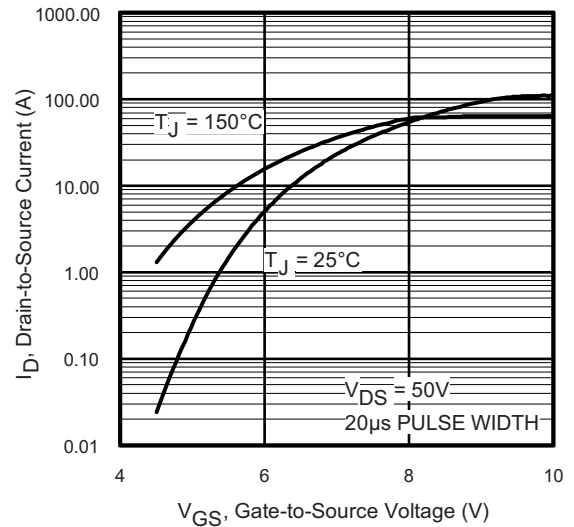
### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80 %  $V_{DS}$ .  
 $C_{oss\text{ eff. (ER)}}$  is a fixed capacitance that stores the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80 %  $V_{DS}$ .

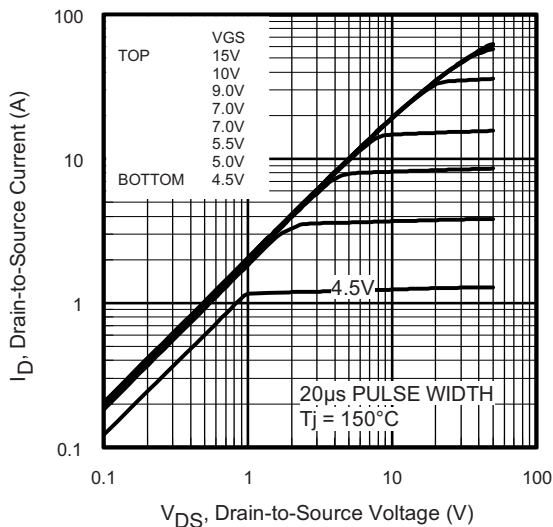
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



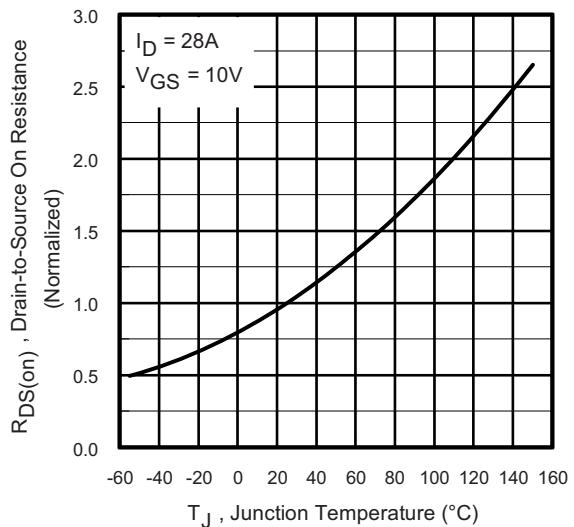
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

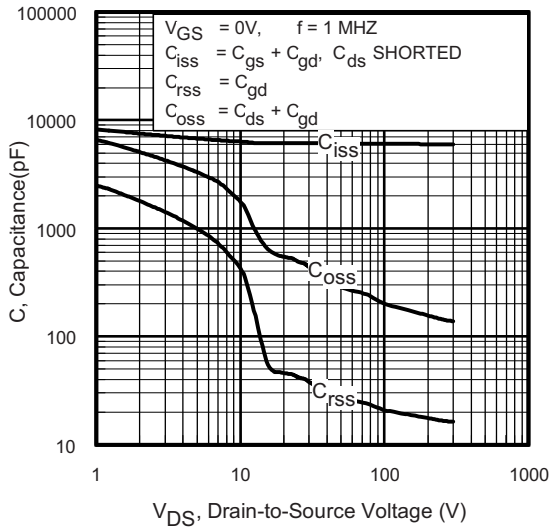


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

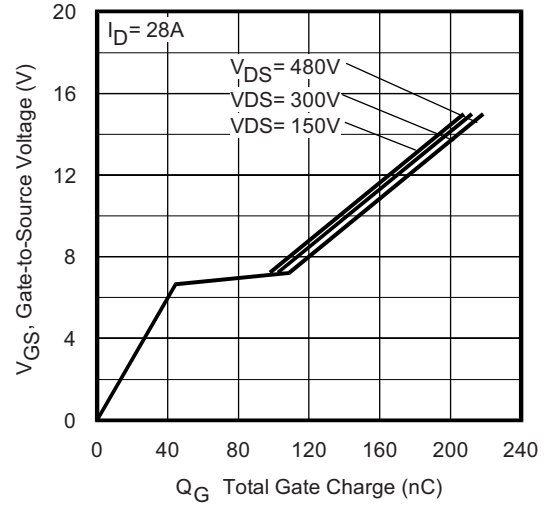


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

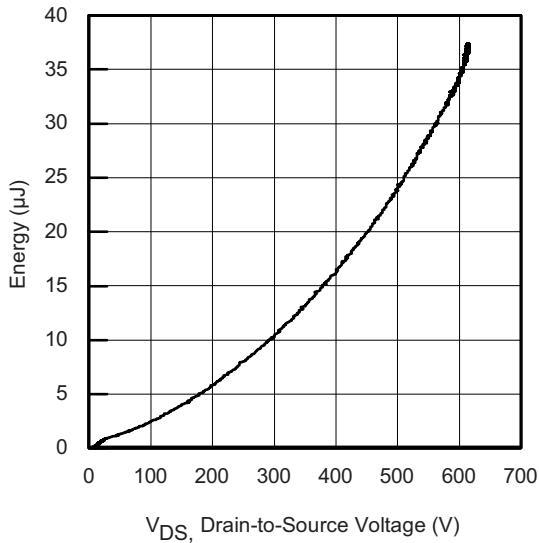


Fig. 6 - Typical Output Capacitance Stored Energy vs.  $V_{DS}$

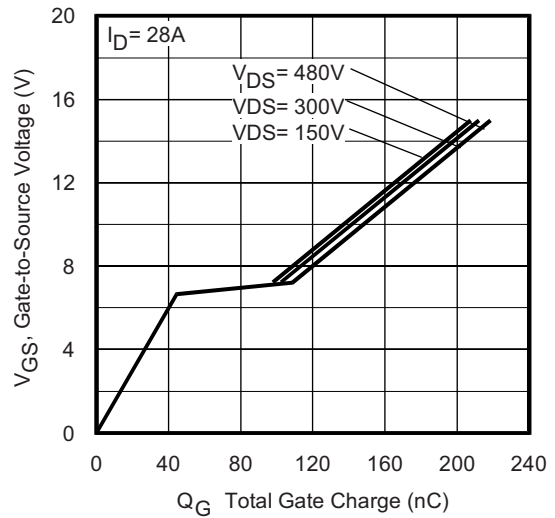
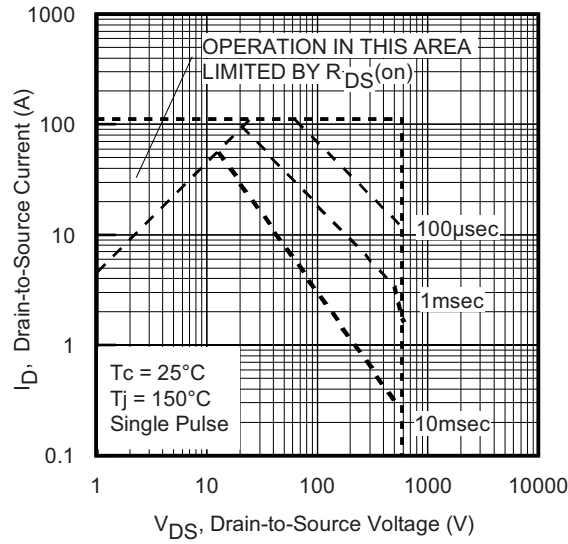
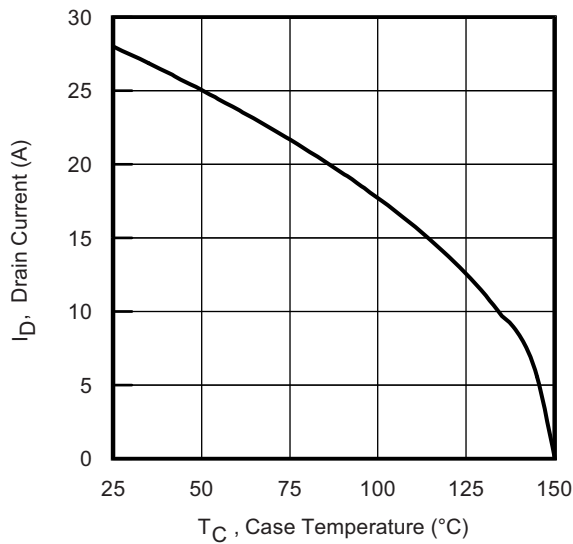


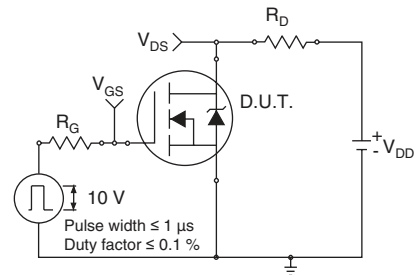
Fig. 8 - Typical Source-Drain Diode Forward Voltage



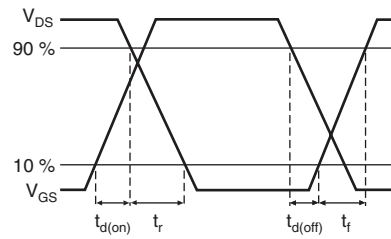
**Fig. 9 - Maximum Safe Operating Area**



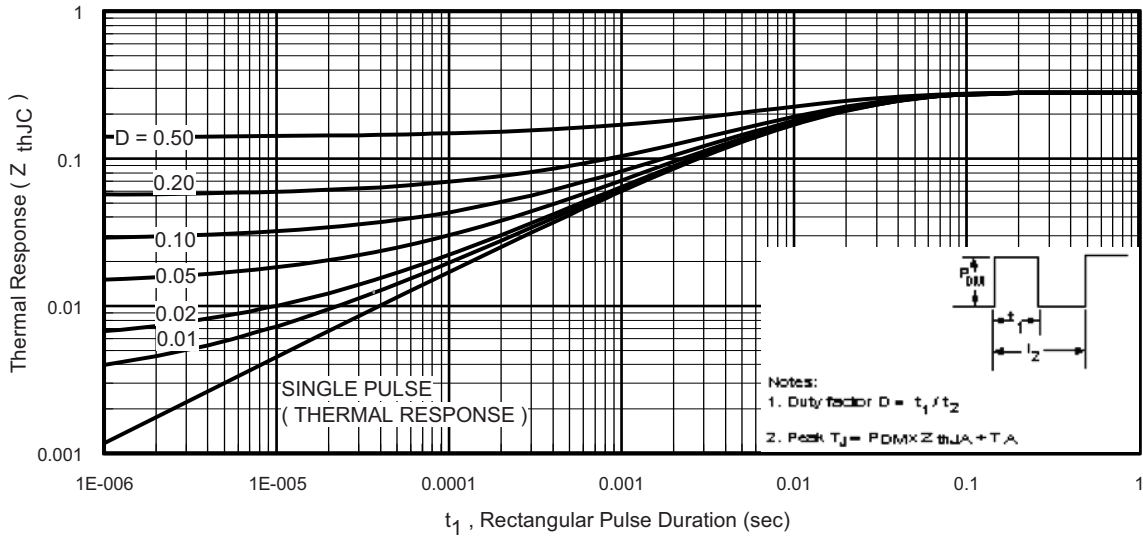
**Fig. 10 - Maximum Drain Current vs. Case Temperature**



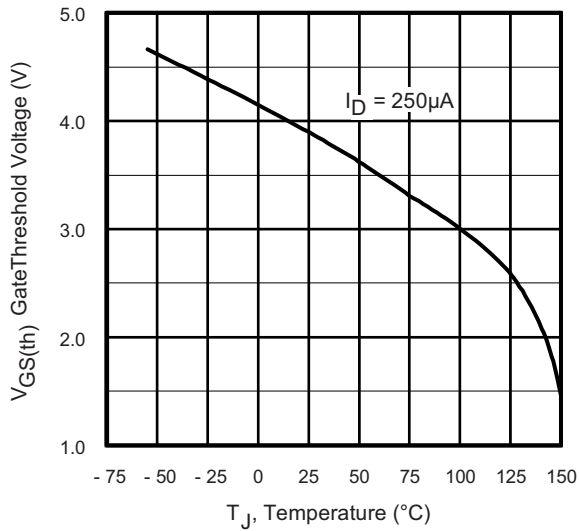
**Fig. 11a - Switching Time Test Circuit**



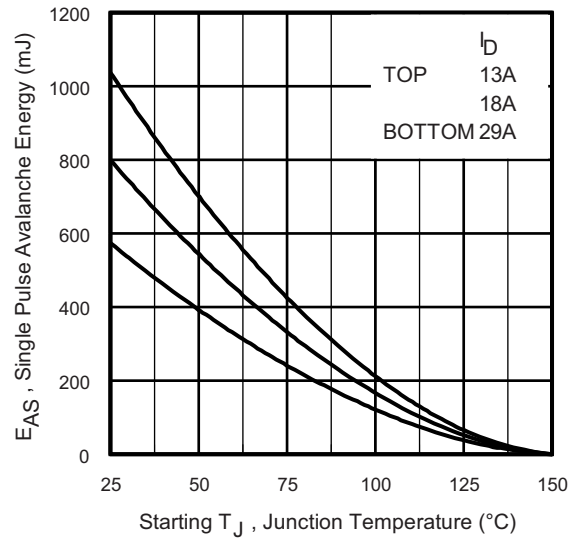
**Fig. 11b - Switching Time Waveforms**



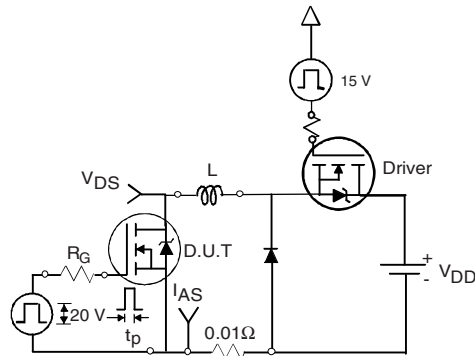
**Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



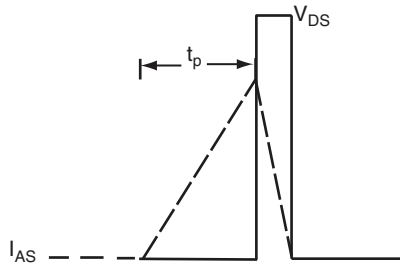
**Fig. 13 - Threshold Voltage vs. Temperature**



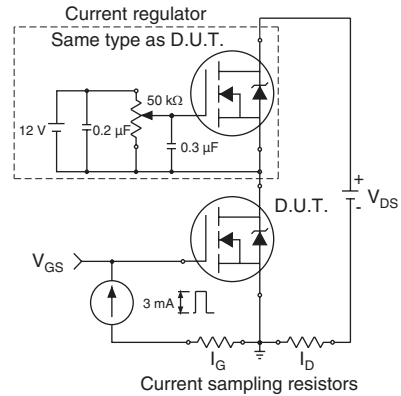
**Fig. 14a - Maximum Avalanche Energy vs. Drain Current**



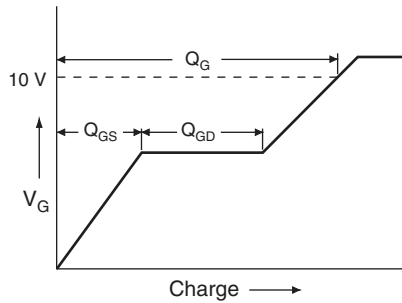
**Fig. 14b - Unclamped Inductive Test Circuit**



**Fig. 14c - Unclamped Inductive Waveforms**

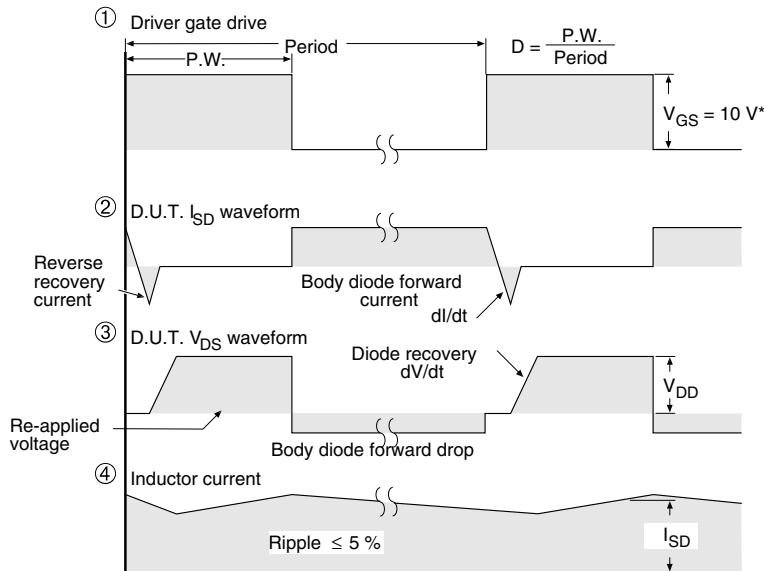
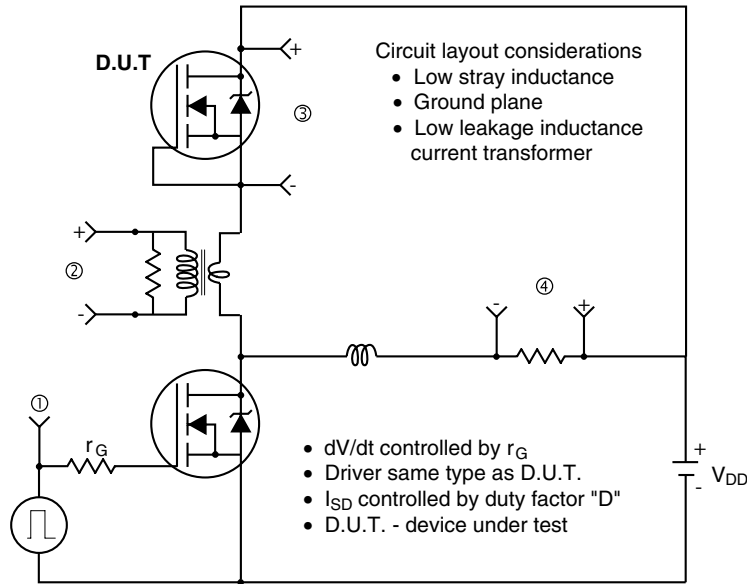


**Fig. 15a - Gate Charge Test Circuit**



**Fig. 15b - Basic Gate Charge Waveform**

## Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5 V$  for logic level devices

Fig. 16 - For N-Channel

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