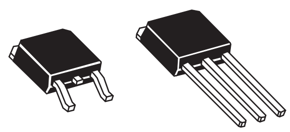
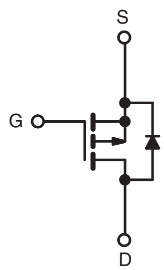
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	- 50	
$R_{DS(on)}$ (Ω)	V_{GS} = - 10 V	0.33
Q_g (Max.) (nC)	14	
Q_{gs} (nC)	6.5	
Q_{gd} (nC)	6.5	
Configuration	Single	

DPAK (TO-252) IPAK (TO-251)





P-Channel MOSFET

FEATURES

- Surface Mountable (Order as IRFR9022/SiHFR9022)
- Straight Lead Option (Order as IRFU9022/SiHFU9022)
- Repetitive Avalanche Ratings
- Dynamic dV/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Lead (Pb)-free Available

Pb Available
RoHS*
COMPLIANT

DESCRIPTION

The Power MOSFET technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dV/dt.

The Power MOSFET transistors also feature all of the well established advantages of MOSFET'S such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The TO-252 surface mount package brings the advantages of Power MOSFET's to high volume applications where PC Board surface mounting is desirable. The surface mount option IRFR9022/SiHFR9022 is provided on 16mm tape. The straight lead option IRFR9022/SiHFR9022 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, DC/DC converters, and a wide range of consumer products.

ORDERING INFORMATION				
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRFR9022PbF	IRFR9022TRPbF[a]	IRFR9022TRLPbF[a]	IRFU9022PbF
	SiHFR9022-E3	SiHFR9022T-E3[a]	SiHFR9022TL-E3[a]	SiHFU9022-E3
SnPb	IRFR9022	IRFR9022TR[a]	IRFR9022TRL[a]	IRFU9022
	SiHFR9022	SiHFR9022T[a]	SiHFR9022TL[a]	SiHFU9022

Note
a. See device orientation.

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	- 50	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	T_C = 25 °C	I_D	- 9.0	A
		T_C = 100 °C		- 5.7	
Pulsed Drain Current[a]			I_{DM}	- 36	
Linear Derating Factor				0.33	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	440	mJ
Repetitive Avalanche Current[a]			I_{AR}	- 9.9	A
Repetitive Avalanche Energy[a]			E_{AR}	4.2	mJ

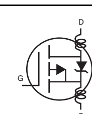
* Pb containing terminations are not RoHS compliant, exemptions may apply

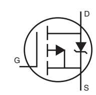
ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Maximum Power Dissipation	T_C = 25 °C	P_D	42	W
Peak Diode Recovery dV/dt[c]		dV/dt	5.8	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300[d]	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).
b. V_{DD} = - 25 V, Starting T_J = 25 °C, L = 5.1 mH, R_G = 25 Ω, Peak I_L = - 9.9 A
c. $I_{SD} \leq$ - 9.9 A, dI/dt ≤ -120 A/µs, $V_{DD} \leq$ 40 V, $T_J \leq$ 150 °C.
d. 0.063" (1.6 mm) from case.
e. When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W
Case-to-Sink	R_{thCS}	-	1.7	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	3.0	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA		- 50	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = max. rating, V_{GS} = 0 V		-	-	250	µA
		V_{DS} = 0.8 x max. rating, V_{GS} = 0 V, T_J = 125 °C		-	-	1000	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = - 10 V	I_D = 5.7 A[b]	-	0.28	0.33	Ω
Forward Transconductance	g_{fs}	$V_{DS} \leq$ - 50 V, I_{DS} = - 5.7 A		2.3	3.5	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = - 25 V, f = 1.0 MHz, see fig. 9		-	490	-	pF
Output Capacitance	C_{oss}			-	320	-	
Reverse Transfer Capacitance	C_{rss}			-	70	-	
Total Gate Charge	Q_g	V_{GS} = - 10 V	I_D = - 9.7 A, V_{DS} = 0.8 x max. rating, see fig. 16 (Independent operating temperature)	-	9.4	14	nC
Gate-Source Charge	Q_{gs}			-	4.3	6.5	
Gate-Drain Charge	Q_{gd}			-	4.3	6.5	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 25 V, I_D = - 9.7 A, R_G = 18 Ω, R_D = 2.4 Ω, see fig. 15 (Independent operating temperature)		-	8.2	12	ns
Rise Time	t_r			-	57	66	
Turn-Off Delay Time	$t_{d(off)}$			-	12	18	
Fall Time	t_f			-	25	38	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact.		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	- 9.9	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	- 40	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = - 9.9 A, V_{GS} = 0 V[b]	-	-	- 6.3	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = - 9,7 A, dI/dt = 100 A/µs[b]	56	110	280	ns
Body Diode Reverse Recovery Charge	Q_{rr}		0.17	0.34	0.85	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

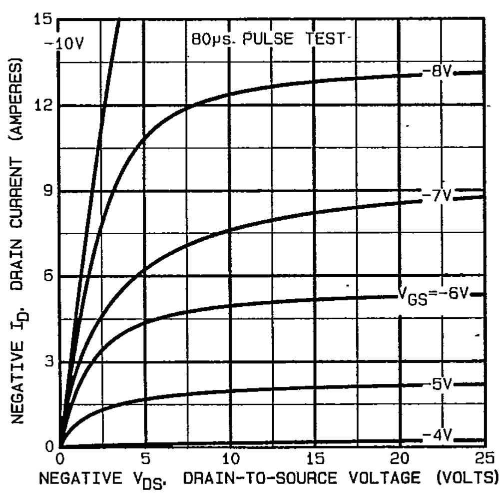


Fig. 1 - Typical Output Characteristics

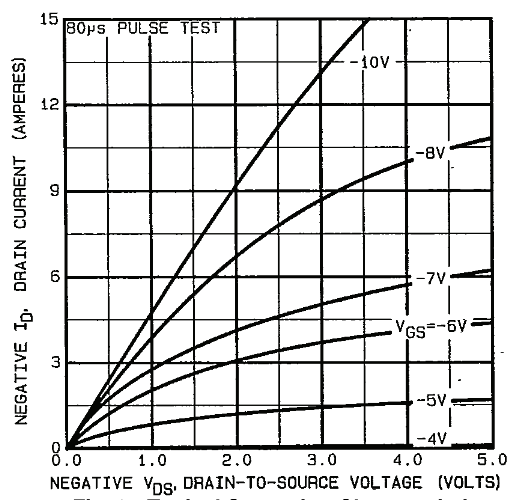


Fig. 3 - Typical Saturation Characteristics

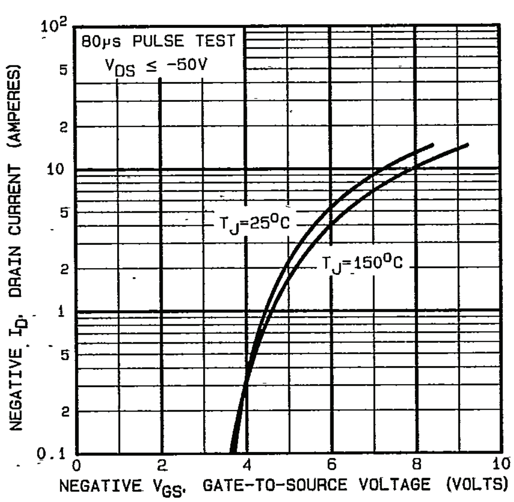


Fig. 2 - Typical Transfer Characteristics

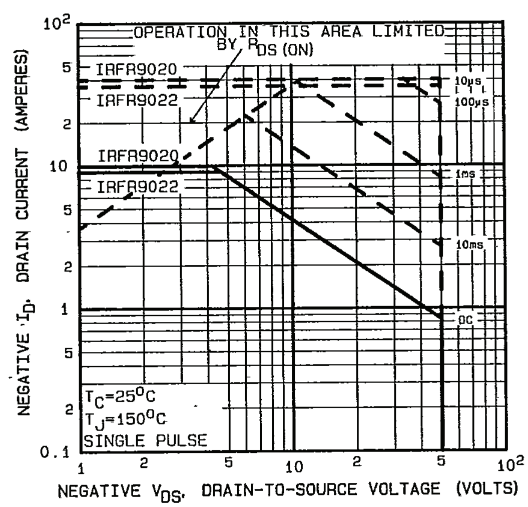


Fig. 4 - Maximum Safe Operating Area

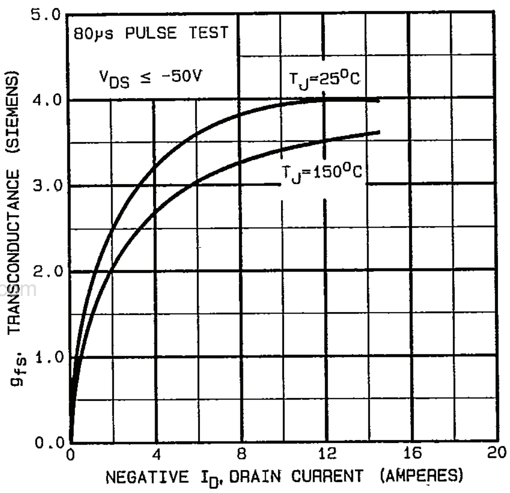


Fig. 5 - Typical Transconductance vs. Drain Current

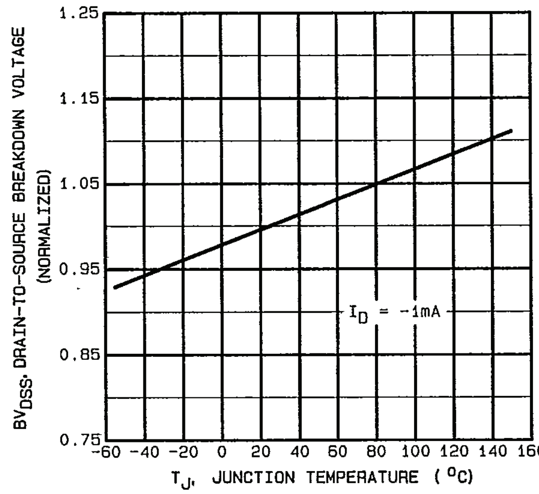


Fig. 7 - Breakdown Voltage vs. Temperature

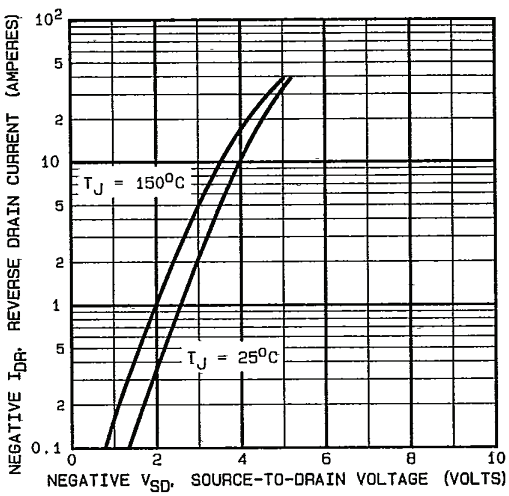


Fig. 6 - Typical Source-Drain Diode Forward Voltage

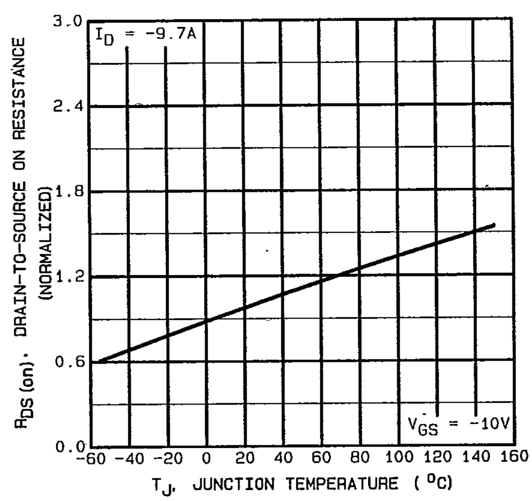


Fig. 8 - Normalized On-Resistance vs. Temperature

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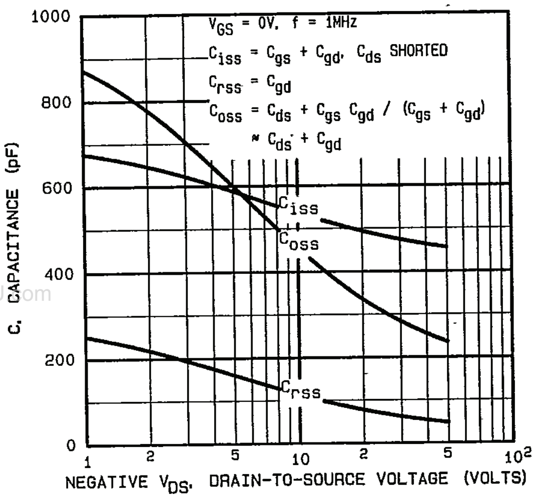


Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage

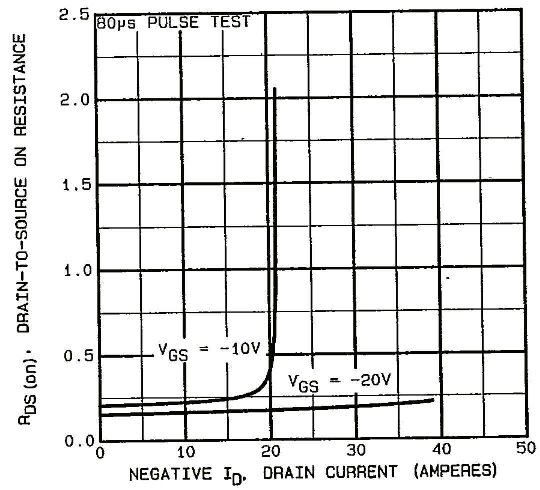


Fig. 11 - Typical On-Resistance vs. Drain Current

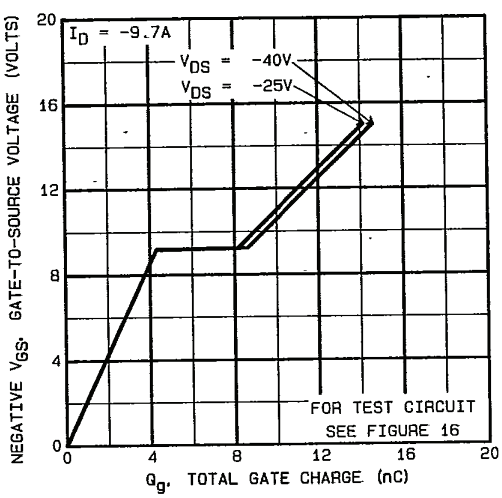


Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

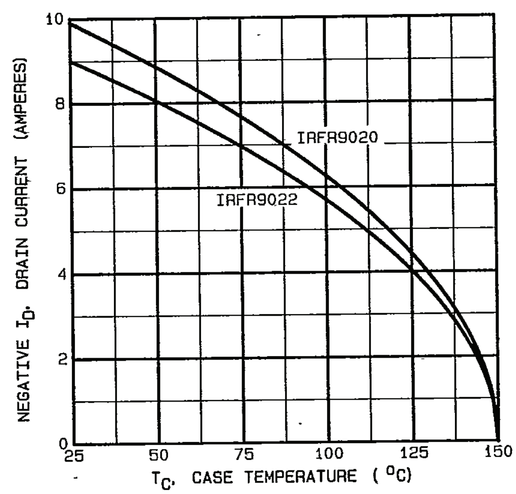


Fig. 12 - Maximum Drain Current vs. Case Temperature

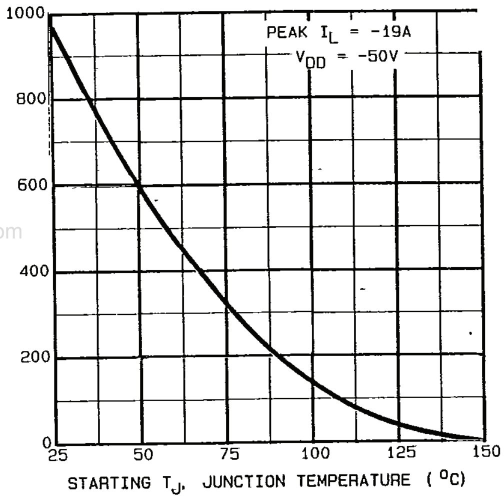


Fig. 13a - Maximum Avalanche vs. Starting Junction Temperature

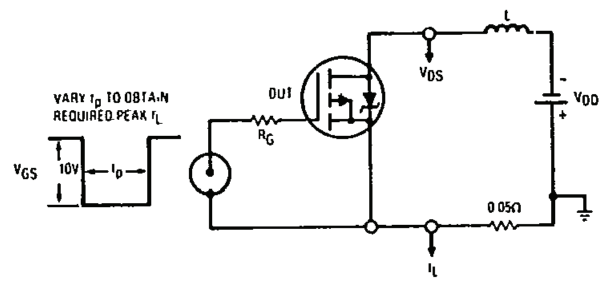


Fig. 13b - Unclamped Inductive Test Circuit

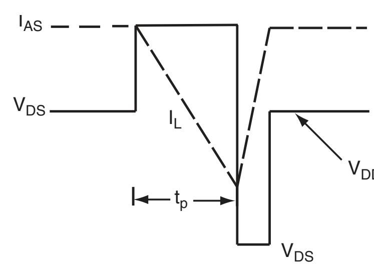


Fig. 13c - Unclamped Inductive Waveforms

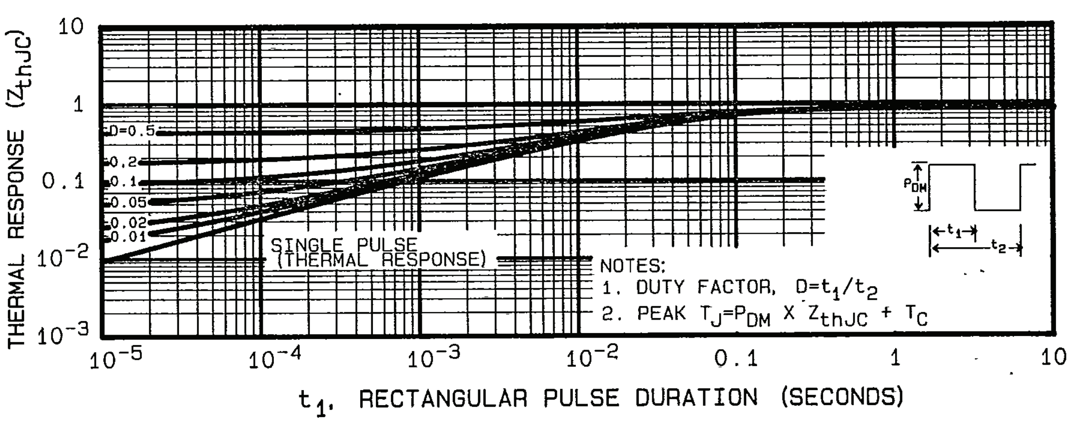


Fig. 14 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

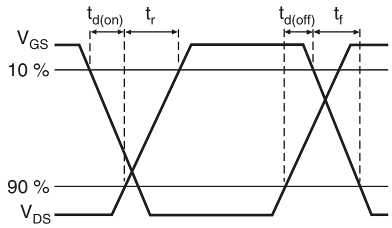


Fig. 15a - Switching Time Waveforms

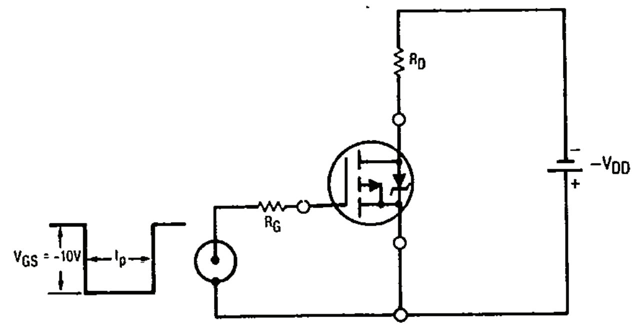


Fig. 15b - Switching Time Test Circuit

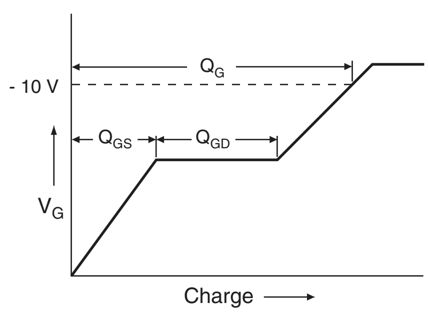


Fig. 16a - Basic Gate Charge Waveform

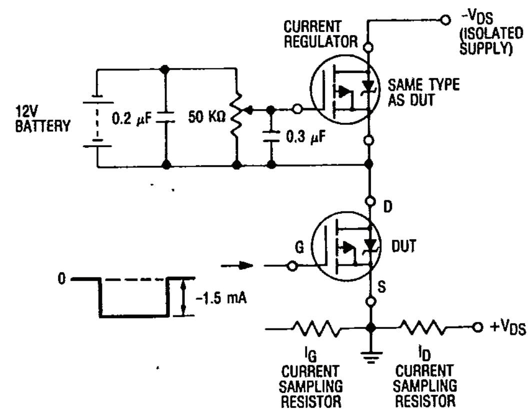
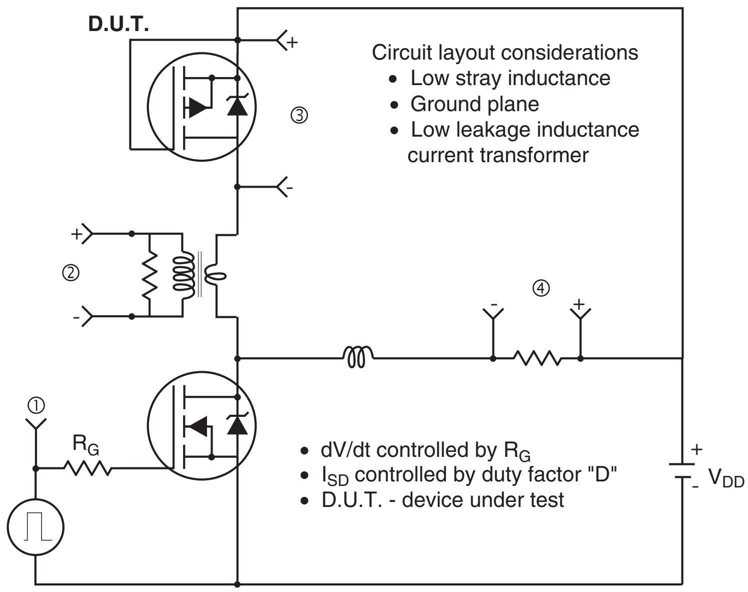
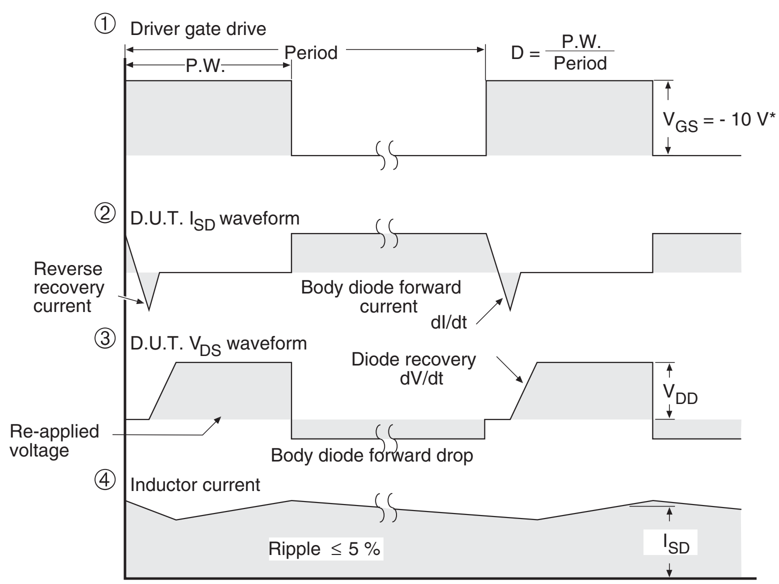


Fig. 16b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



• Compliment N-Channel of D.U.T. for driver



* V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig. 17 - For P-Channel

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