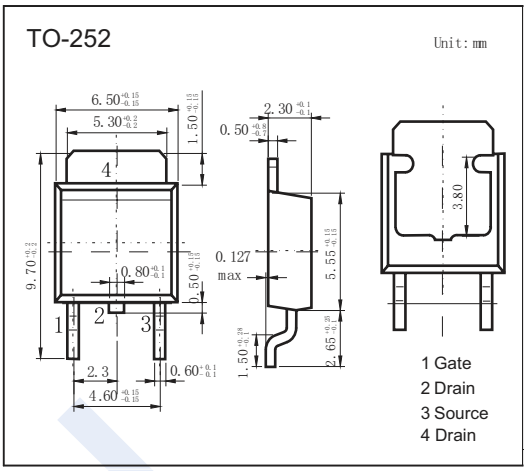
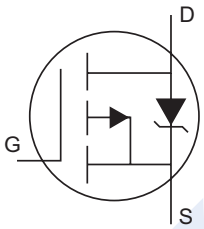
P-Channel MOSFET

IRFR9024N



■ Features

- V_{DS} (V) =- 55V
- I_D =-11 A (V_{GS} =-10V)
- $R_{DS(ON)}$ < 0.175Ω (V_{GS} =-10V)



■ Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	-55	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current, V_{GS} @ -10V	T_C = 25 °C	I_D	-11	A
	T_C = 100 °C		-8	
Pulsed Drain Current *1		I_{DM}	-44	
Single Pulse Avalanche Energy *2		E_{AS}	62	mJ
Avalanche Current *1		I_{AR}	-6.6	A
Repetitive Avalanche Energy *1		E_{AR}	3.8	mJ
Peak Diode Recovery dv/dt *3		dv/dt	-10	V/ns
Power Dissipation	T_C = 25 °C	P_D	38	W
Thermal Resistance.Junction- to-Ambient (PCB mount *4)		R_{thJA}	50	℃/W
Thermal Resistance.Junction- to-Ambient			110	
Thermal Resistance.Junction- to-Case		R_{thJC}	3.3	
Junction Temperature		T_J	150	℃
Junction Storage Temperature Range		T_{stg}	-55 to 150	

Notes:

*1. Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

*2. Starting T_J = 25℃, L = 2.8mH, R_G = 25Ω, I_{AS} = -6.6A. (See Figure 12)

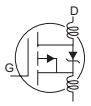
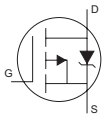
*3. I_{SD} ≤-6.6A, di/dt ≤240A/μs, V_{DD}≤ $V_{(BR)DSS}$, T_J ≤150℃

*4 When mounted on 1" square PCB (FR-4 Material) .

P-Channel MOSFET

IRFR9024N

■ Electrical Characteristics (T_J = 25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	I_D=-250μA, V_{GS}=0V	-55			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-55V, V_{GS}=0V			-25	μA
		V_{DS}=-44V, V_{GS}=0V, T_J=150℃			-250	
Gate-Body Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} , I_D=-250μA	-2		-4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-6.6A *5			0.175	Ω
Forward Transconductance	g_{fs}	V_{DS}=-25V, I_D=-7.2A	2.5			S
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-25V, f=1MHz See Fig. 5		350		pF
Output Capacitance	C_{oss}			170		
Reverse Transfer Capacitance	C_{rss}			92		
Total Gate Charge	Q_g	V_{GS}=-10V, V_{DS}=-44V, I_D=-7.2A See Fig. 6 and 13 *5			19	nC
Gate Source Charge	Q_{gs}				5.1	
Gate Drain Charge	Q_{gd}				10	
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=-28V,I_D = - 7.2 A, R_G = 24Ω,R_D=3.7Ω, See Fig. 10 *5		13		ns
Turn-On Rise Time	t_r			55		
Turn-Off Delay Time	$t_{d(off)}$			23		
Turn-Off Fall Time	t_f			37		
Internal Drain Inductance	L_D	Between lead and center of die contact 		4.5		nH
Internal Source Inductance	L_S			7.5		
Body Diode Reverse Recovery Time	t_{rr}	I_F=-7.2A, dI/dt=100A/μs *5		47	71	ns
Body Diode Reverse Recovery Charge	Q_{rr}			84	130	nC
Body Diode Continuous Source Current	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 			-11	A
Maximum Body Diode Pulsed Current	I_{SM}				--44	
Diode Forward Voltage	V_{SD}	I_S=-7.2A,V_{GS}=0V *5			-1.6	V
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

*5. Pulse width ≤300μs; duty cycle≤2%.

P-Channel MOSFET

IRFR9024N

■ Typical Characterisitics

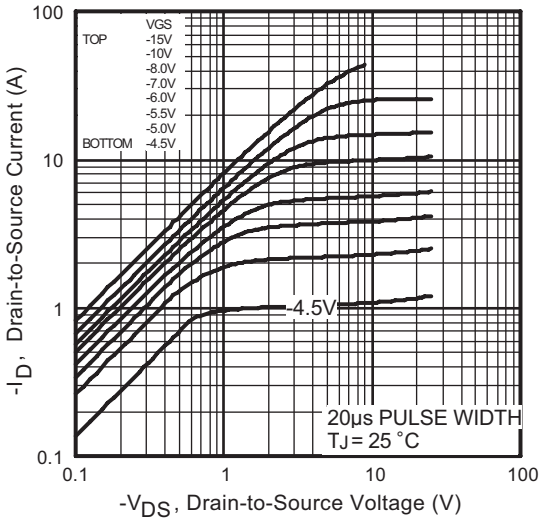


Fig 1. Typical Output Characteristics

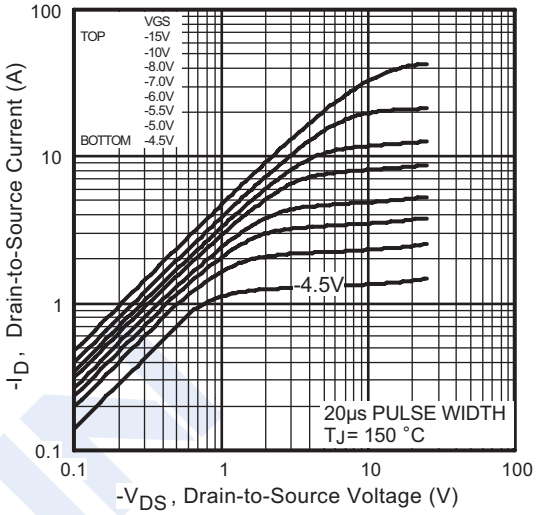


Fig 2. Typical Output Characteristics

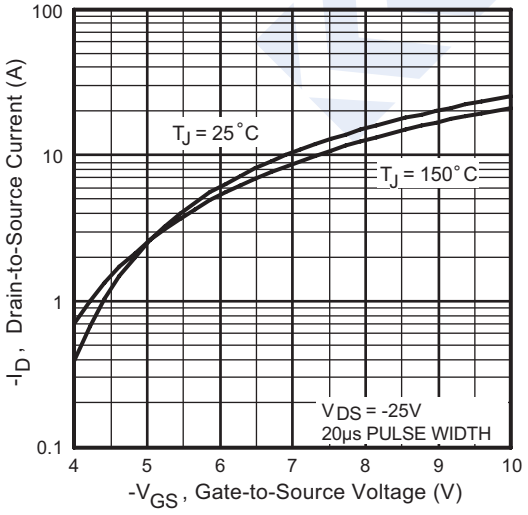


Fig 3. Typical Transfer Characteristics

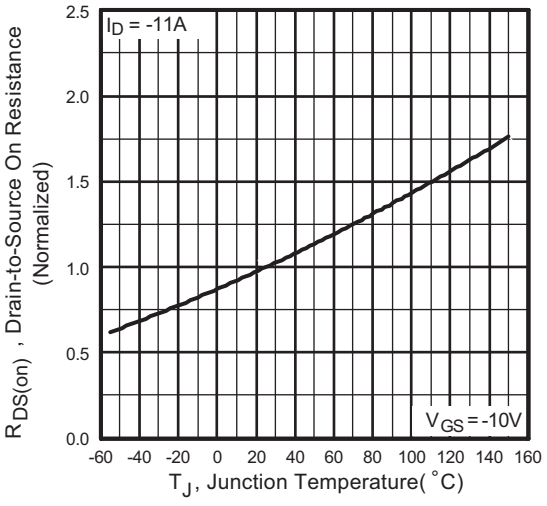


Fig 4. Normalized On-Resistance Vs. Temperature

P-Channel MOSFET

IRFR9024N

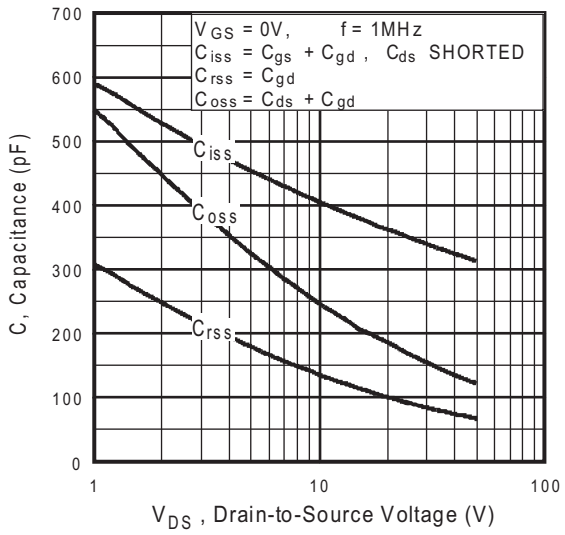


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

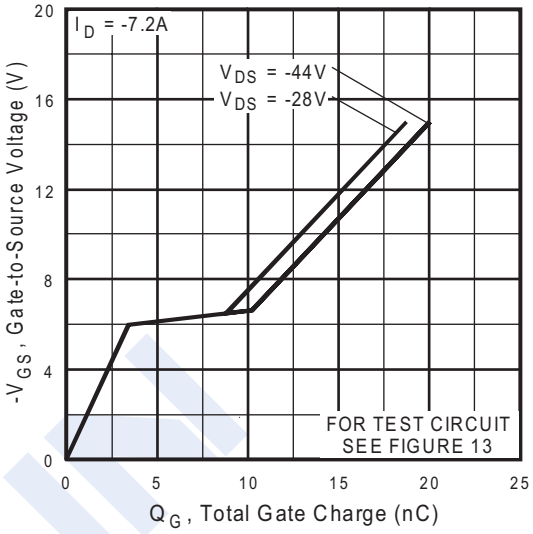


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

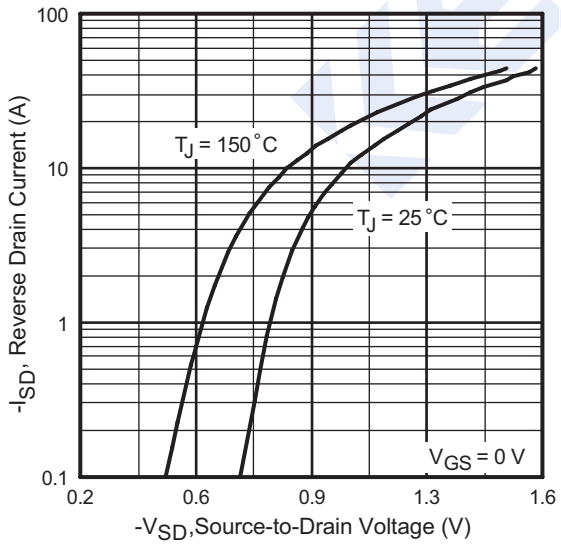


Fig 7. Typical Source-Drain Diode Forward Voltage

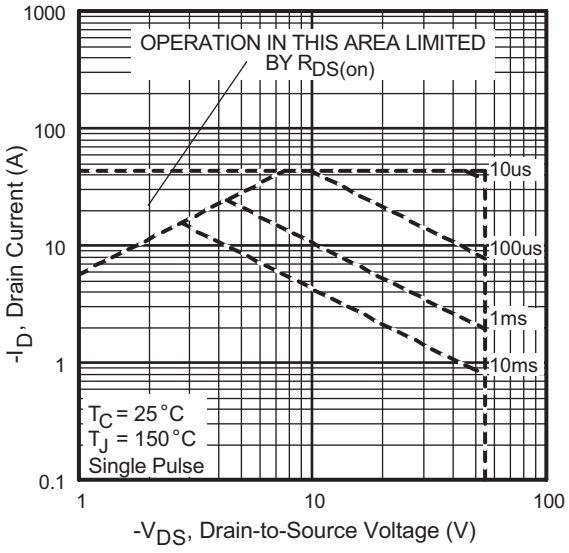


Fig 8. Maximum Safe Operating Area

P-Channel MOSFET

IRFR9024N

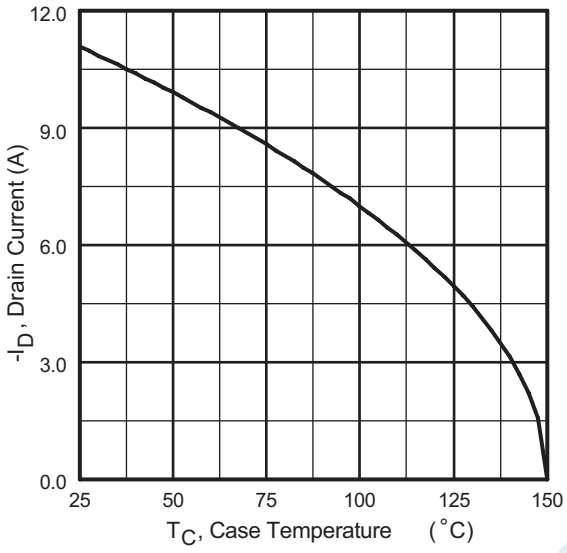


Fig 9. Maximum Drain Current Vs. Case Temperature

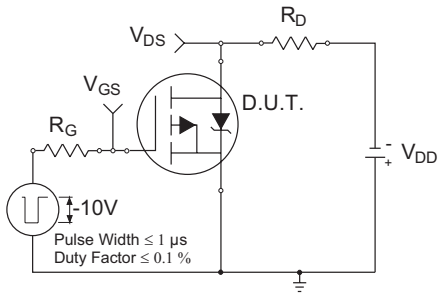


Fig 10a. Switching Time Test Circuit

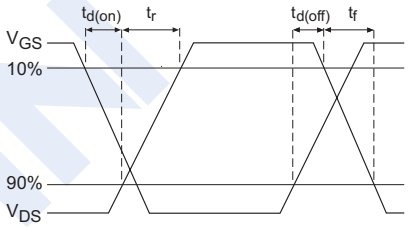


Fig 10b. Switching Time Waveforms

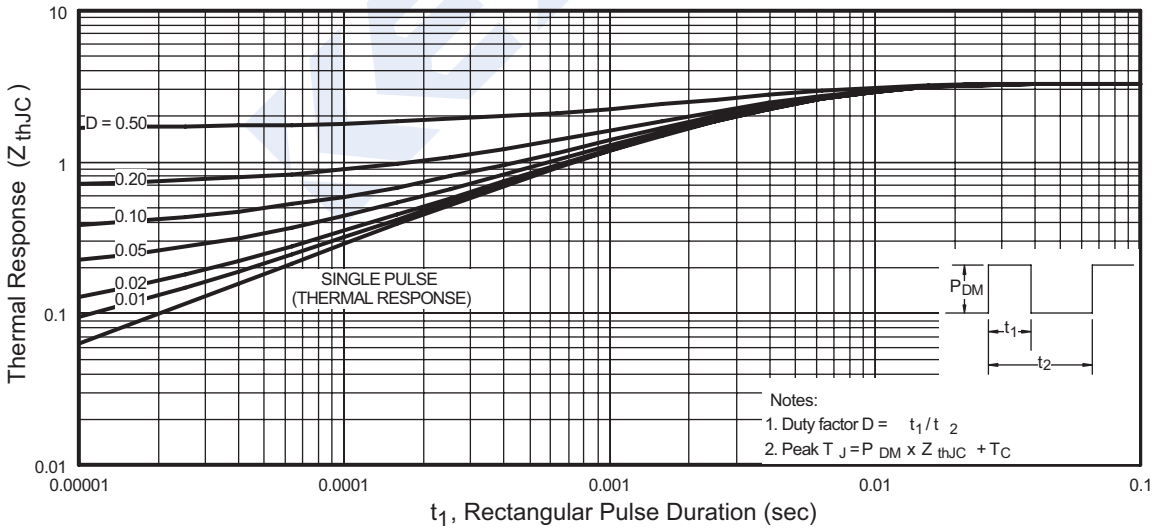


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

P-Channel MOSFET

IRFR9024N

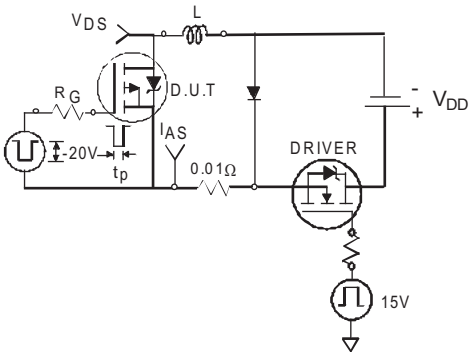


Fig 12a. Unclamped Inductive Test Circuit

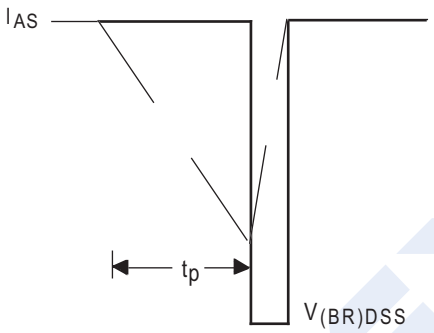


Fig 12b. Unclamped Inductive Waveforms

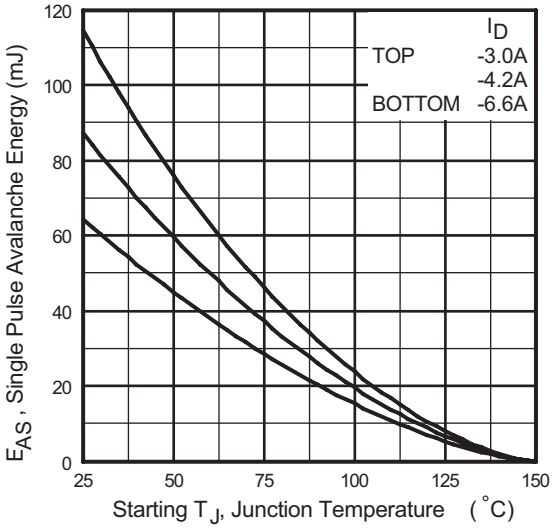


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

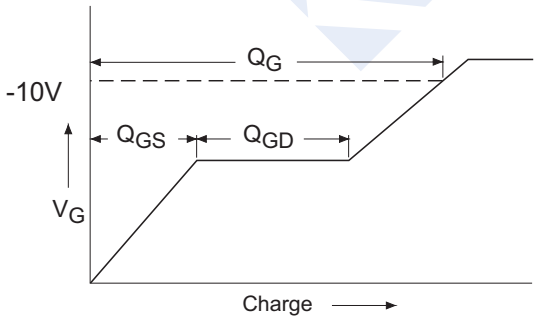


Fig 13a. Basic Gate Charge Waveform

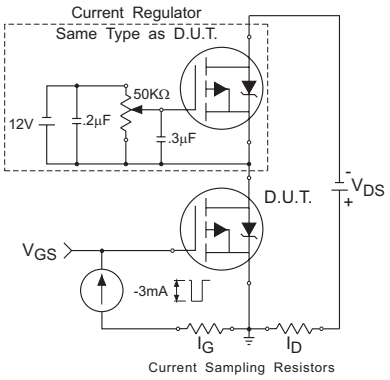
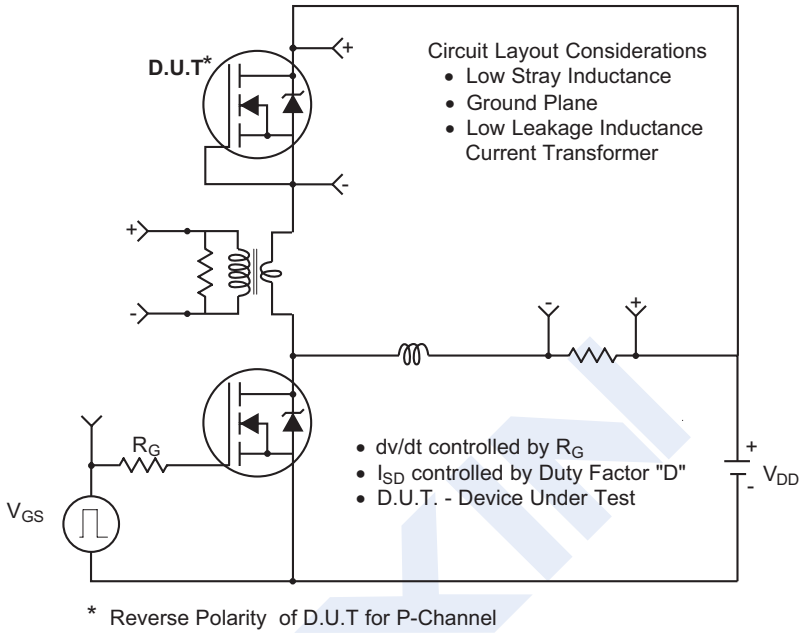


Fig 13b. Gate Charge Test Circuit

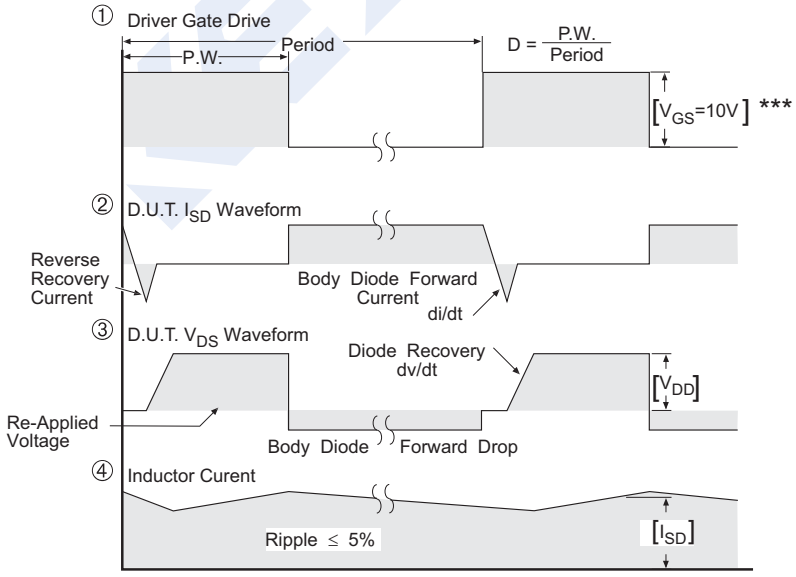
P-Channel MOSFET

IRFR9024N

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For P-Channel MOSFET