FAIRCHILD SEMICONDUCTOR™

August 1999
DISTRIBUTION GROUP*

IRFR9024

P-Channel Enhancement Mode Field Effect Transistor

General Description

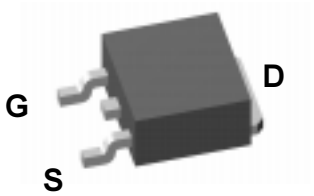
This P-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications.

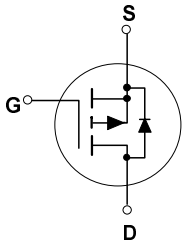
The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

Features

- -8.8 A, -60 V. $R_{DS(ON)}$ = 0.28 Ω @ V_{GS} = -10 V
- Low gate charge.
- Fast switching speed.
- High performance technology for low $R_{DS(ON)}$.



TO-252



Absolute Maximum Ratings

T_C=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		-60	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Maximum Drain Current -Continuous	(Note 1)	-8.8	A
	T_C = 100°C	(Note 1)	-5.6	
	Maximum Drain Current -Pulsed		-35	
P_D	Maximum Power Dissipation @ T_C = 25°C	(Note 1)	42	W
	T_A = 25°C	(Note 1a)	3.2	
	T_A = 25°C	(Note 1b)	1.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to- Case	(Note 1)	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to- Ambient	(Note 1a)	38	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
IRFR9024	IRFR9024	13"	16mm	2500

* Die and manufacturing source subject to change without prior notification.

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 2)						
w_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = -25 V, I_D = -8.8 A			300	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				-8.8	A
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C		-60		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -60 V, V_{GS} = 0 V			100	μA
		V_{DS} = -48 V, V_{GS} = 0 V, T_J = 125°C			500	
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-2	-2.3	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C		3.2		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -5.3 A,			0.280	Ω
g_{FS}	Forward Transconductance	V_{DS} = -25 V, I_D = -5.3 A	2.9			S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz		560		pF
C_{oss}	Output Capacitance			130		pF
C_{rss}	Reverse Transfer Capacitance			35		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -30 V, I_D = -11 A, V_{GS} = -10 V, R_{GEN} = 18 Ω		8		ns
t_r	Turn-On Rise Time			20		ns
$t_{d(off)}$	Turn-Off Delay Time			20		ns
t_f	Turn-Off Fall Time			5		ns
Q_g	Total Gate Charge	V_{DS} = -48 V, I_D = -11 A, V_{GS} = -10 V			19	nC
Q_{gs}	Gate-Source Charge				5.4	nC
Q_{gd}	Gate-Drain Charge				11	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current (Note 2)				-8.8	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current (Note 2)				-35	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -8.8 A (Note 2)			-6.3	V
t_{rr}	Drain-Source Reverse Recovery Time	I_F = -11 A, di/dt = 100A/μs			200	nS

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the drain tab. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ = 38°C/W when mounted on a 1 in^2 pad of 2oz copper.

b) $R_{\theta JA}$ = 96°C/W when mounted on a minimum pad.

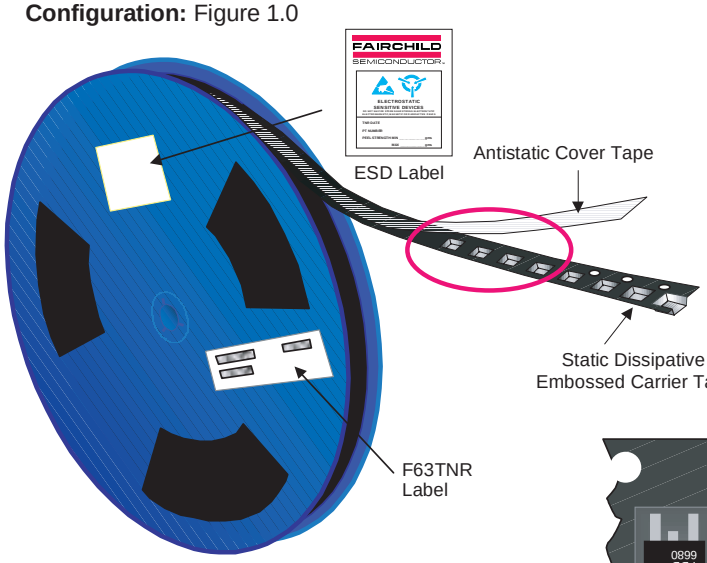
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TO-252 Tape and Reel Data and Package Dimensions

FAIRCHILD SEMICONDUCTOR™

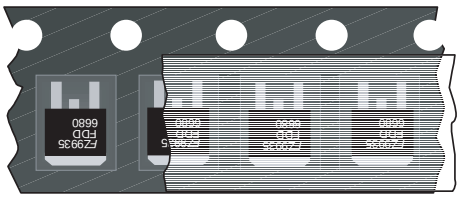
D-PAK (TO-252) Packaging Configuration: Figure 1.0



Packaging Description:

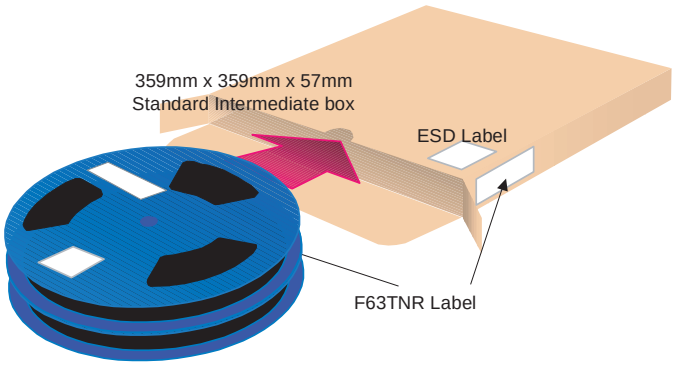
TO-252 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). This and some other options are further described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

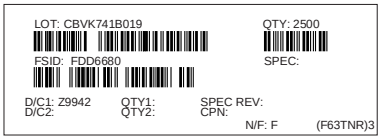


D-PAK (TO-252) Unit Orientation

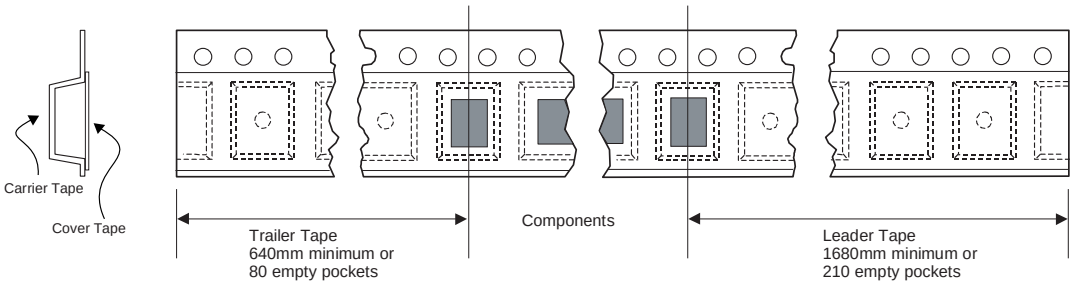
D-PAK (TO-252) Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	TNR
Qty per Reel/Tube/Bag	2,500
Reel Size	13" Dia
Box Dimension (mm)	359x359x57
Max qty per Box	5,000
Weight per unit (gm)	0.300
Weight per Reel(kg)	1.200
Note/Comments	



F63TNR Label sample



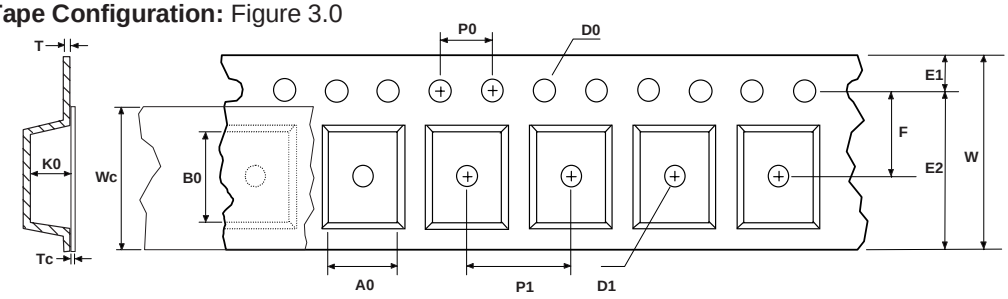
TO-252 (D-PAK) Tape Leader and Trailer Configuration: Figure 2.0



TO-252 Tape and Reel Data and Package Dimensions

D-PAK (TO-252) Embossed Carrier

Tape Configuration: Figure 3.0

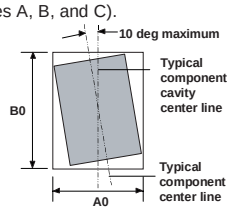


User Direction of Feed

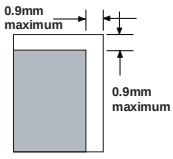
Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
TO252 (24mm)	6.90 +/-0.10	10.50 +/-0.10	16.0 +/-0.3	1.55 +/-0.05	1.5 +/-0.10	1.75 +/-0.10	14.25 min	7.50 +/-0.10	8.0 +/-0.1	4.0 +/-0.1	2.65 +/-0.10	0.30 +/-0.05	13.0 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Sketch A (Side or Front Sectional View)
Component Rotation



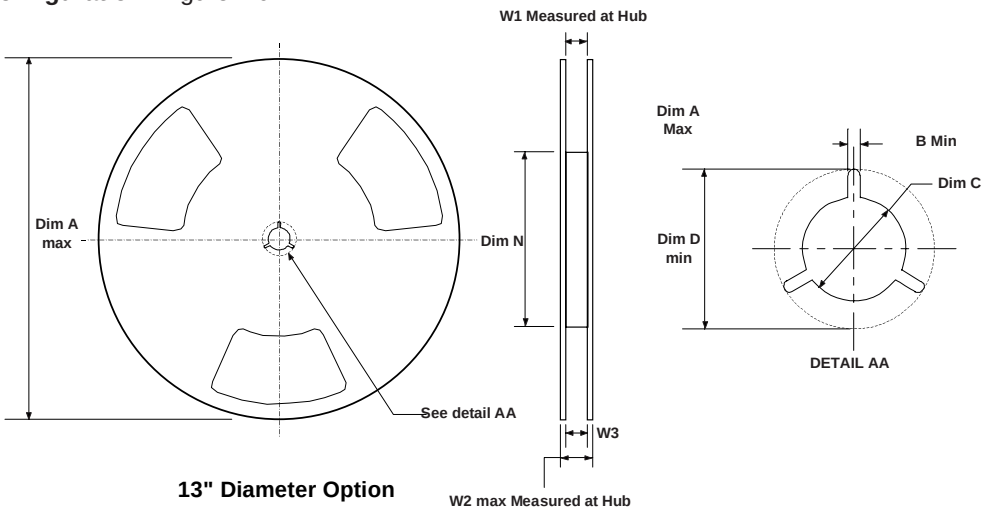
Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

D-PAK (TO-252) Reel

Configuration: Figure 4.0

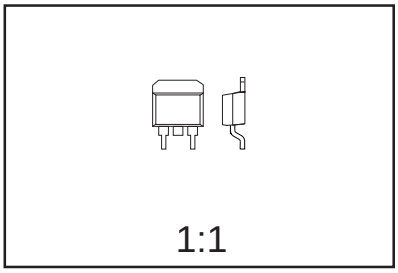


13" Diameter Option

Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
164mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.646 +0.078/-0.000 16.4 +2/0	0.882 22.4	0.626 – 0.764 15.9 – 19.4

TO-252 Tape and Reel Data and Package Dimensions

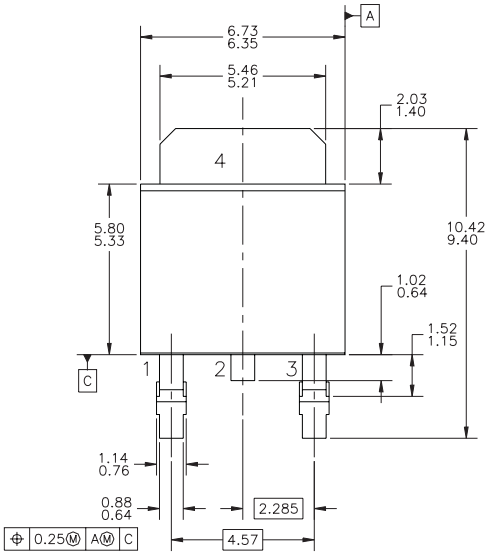
TO-252 (FS PKG Code AA)

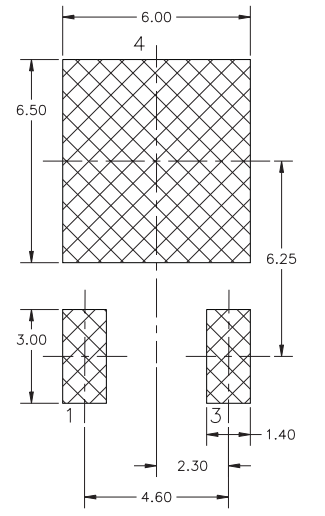


Scale 1:1 on letter size paper

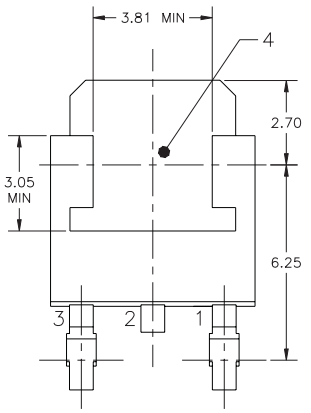
Dimensions shown below are in:
inches [millimeters]

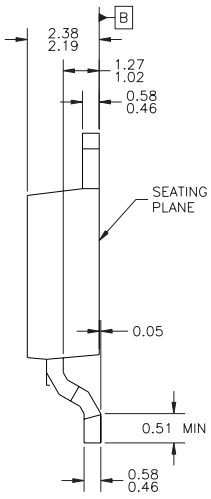
Part Weight per unit (gram): 0.300





LAND PATTERN RECOMMENDATION





NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE B, VARIATION AB, ITEM 10.268, DATED SEPTEMBER 1988.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™
CoolFET™
CROSSVOLT™
E^2CMOS^{TM}
FACT™
FACT Quiet Series™
FAST®
FASTr™
GTO™
HiSeC™
ISOPLANAR™
MICROWIRE™
POP™
PowerTrench®
QFET™
QS™
Quiet Series™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
TinyLogic™
UHC™
VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.