

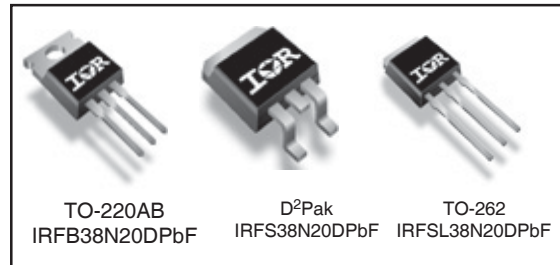
### Applications

- High frequency DC-DC converters
- Plasma Display Panel

### Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective  $C_{OSS}$  to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current
- Lead-Free

Key Parameters		
$V_{DS}$	200	V
$V_{DS(Avalanche)}$ min.	260	V
$R_{DS(ON)}$ max @ 10V	54	m $\Omega$
$T_J$ max	175	$^{\circ}C$



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^{\circ}C$	Continuous Drain Current, $V_{GS}$ @ 10V ⑦	43*	A
$I_D$ @ $T_C = 100^{\circ}C$	Continuous Drain Current, $V_{GS}$ @ 10V ⑦	30*	
$I_{DM}$	Pulsed Drain Current ①	180	W
$P_D$ @ $T_A = 25^{\circ}C$	Power Dissipation ⑦	3.8	
$P_D$ @ $T_C = 25^{\circ}C$	Power Dissipation ⑦	300*	$W/^{\circ}C$
	Linear Derating Factor ⑦	2.0*	
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
dv/dt	Peak Diode Recovery dv/dt ③	9.5	V/ns
$T_J$	Operating Junction and	-55 to + 175	$^{\circ}C$
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torque, 6-32 or M3 screw⑥	10 lbf•in (1.1N•m)	

### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.47*	$^{\circ}C/W$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑧	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient⑧	—	62	
$R_{\theta JA}$	Junction-to-Ambient⑦	—	40	

\*  $R_{\theta JC}$  (end of life) for D²Pak and TO-262 = 0.50 $^{\circ}C/W$ . This is the maximum measured value after 1000 temperature cycles from -55 to 150 $^{\circ}C$  and is accounted for by the physical wearout of the die attach medium.

Notes ① through ⑧ are on page 11

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.22	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.054	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 26A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0	—	5.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 200V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -30V

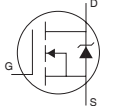
**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	17	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 26A
Q <sub>g</sub>	Total Gate Charge	—	60	91	nC	I <sub>D</sub> = 26A
Q <sub>gs</sub>	Gate-to-Source Charge	—	17	25		V <sub>DS</sub> = 100V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	28	42		V <sub>GS</sub> = 10V, ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	16	—	ns	V <sub>DD</sub> = 100V
t <sub>r</sub>	Rise Time	—	95	—		I <sub>D</sub> = 26A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	29	—		R <sub>G</sub> = 2.5Ω
t <sub>f</sub>	Fall Time	—	47	—		V <sub>GS</sub> = 10V ④
C <sub>iss</sub>	Input Capacitance	—	2900	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	450	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	73	—		f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	3550	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	180	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 160V, f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance	—	380	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 160V ⑤

**Avalanche Characteristics**

	Parameter	Min.	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②⑥	—	—	460	mJ
I <sub>AR</sub>	Avalanche Current ①	—	—	26	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	—	390	—	mJ
V <sub>DS (Avalanche)</sub>	Repetitive Avalanche Voltage ①	260	—	—	V

**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	44	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①⑥	—	—	180		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.5	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 26A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	160	240	nS	T <sub>J</sub> = 25°C, I <sub>F</sub> = 26A
Q <sub>rr</sub>	Reverse Recovery Charge	—	1.3	2.0	μC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

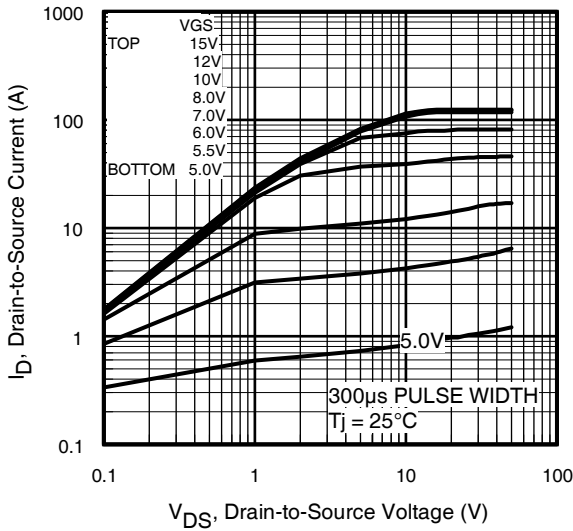


Fig 1. Typical Output Characteristics

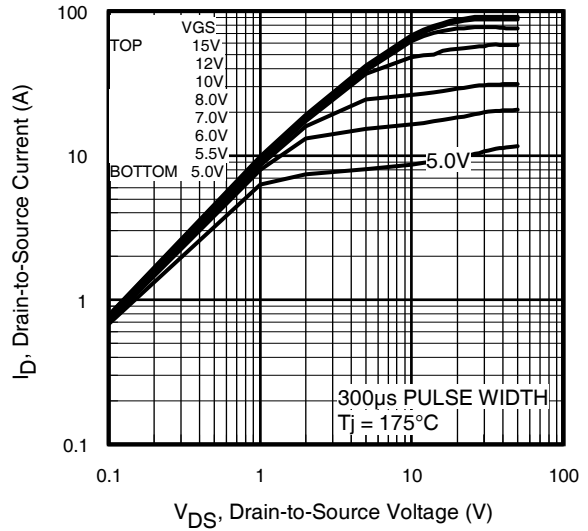


Fig 2. Typical Output Characteristics

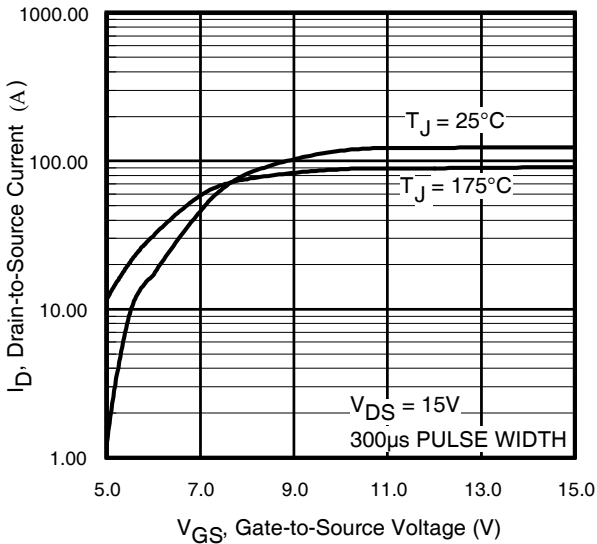


Fig 3. Typical Transfer Characteristics

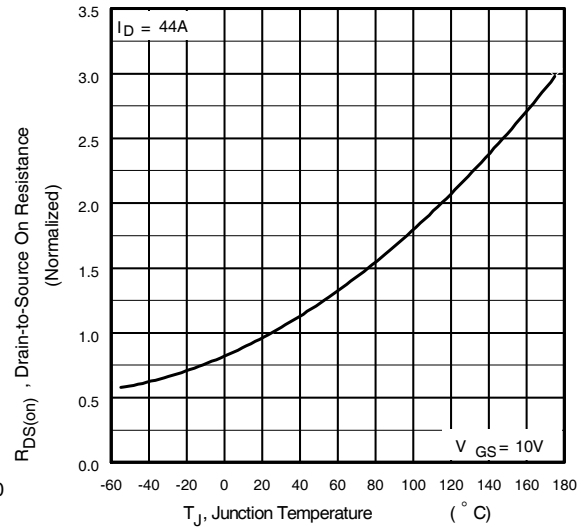
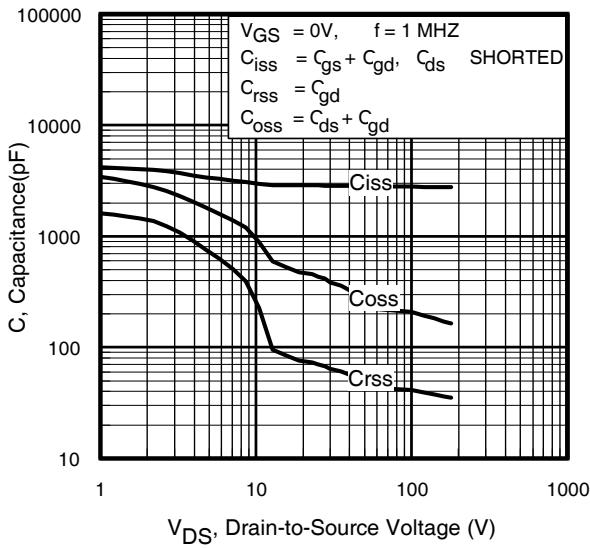
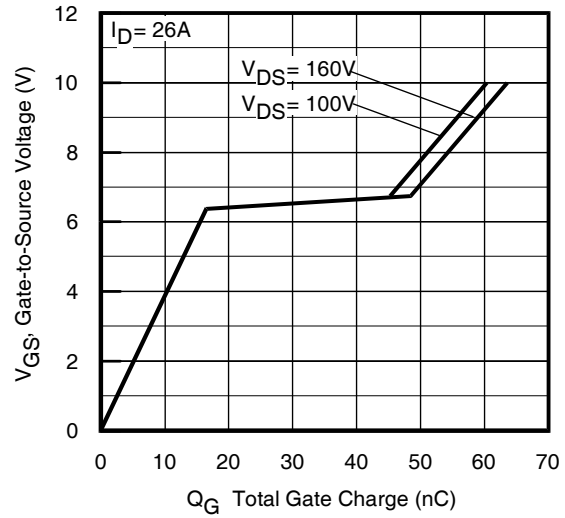


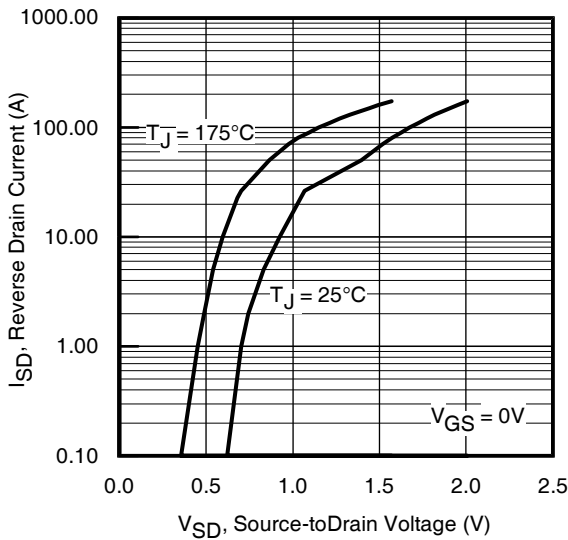
Fig 4. Normalized On-Resistance Vs. Temperature



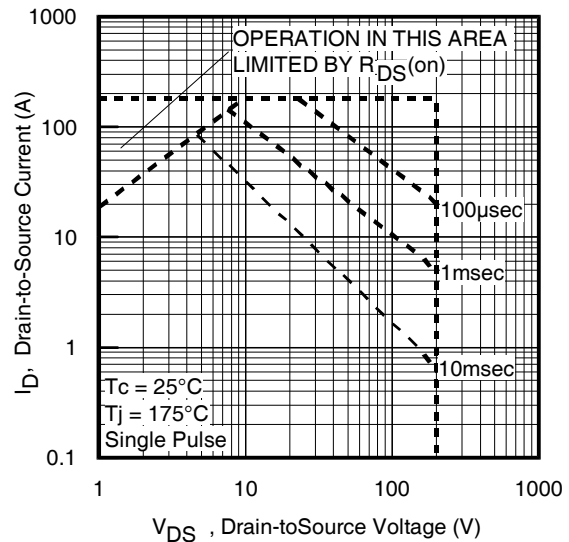
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

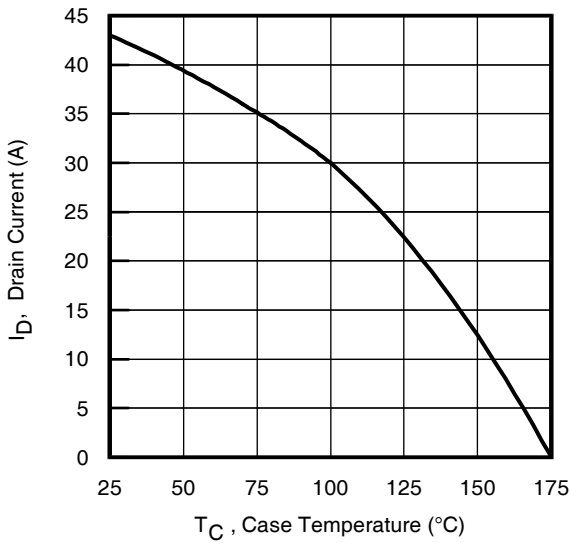


Fig 9. Maximum Drain Current Vs. Case Temperature

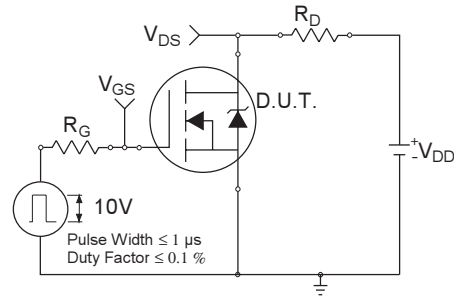


Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

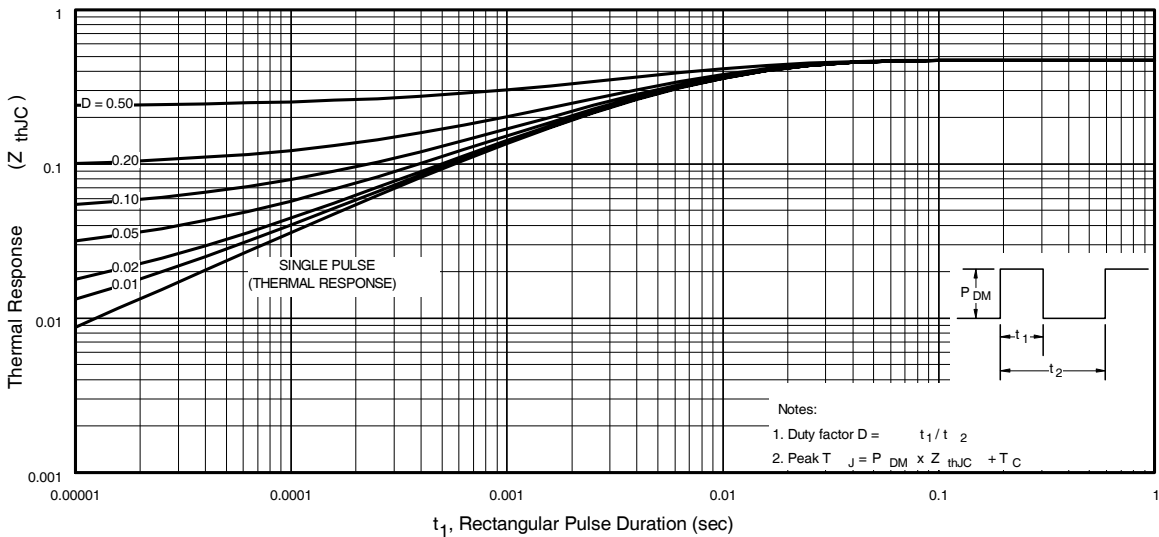


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

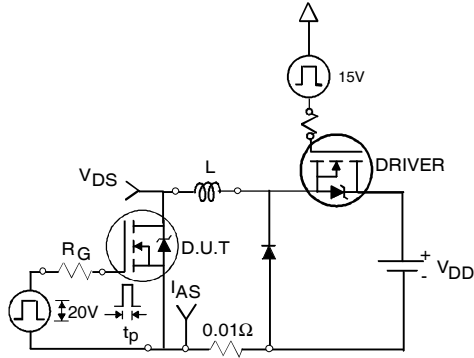


Fig 12a. Unclamped Inductive Test Circuit

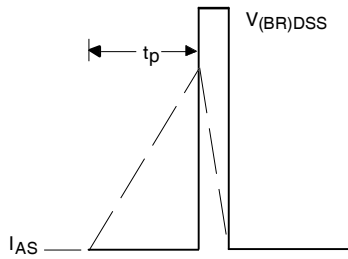


Fig 12b. Unclamped Inductive Waveforms

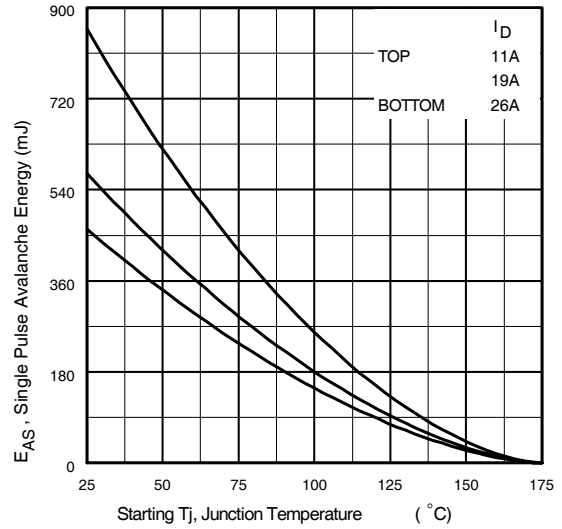


Fig 12c. Maximum Avalanche Energy Vs. Drain Current



Fig 13a. Basic Gate Charge Waveform

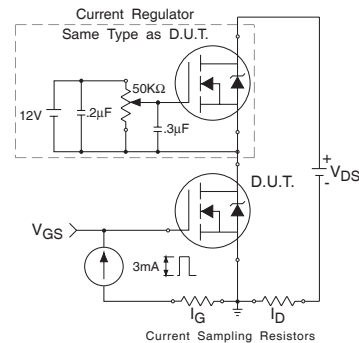
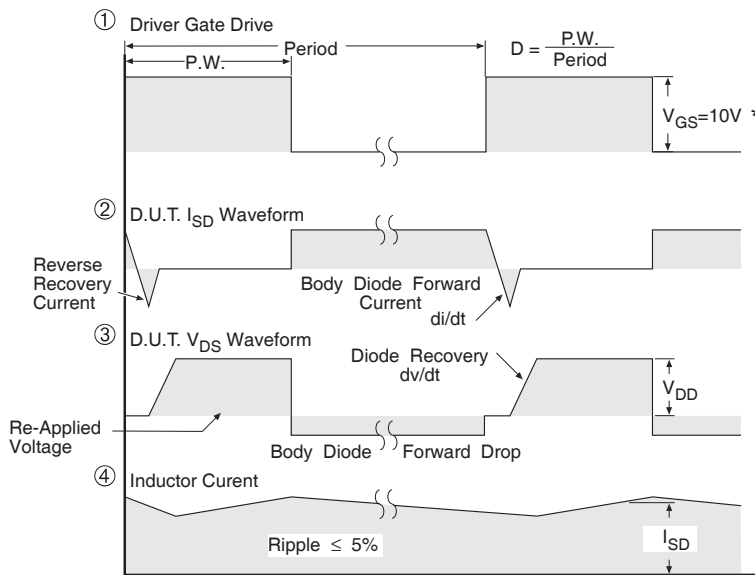


Fig 13b. Gate Charge Test Circuit

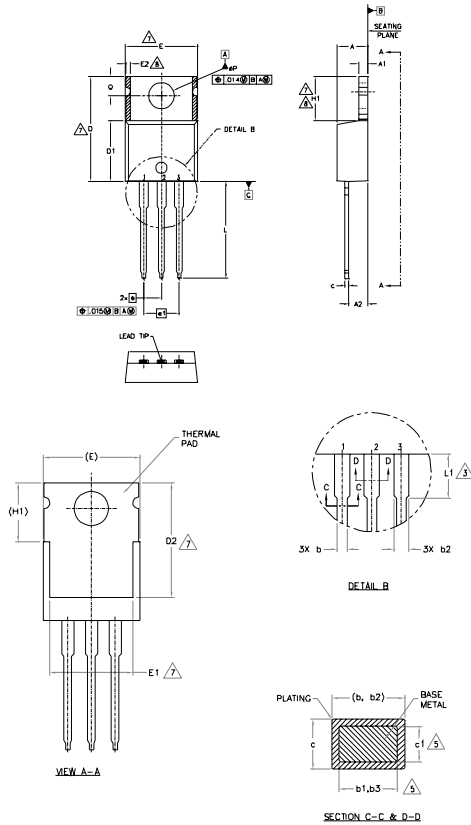
### Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

IRFB/S/SL38N20DPbF  
**TO-220AB Package Outline**  
 Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
  - 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
  - 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
  - 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY. DIMENSION D1, b3 & c1 APPLY TO BASE METAL ONLY.
  - 5.- CONTROLLING DIMENSION . INCHES.
  - 6.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
  - 7.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
  - 8.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

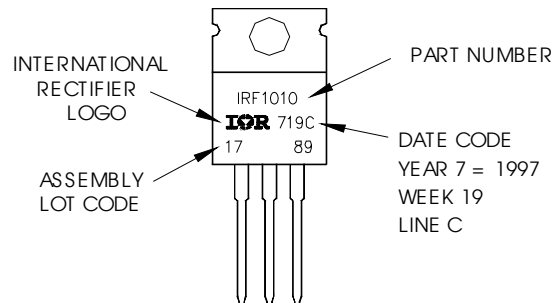
LEAD ASSIGNMENTS

- HERFEL  
 1- GATE  
 2- DRAIN  
 3- SOURCE
- IRFBx COPACK  
 1- GATE  
 2- COLLECTOR  
 3- EMITTER
- ISGSES  
 1- ANODE  
 2- CATHODE  
 3- ANODE

**TO-220AB Part Marking Information**

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

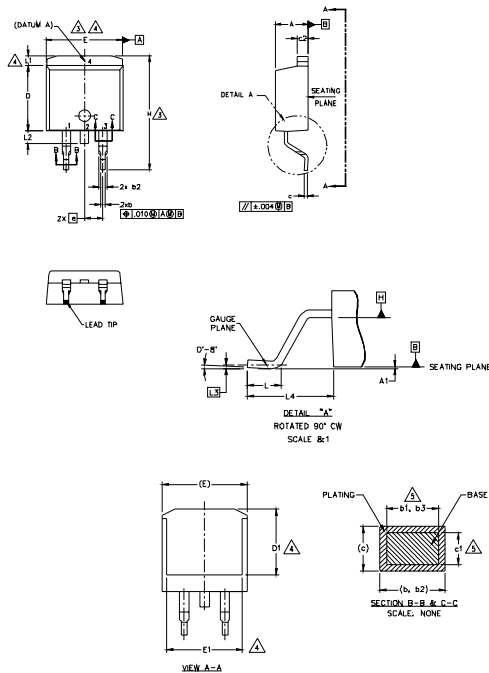
**Notes:**

1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>



## D<sup>2</sup>Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				UNIT
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	5
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.58	0.74	.015	.029	
c1	0.58	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54	BSC	.100	BSC	4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	4
L1	-	1.65	-	.066	
L2	-	1.78	-	.070	4
L3	0.25	BSC	.010	BSC	
L4	4.78	5.28	.188	.208	

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
  4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
  7. CONTROLLING DIMENSION: INCH.
  8. B OUTLINE CONFORMS TO JEDEC OUTLINE 10-263AB.

### LEAD ASSIGNMENTS

#### DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2.- CATHODE
- 3.- ANODE

#### HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

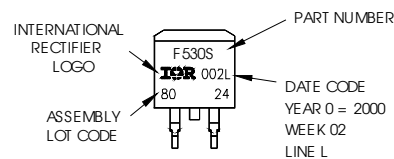
#### IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

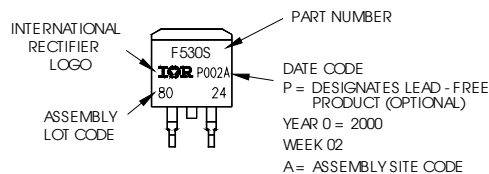
## D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW02, 2000  
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position  
indicates "Lead - Free"



OR



### Notes:

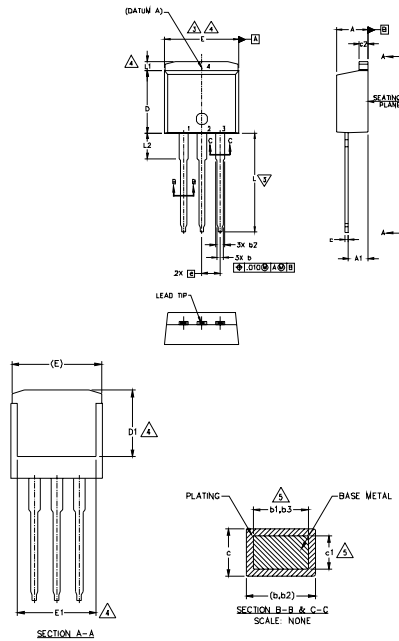
1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

# IRFB/S/SL38N20DPbF



## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

- NOTES:
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  - DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
  - DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  - THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  - DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  - CONTROLLING DIMENSION: INCH.
  - OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(max.), b1(max.) AND D1(max.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

### LEAD ASSIGNMENTS

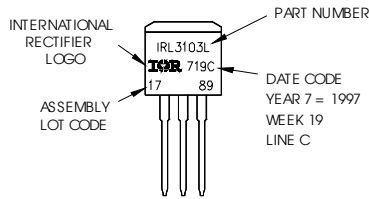
- TO-262 CAP-PAK
- GATE
  - COLLECTOR
  - EMITTER
  - COLLECTOR

- HERFET DIGGES
- GATE
  - DRAIN
  - SOURCE
  - DRAIN
  - NODE (TO DIE) / OPEN (ONE DIE)
  - CATHODE
  - ANODE

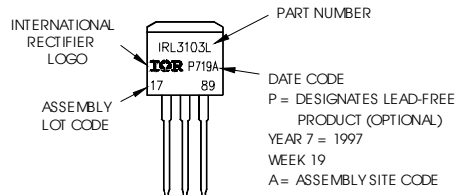
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



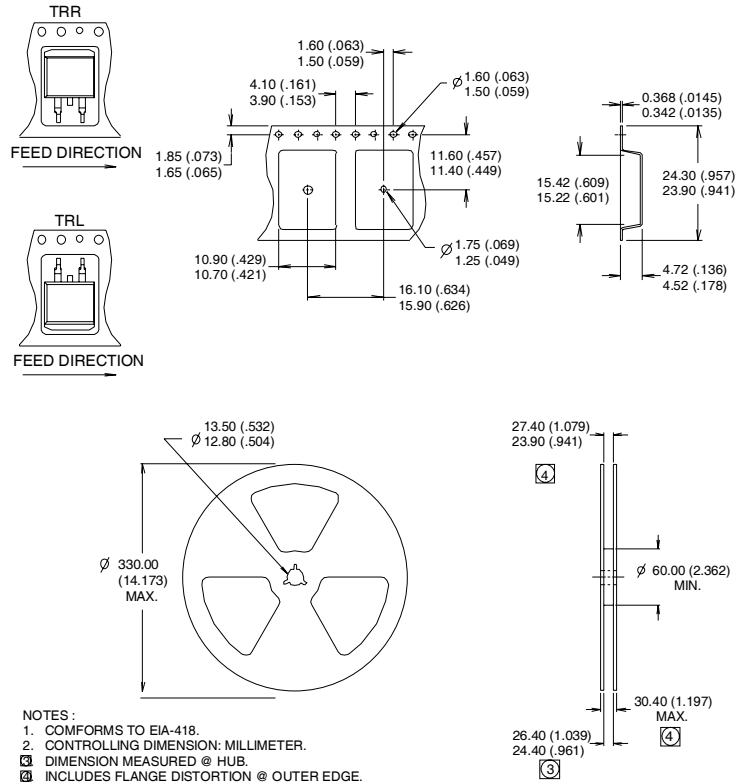
OR



### Notes:

- For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
- For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## D<sup>2</sup>Pak Tape & Reel Information



### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.3\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 26\text{A}$ .
- ③  $I_{SD} \leq 26\text{A}$ ,  $di/dt \leq 390\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥ This is only applied to TO-220AB package.
- ⑦ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Industrial market.  
 Qualification Standards can be found on IR's Web site.