

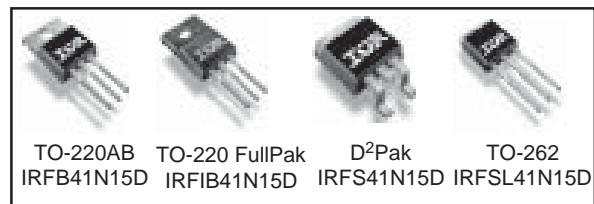
### Applications

- High frequency DC-DC converters

### Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective  $C_{OSS}$  to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

$V_{DSS}$	$R_{DS(on) \max}$	$I_D$
150V	0.045 $\Omega$	41A



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	41	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	29	
$I_{DM}$	Pulsed Drain Current ①	164	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation, D²Pak	3.1	W
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation, TO-220	200	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation, Fullpak	48	
	Linear Derating Factor, TO-220	1.3	W/°C
	Linear Derating Factor, Fullpak	0.32	
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
dv/dt	Peak Diode Recovery dv/dt ③	2.7	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torque, 6-32 or M3 screw	1.1(10)	N•m (lbf•in)

### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta JC}$	Junction-to-Case, Fullpak	—	3.14	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ④	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, TO-220 ⑥	—	62	
$R_{\theta JA}$	Junction-to-Ambient, D²Pak ⑦	—	40	
$R_{\theta JA}$	Junction-to-Ambient, Fullpak	—	65	

Notes ① through ⑦ are on page 12

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# IRFB/IRFIB/IRFS/IRFSL41N15D

International  
IR Rectifier

## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	150	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.17	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.045	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 25A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0	—	5.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 150V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 120V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -30V

## Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)

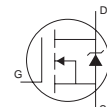
	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	18	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 25A
Q <sub>g</sub>	Total Gate Charge	—	72	110	nC	I <sub>D</sub> = 25A V <sub>DS</sub> = 120V V <sub>GS</sub> = 10V ④
Q <sub>gs</sub>	Gate-to-Source Charge	—	21	31		
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	35	52		
t <sub>d(on)</sub>	Turn-On Delay Time	—	16	—	ns	V <sub>DD</sub> = 75V I <sub>D</sub> = 25A R <sub>G</sub> = 2.5Ω V <sub>GS</sub> = 10V ④
t <sub>r</sub>	Rise Time	—	63	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	25	—		
t <sub>f</sub>	Fall Time	—	14	—		
C <sub>iss</sub>	Input Capacitance	—	2520	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = 120V, f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 120V ⑤
C <sub>oss</sub>	Output Capacitance	—	510	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	110	—		
C <sub>oss</sub>	Output Capacitance	—	3090	—		
C <sub>oss</sub>	Output Capacitance	—	230	—		
C <sub>oss eff.</sub>	Effective Output Capacitance	—	250	—		

## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	470	mJ
I <sub>AR</sub>	Avalanche Current ①	—	25	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	—	20	mJ

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	41	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	164		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 25A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	170	260	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 25A
Q <sub>rr</sub>	Reverse Recovery Charge	—	1.3	1.9	μC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



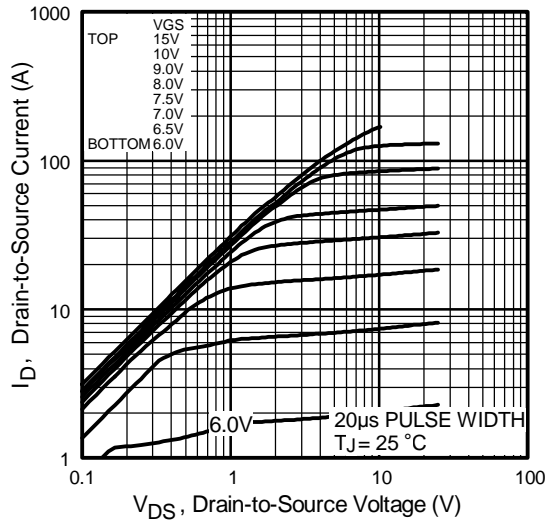


Fig 1. Typical Output Characteristics

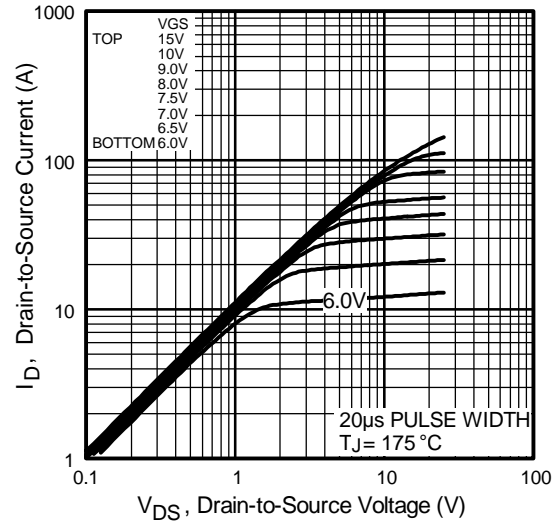


Fig 2. Typical Output Characteristics

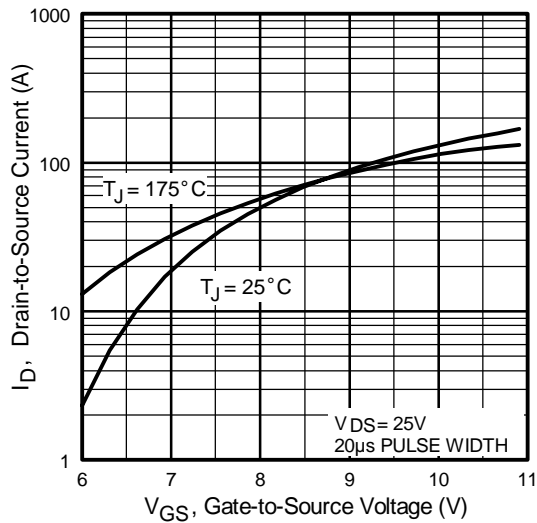


Fig 3. Typical Transfer Characteristics

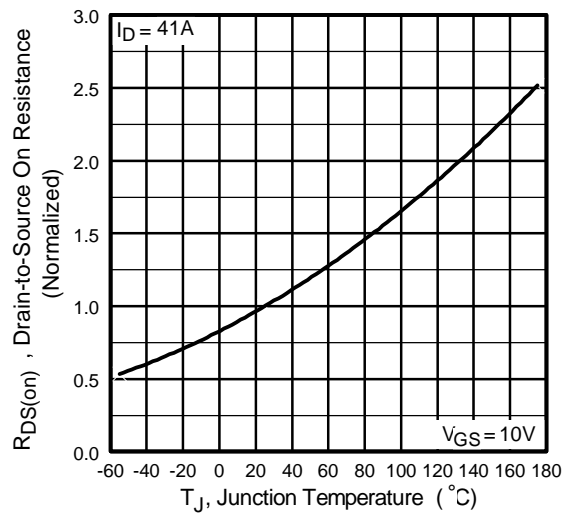
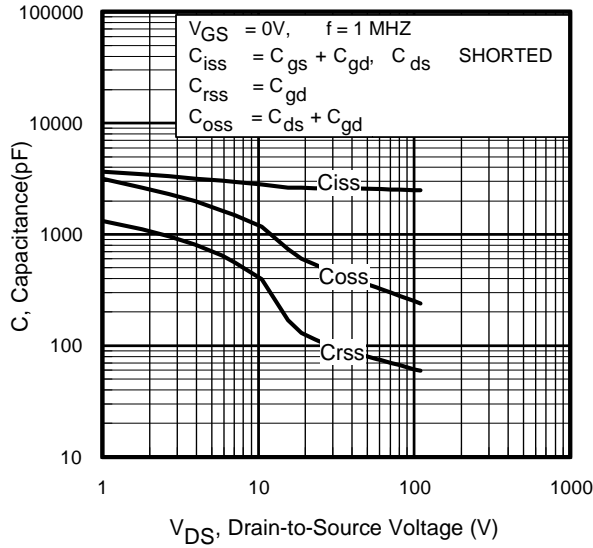
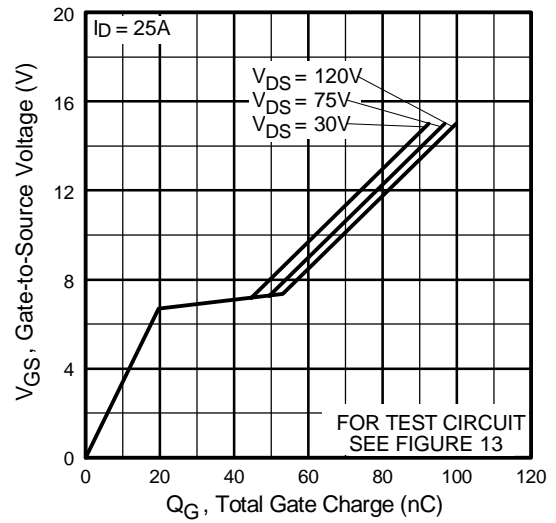


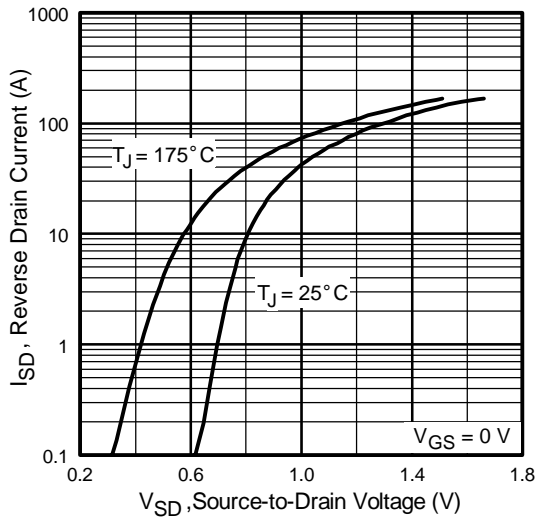
Fig 4. Normalized On-Resistance vs. Temperature



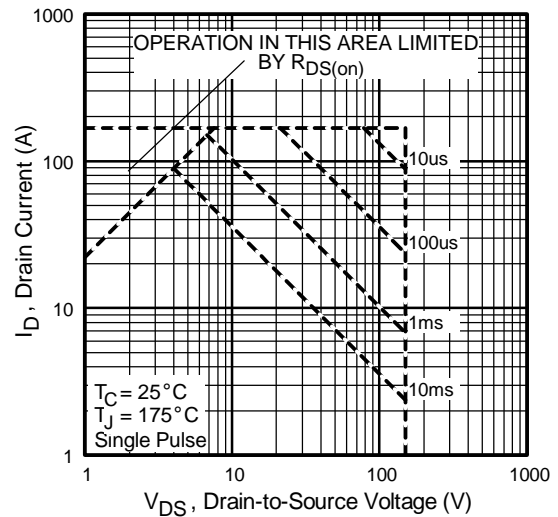
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



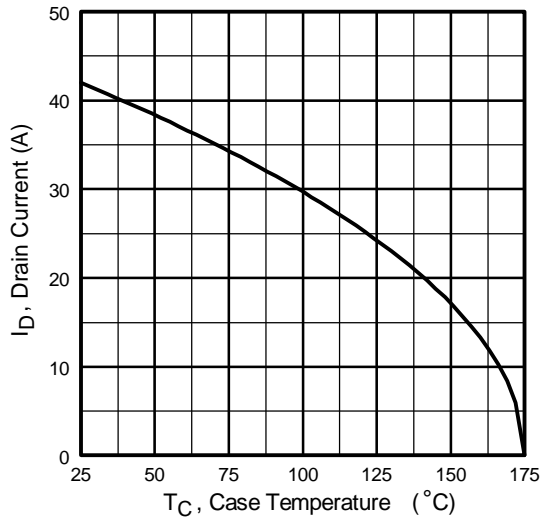
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



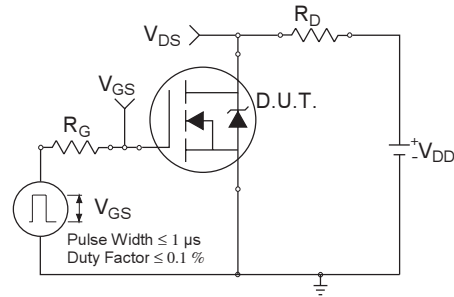
**Fig 7.** Typical Source-Drain Diode Forward Voltage



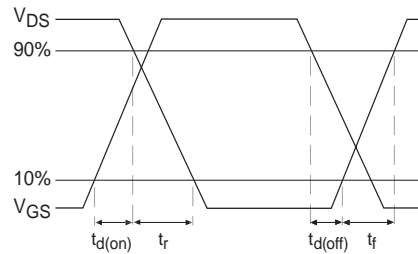
**Fig 8.** Maximum Safe Operating Area



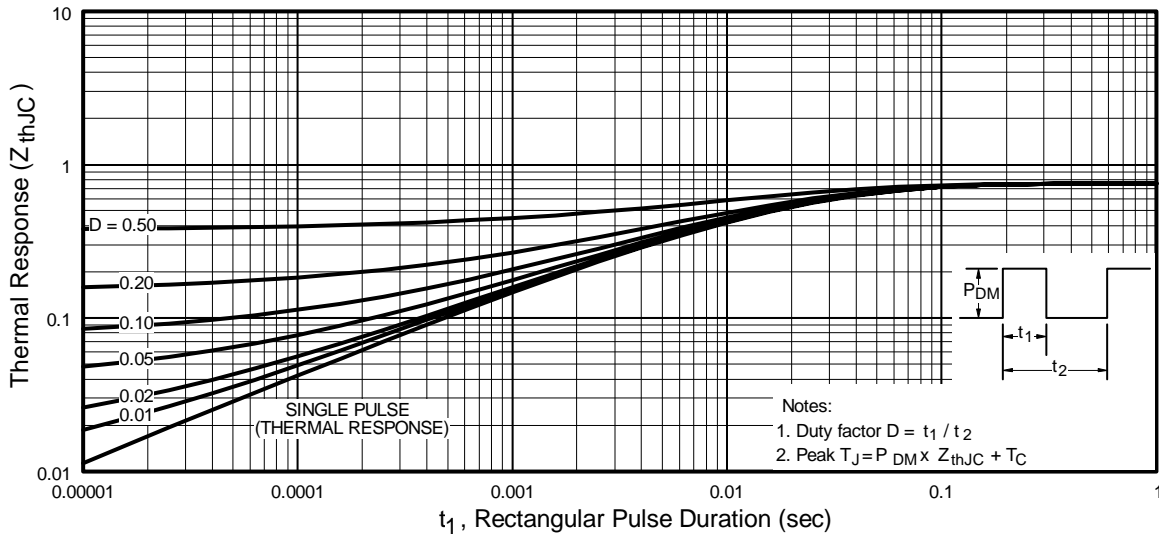
**Fig 9.** Maximum Drain Current Vs. Case Temperature



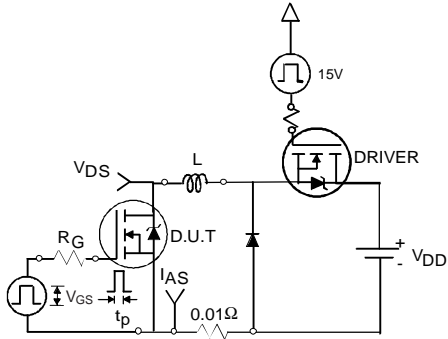
**Fig 10a.** Switching Time Test Circuit



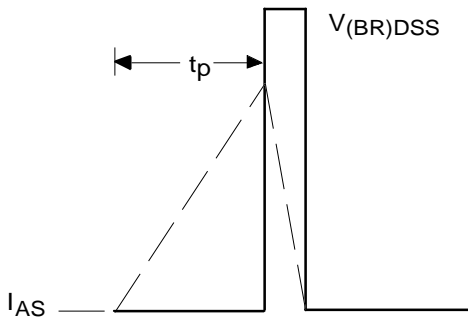
**Fig 10b.** Switching Time Waveforms



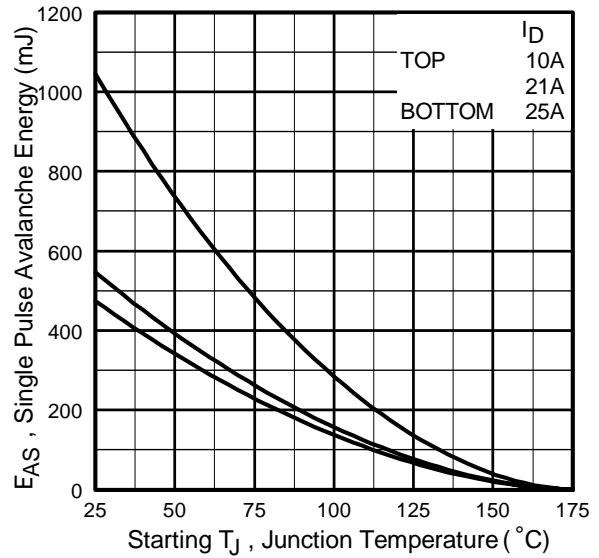
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



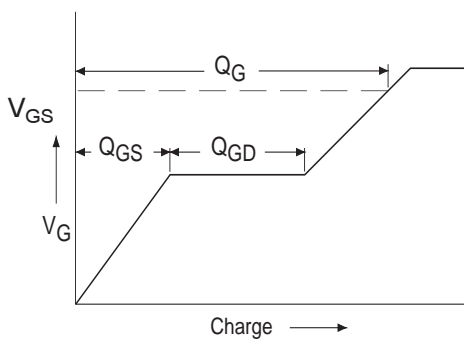
**Fig 12a.** Unclamped Inductive Test Circuit



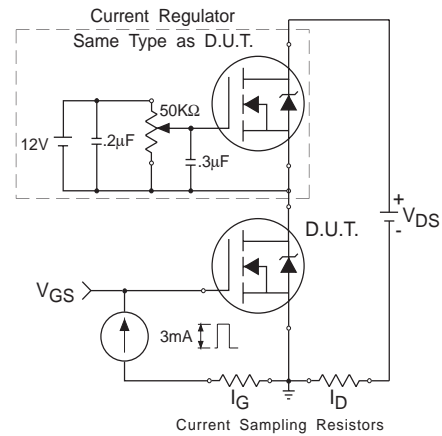
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

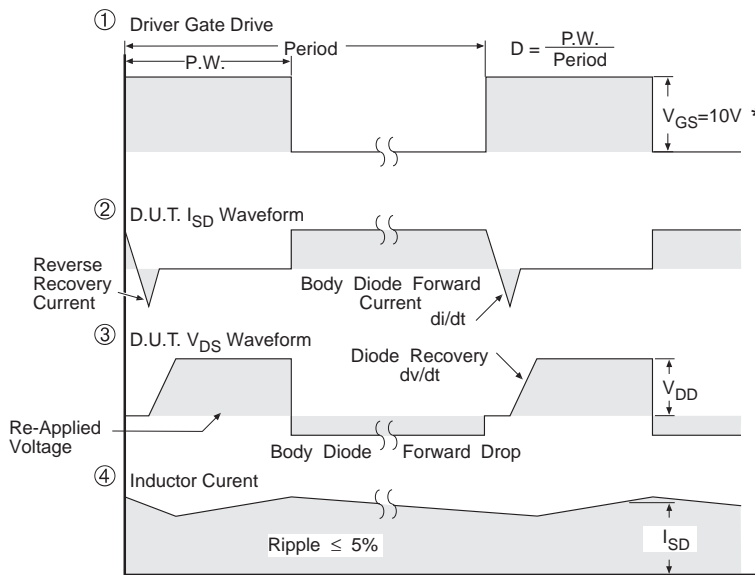
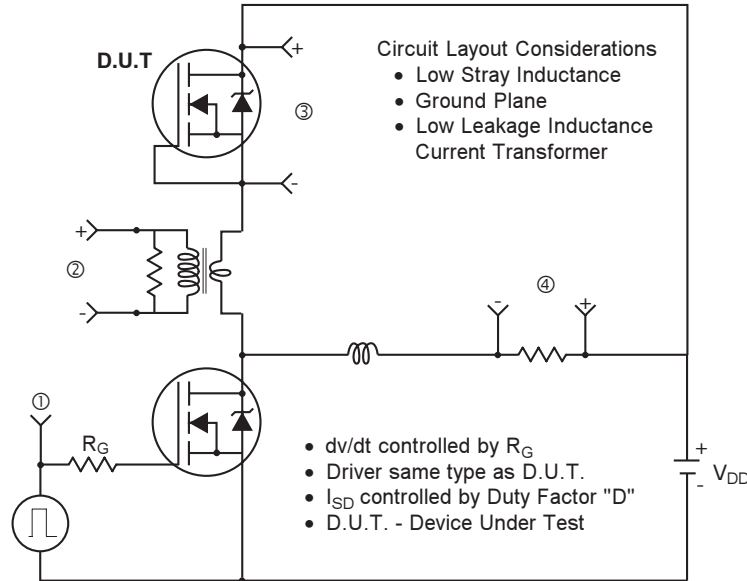


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

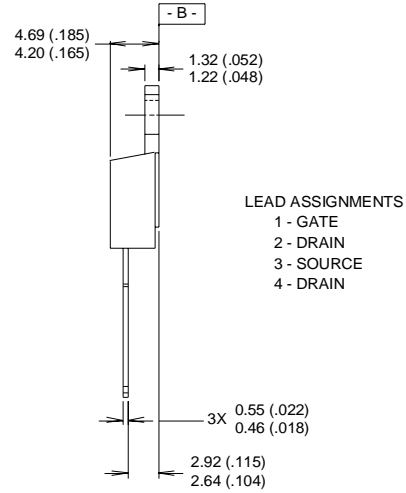
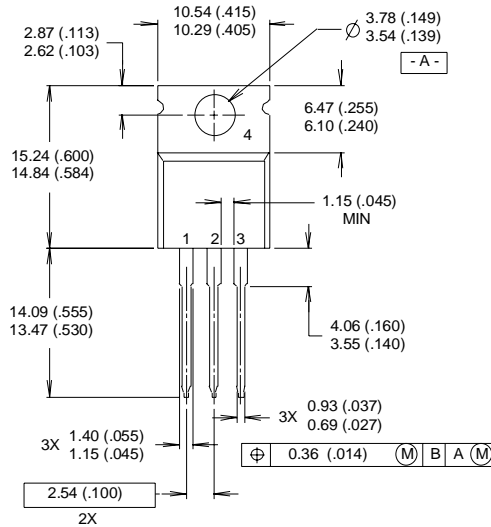
**Fig 14.** For N-Channel HEXFET® Power MOSFETs

# IRFB/IRFIB/IRFS/IRFSL41N15D

International  
**IR** Rectifier

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



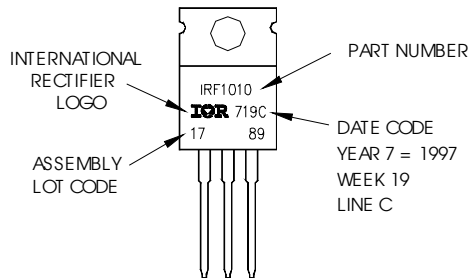
**NOTES:**

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

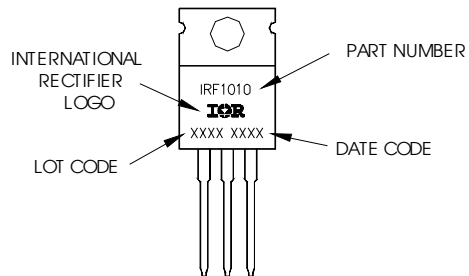
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"



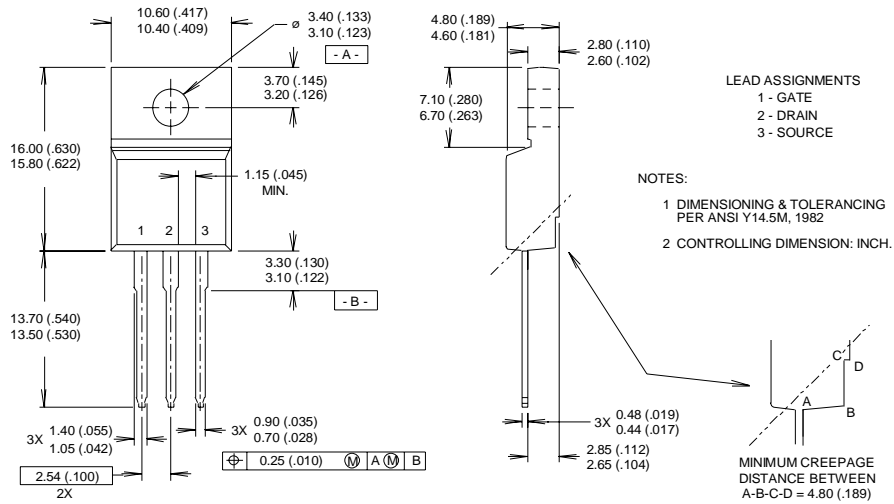
For GB Production  
 EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"





## TO-220 Full-Pak Package Outline

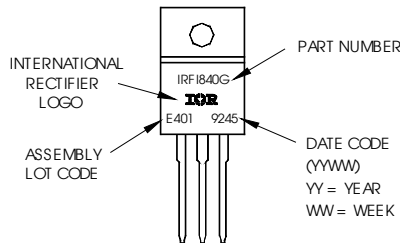
Dimensions are shown in millimeters (inches)



## TO-220 Full-Pak Part Marking Information

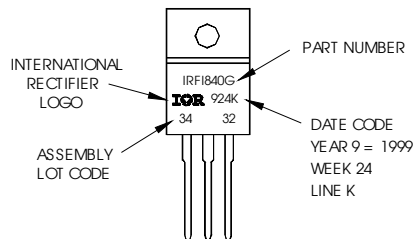
Notes: This part marking information applies to all devices produced before 02/26/2001 and currently for parts manufactured in GB.

EXAMPLE: THIS IS AN IRF1840G  
 WITH ASSEMBLY  
 LOT CODE E401



Notes: This part marking information applies to devices produced after 02/26/2001 in location other than GB.

EXAMPLE: THIS IS AN IRF1840G  
 WITH ASSEMBLY  
 LOT CODE 3432  
 ASSEMBLED ON WW 24 1999  
 IN THE ASSEMBLY LINE "K"

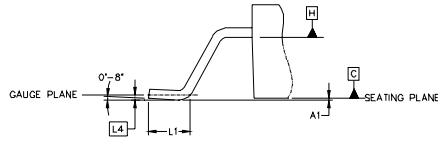


# IRFB/IRFIB/IRFS/IRFSL41N15D

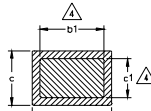
International  
**IR** Rectifier

## D<sup>2</sup>Pak Package Outline

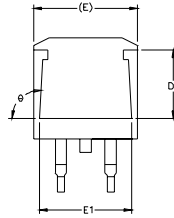
Dimensions are shown in millimeters (inches)



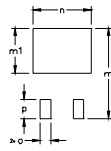
DETAIL "A"  
ROTATED 90°  
SCALE R:1



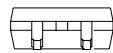
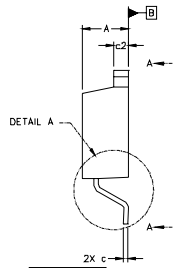
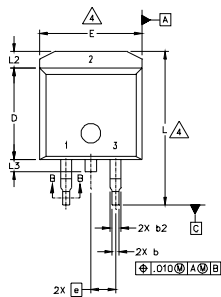
SECTION B-B  
SCALE: NONE



SECTION A-A



FOOT PRINT  
SCALE 2:1



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	4
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2			1.65	.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

### LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

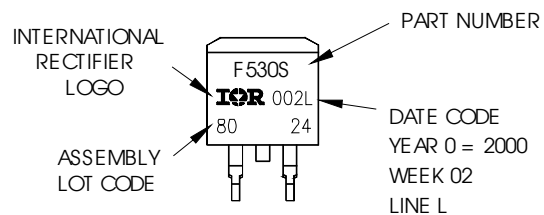
\* PART DEPENDENT.

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

## D<sup>2</sup>Pak Part Marking Information

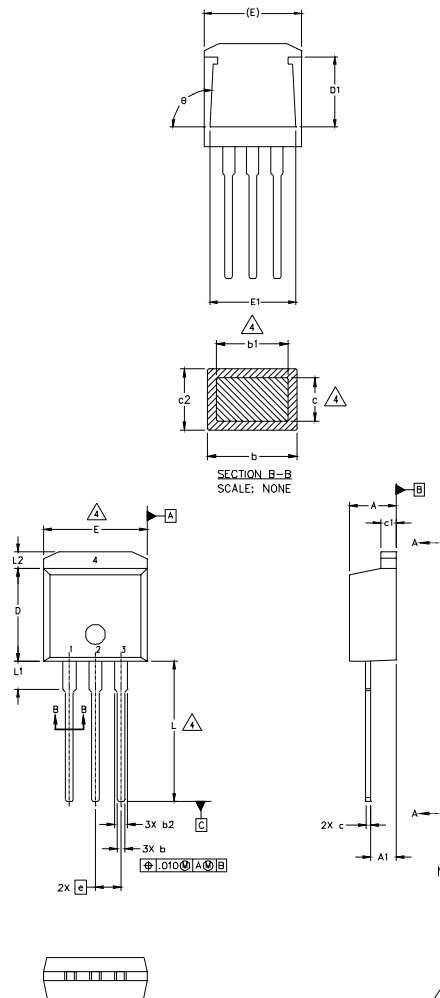
EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW02, 2000  
IN THE ASSEMBLY LINE "L"



# IRFB/IRFIB/IRFS/IRFSL41N15D

## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	4
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

### LEAD ASSIGNMENTS

#### HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

#### IGBT

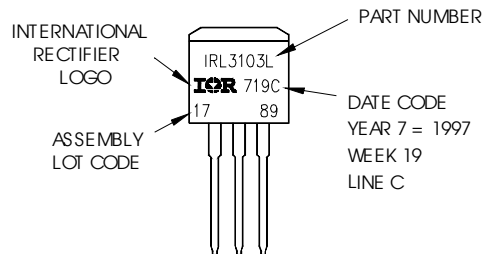
- 1- GATE
- 2- COLLECTOR
- 3- EMITTER

#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

## TO-262 Part Marking Information

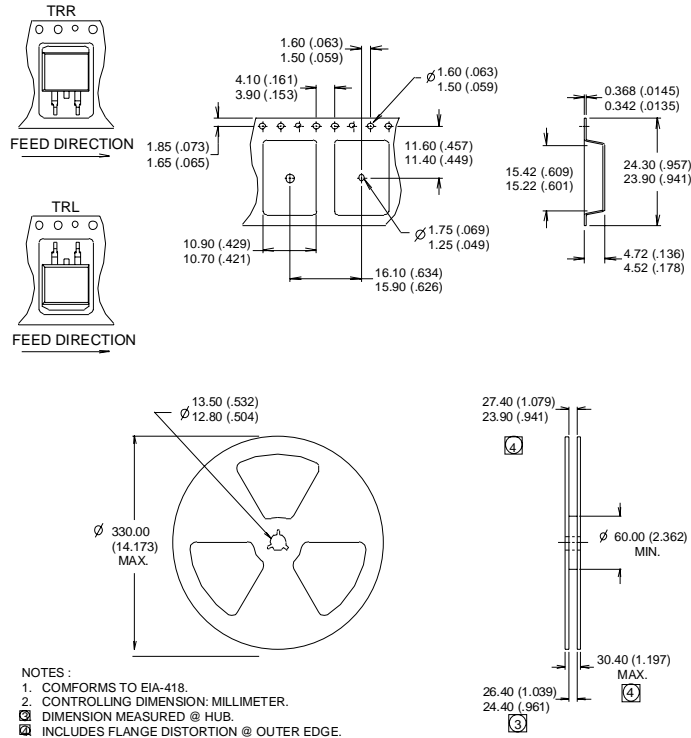
EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"



# IRFB/IRFIB/IRFS/IRFSL41N15D

## D<sup>2</sup>Pak Tape & Reel Information

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### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.5\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 25\text{A}$ .
- ③  $I_{SD} \leq 25\text{A}$ ,  $di/dt \leq 340\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- ⑥ This is only applied to TO-220AB package.
- ⑦ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

**TO-220AB & TO-220 FullPak packages are not recommended for Surface Mount Application.**

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

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