

**HEXFET® POWER MOSFET**

**IRFY240CM**

N-CHANNEL

**200 Volt, 0.18Ω HEXFET**

HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance.

HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required.

The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.

**Product Summary**

Part Number	BV <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
IRFY240CM	200V	0.18Ω	16A

**Features**

- Hermetically Sealed
- Electrically Isolated
- Simple Drive Requirements
- Ease of Paralleling
- Ceramic Eyelets

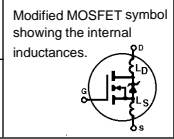
**Absolute Maximum Ratings**

	Parameter	IRFY240CM	Units
I <sub>D</sub> @ V <sub>GS</sub> =10V, T <sub>C</sub> = 25°C	Continuous Drain Current	16	A
I <sub>D</sub> @ V <sub>GS</sub> =10V, T <sub>C</sub> = 100°C	Continuous Drain Current	10.2	
I <sub>DM</sub>	Pulsed Drain Current ①	64	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Max. Power Dissipation	100	W
	Linear Derating Factor	0.8	W/K ⑤
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	580	mJ
I <sub>AR</sub>	Avalanche Current ①	16	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	10	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5	V/ns
T <sub>J</sub>	Operating Junction	-55 to 150	°C
T <sub>stg</sub>	Storage Temperature Range		
	Lead Temperature	300 (0.063 in (1.6mm) from case for 10 sec)	
	Weight	4.3 (typical)	g

# IRFY240CM Device

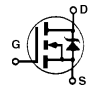
## Electrical Characteristics @ T<sub>J</sub> = 25°C (Unless Otherwise Specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions	
BV <sub>DSS</sub>	200	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA	
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	—	0.29	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA	
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	0.18	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 10.2A ④
		—	—	0.25		V <sub>GS</sub> = 10V, I <sub>D</sub> = 16A
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	6.1	—	—	S (S)	V <sub>DS</sub> ≥ 15V, I <sub>DS</sub> = 10.2A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	25	μA	V <sub>DS</sub> = 0.8 x max. rating, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 0.8 x max. rating V <sub>GS</sub> = 0V, T <sub>J</sub> = 25°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	—	-100	nA	V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	32	—	60	nC	V <sub>GS</sub> = 10V, I <sub>D</sub> = 16A
Q <sub>gs</sub>	Gate-to-Source Charge	2.2	—	10.6		V <sub>DS</sub> = Max. Rating x 0.5
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	14.2	—	37.6		see figures 6 and 13
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	20	ns	V <sub>DD</sub> = 100V, I <sub>D</sub> = 16A, R <sub>G</sub> = 9.1Ω V <sub>GS</sub> = 10V  see figure 10
t <sub>r</sub>	Rise Time	—	—	152		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	58		
t <sub>f</sub>	Fall Time	—	—	67		
L <sub>D</sub>	Internal Drain Inductance	—	8.7	—		
L <sub>S</sub>	Internal Source Inductance	—	8.7	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.  Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C <sub>iss</sub>	Input Capacitance	—	1300	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V f = 1.0MHz. see figure 5
C <sub>oss</sub>	Output Capacitance	—	400	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	130	—		



## Source-Drain Diode Ratings and Characteristics

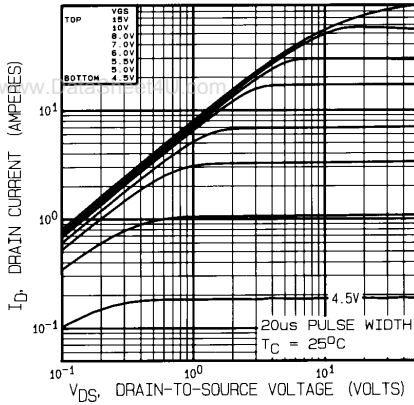
Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	—	—	16	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier.
I <sub>SM</sub>	—	—	64		
V <sub>SD</sub>	—	—	1.5	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 16A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	—	—	500	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 16A, di/dt ≤ 100 A/μs
Q <sub>RR</sub>	—	—	5.3	μC	V <sub>DD</sub> ≤ 50 V ④
t <sub>on</sub>	Forward Turn-On Time Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .				



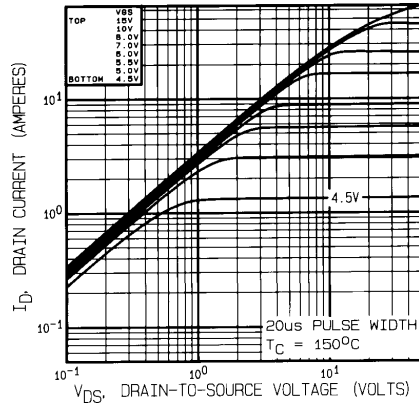
## Thermal Resistance

Parameter	Min.	Typ.	Max.	Units	Test Conditions
R <sub>thJC</sub>	—	—	1.25	KW ⑤	Typical socket mount Mounting surface flat, smooth
R <sub>thJA</sub>	—	—	80		
R <sub>thCS</sub>	—	0.21	—		

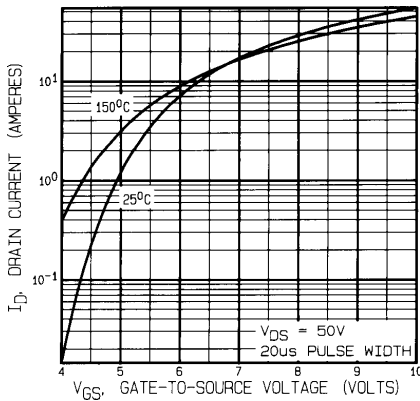
# IRFY240CM Device



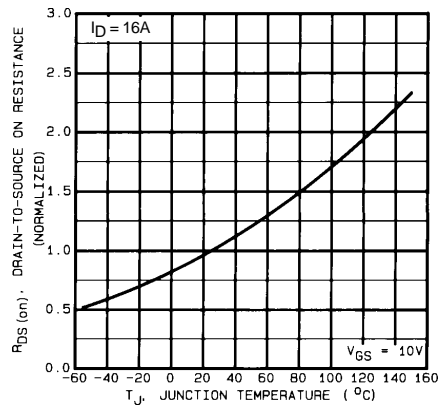
**Fig. 1 — Typical Output Characteristics**  
 $T_C = 25^\circ\text{C}$



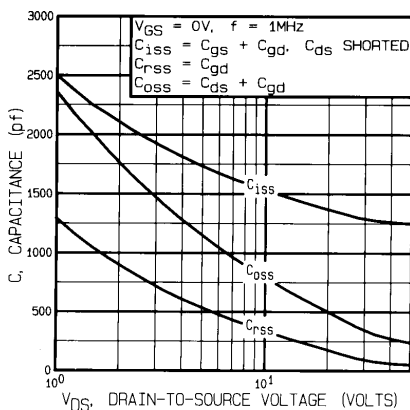
**Fig. 2 — Typical Output Characteristics**  
 $T_C = 150^\circ\text{C}$



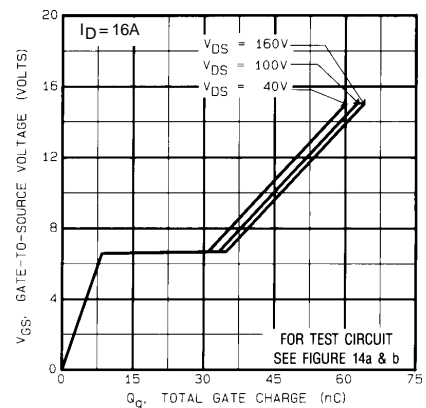
**Fig. 3 — Typical Transfer Characteristics**



**Fig. 4 — Normalized On-Resistance Vs. Temperature**

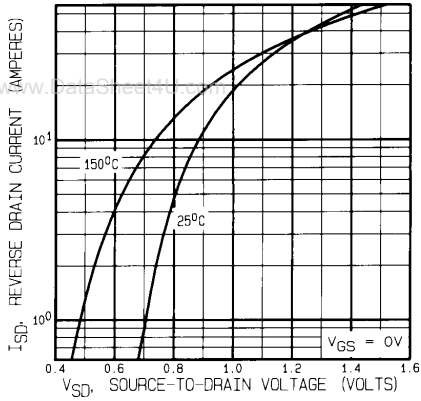


**Fig. 5 — Typical Capacitance Vs. Drain-to-Source Voltage**

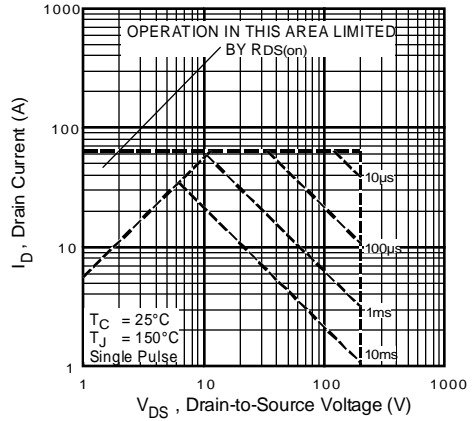


**Fig. 6 — Typical Gate Charge Vs. Gate-to-Source Voltage**

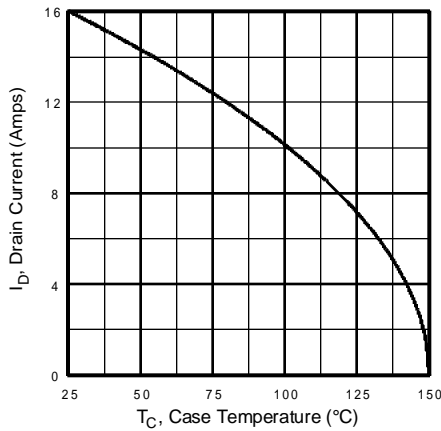
# IRFY240CM Device



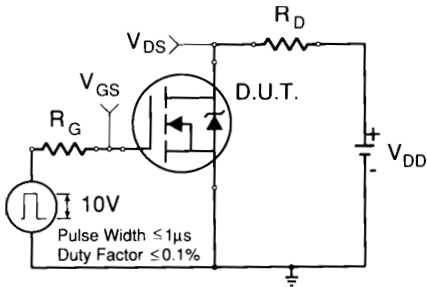
**Fig. 7 — Typical Source-to-Drain Diode Forward Voltage**



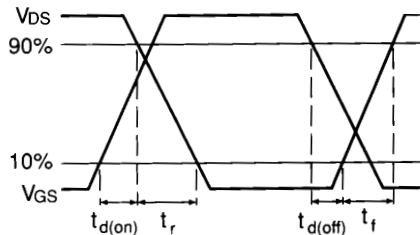
**Fig. 8 — Maximum Safe Operating Area**



**Fig. 9 — Maximum Drain Current Vs. Case Temperature**



**Fig. 10a — Switching Time Test Circuit**



**Fig. 10b — Switching Time Waveforms**

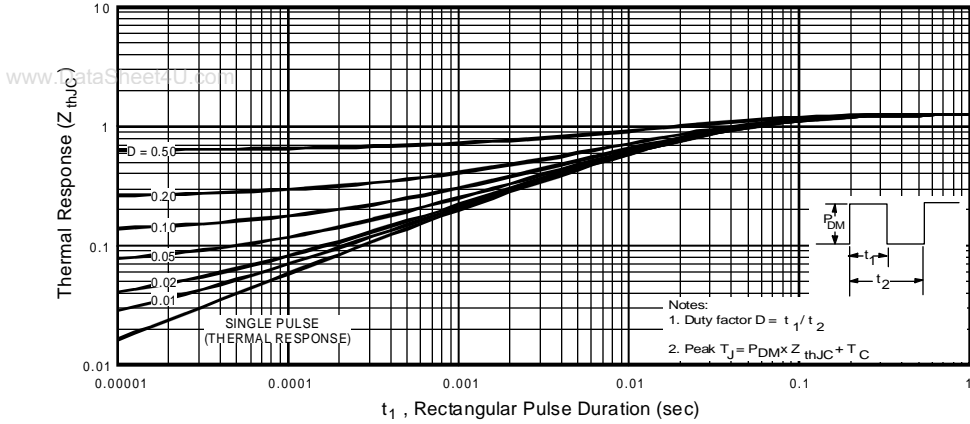


Fig. 11 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

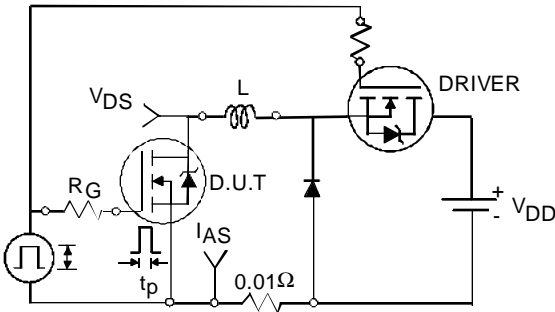


Fig. 12a — Unclamped Inductive Test Circuit

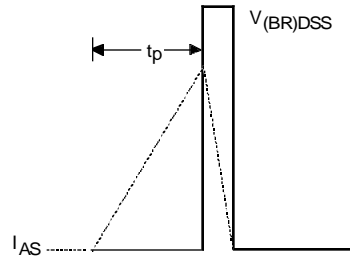


Fig. 12b — Unclamped Inductive Waveforms

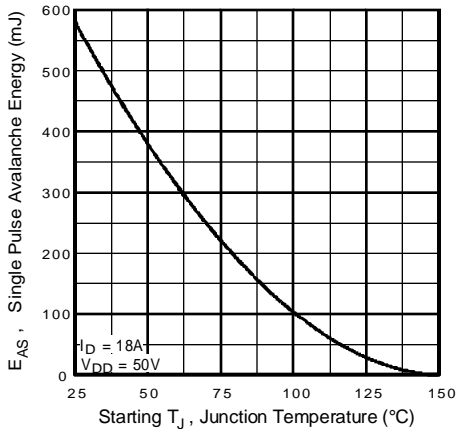


Fig. 12c — Max. Avalanche Energy vs. Current

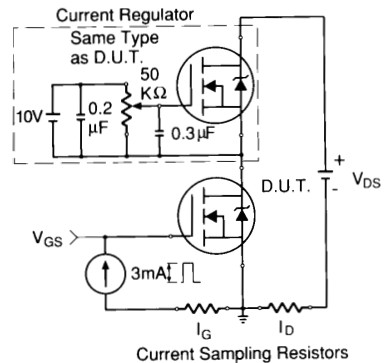


Fig. 13a — Gate Charge Test Circuit

# IRFY240CM Device

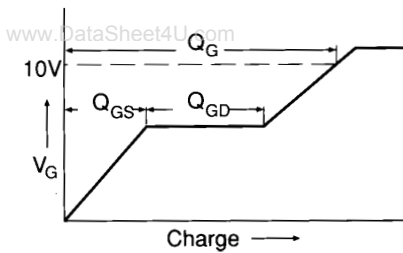
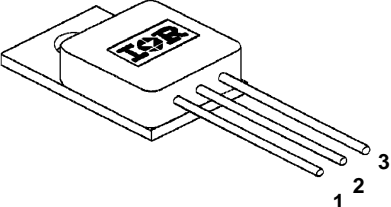
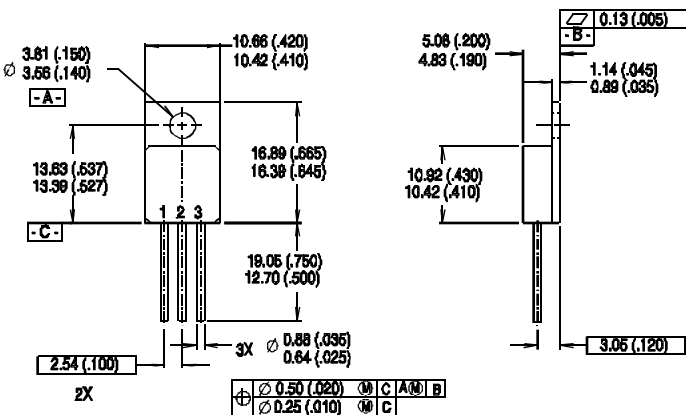


Fig. 13b — Basic Gate Charge Waveform

### Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 11).
- ② @  $V_{DD} = 50V$ , Starting  $T_J = 25^\circ C$ ,  
 $E_{AS} = [0.5 * L * (I_L^2) * [BV_{DSS}/(BV_{DSS}-V_{DD})]]$   
 Peak  $I_L = 16A$ ,  $V_{GS} = 10V$ ,  $25 \leq R_G \leq 200\Omega$  (figure 12)
- ③  $I_{SD} \leq 16A$ ,  $di/dt \leq 150A/\mu s$ ,  $V_{DD} \leq BV_{DSS}$ ,  $T_J \leq 150^\circ C$
- ④ Pulse width  $\leq 300 \mu s$ ; Duty Cycle  $\leq 2\%$
- ⑤  $K/W = ^\circ C/W$        $W/K = W/^\circ C$

## Case Outline and Dimensions — TO-257AA

<p>Pin 1 - Drain Pin 2 - Source Pin 3 - Gate</p>  <p style="text-align: center;"><b>TO-257AA</b></p>	 <p style="text-align: center;"><b>NON-STANDARD PIN CONFIGURATION</b></p> <p style="text-align: center;">Pin 1 - Gate Pin 2 - Drain Pin 3 - Source</p> <p style="text-align: center;"><b>Order Part Type IRFY240C</b></p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>1. Dimensioning and tolerancing per ANSI Y14.5M-1982</li> <li>2. Controlling dimension: Inch</li> <li>3. Dimensions are shown in millimeters (Inches)</li> <li>4. Outline conforms to JEDEC outline TO-257AA</li> </ol>
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**CAUTION**

**BERYLLIA WARNING PER MIL-PRF-19500**

Packages containing beryllia shall not be ground, sandblasted, machined or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

# International **IR** Rectifier

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