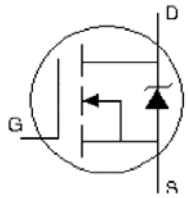
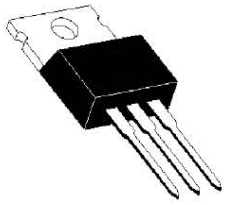
IRFZ34N
HEXFET® Power MOSFET

Advanced Process Technology
Dynamic dv/dt Rating
175°C Operating Temperature
Fast Switching
Fully Avalanche Rated



V_{DSS}=55V
$R_{DS(on)}$=0.040Ω
I_D=26A



TO-220AB

Description

Fifth Generation HEXFETs from international Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

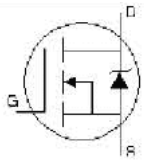
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ Tc=25°C	Continuous Drain Current, V_{GS} @ 10V	26	A
I_D @ Tc=100°C	Continuous Drain Current, V_{GS} @ 10V	18	
I_{DM}	Pulsed Drain Current ①	100	
P_D @ Tc=25°C	Power Dissipation	56	W
	Linear Derating Fastor	0.37	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	110	mJ
I_{AR}	Avalanche Current ①	16	A
E_{AR}	Repetitive Avalanche Energy ①	5.6	mJ
Dv/dt	Peak Diode Recovery dv/dt ③	4.6	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

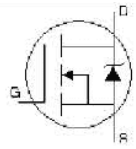
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\Theta JC}$	Junction-to-Case	-	-	2.7	°C/W
$R_{\Theta CS}$	Case-to-Sink,	-	0.50	-	
$R_{\Theta JA}$	Junction-to-Ambient	-	-	62	

Electrical Characteristics @ TJ=25℃ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	-	-	V	V_{GS}=0V, I_D=250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	-	0.052	-	V/°C	Reference to 25°C, I_D=1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	-	-	0.040	Ω	V_{GS}=10V, I_D=16A④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	-	4.0	V	V_{DS}=V_{GS},I_D=250μA
gfs	Forward Transconductance	6.5	-	-	s	V_{DS}=25V, I_D=16A
I_{DSS}	Drain-to-Source Leakage Current	-	-	25	μA	V_{DS}=55V, V_{GS}=0V
		-	-	250		V_{DS}=44V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-Source Forward Leakage	-	-	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	-	-	-100		V_{GS}=-20V
Qg	Total Gate Charge	-	-	34	nC	I_D=16A
Qgs	Gate-to-Source Charge	-	-	6.8		V_{DS}=44V
Qgd	Gate-to-Drain (“Miller”) Charge	-	-	14		V_{GS}=10V, See Fig. 6 and 13④
$t_{d(on)}$	Turn-On Delay Time	-	7.0	-	ns	V_{DD}=28V
tr	Rise Time	-	49	-		I_D=16A
td(off)	Turn-Off Delay Time	-	31	-		R_G=18Ω
tf	Fall Time	-	40	-		R_D=1.8Ω, See Fig. 10④
LD	Internal Drain Inductance	-	4.5	-	nH	Between lead, 6mm (0.25in.) From package and center of die contact 
LS	Internal source inductance	-	7.5	-		
Ciss	Input Capacitance	-	700	-	pF	V_{GS}=0v
Coss	Output Capacitance	-	240	-		V_{DS}=25V
Crss	Reverse Transfer Capacitance	-	100	-		F=1.0MHz, See Fig.5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
Is	Continuous Source Current (Body Diode)	-	-	26	A	MOSFET symbol Showing the integral reverse p-n junction diode. 
I_{SM}	Diode Forward Voltage	-	-	100		
V_{SD}	Reverse Recovery Time	-	-	1.6	V	T_J=25°C, I_S=16A, V_{GS}=0V ④
trr	Reverse Recovery Charge	-	57	86	ns	T_J=25°C, I_F=16A
Qrr	Reverse Recovery Charge	-	130	200	nC	ti/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L s+L_D)				

Notes:

①Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD}=25V, starting T_J=25°C, L=610μH, R_G=25Ω, I_{AS}=16A. (See Figure 12)

③ I_{SD}≤16A, di/dt ≤ 420A/μs, V_{DD}≤$V_{(BR)DSS}$, T_J≤175°C.

④ Pulse width ≤300μs; duty cycle μs2%.

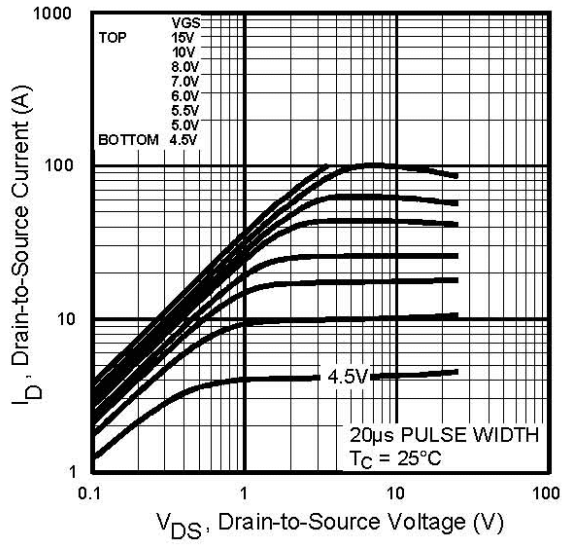


Fig 1. Typical Output Characteristics, Tc=25°C

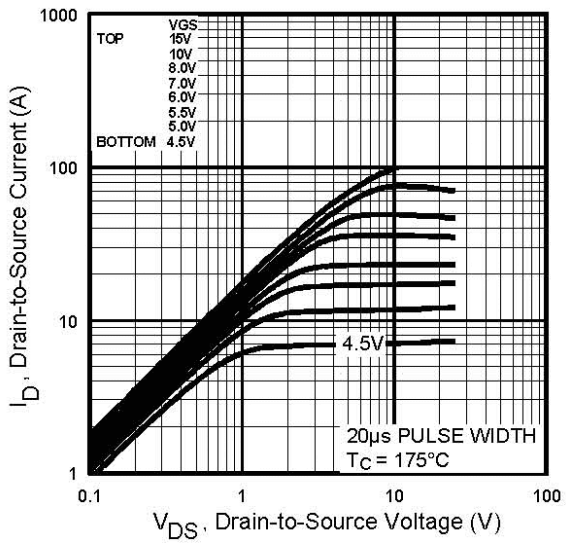


Fig 2. Typical Output Characteristics, Tc =175°C

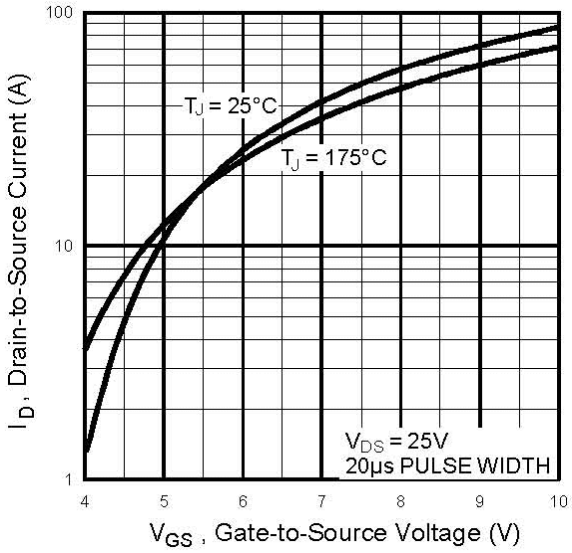


Fig 3. Typical Transfer Characteristics

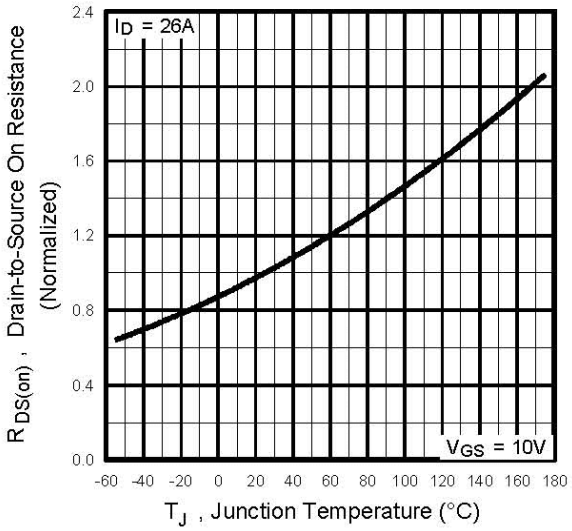


Fig 4. Normalized On-Resistance Vs. Temperature

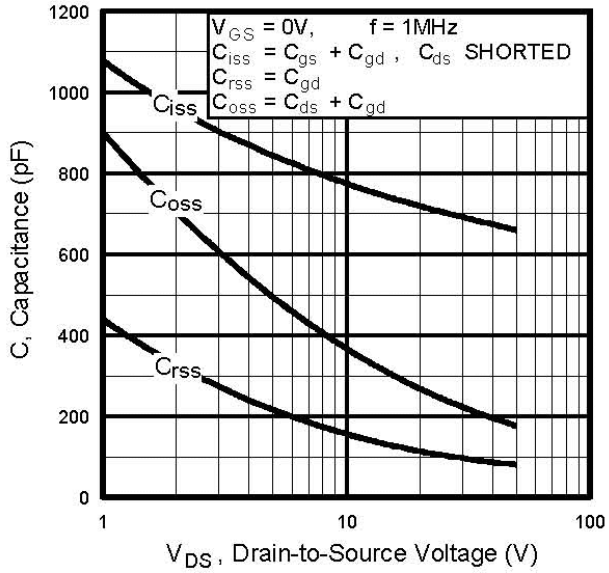


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

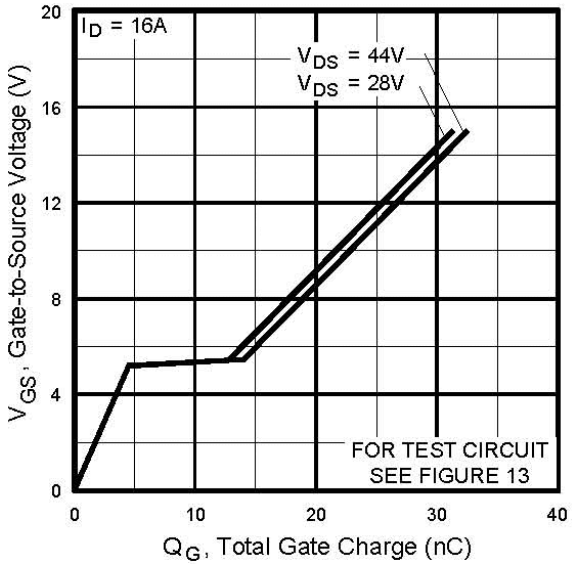


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

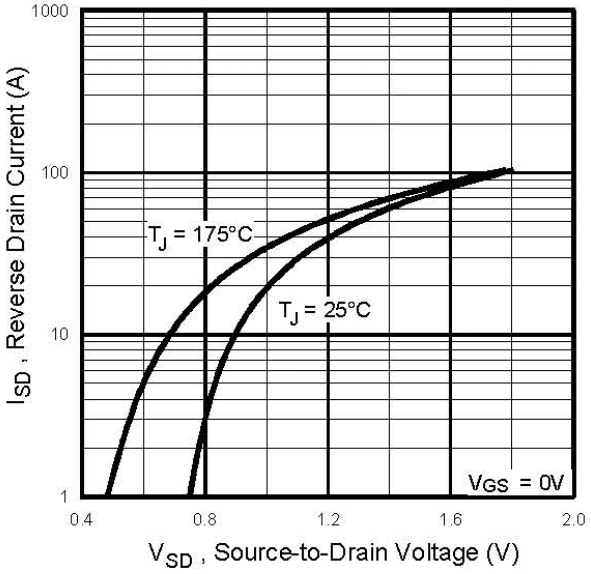


Fig 7. Typical Source-Drain Diode Forward Voltage

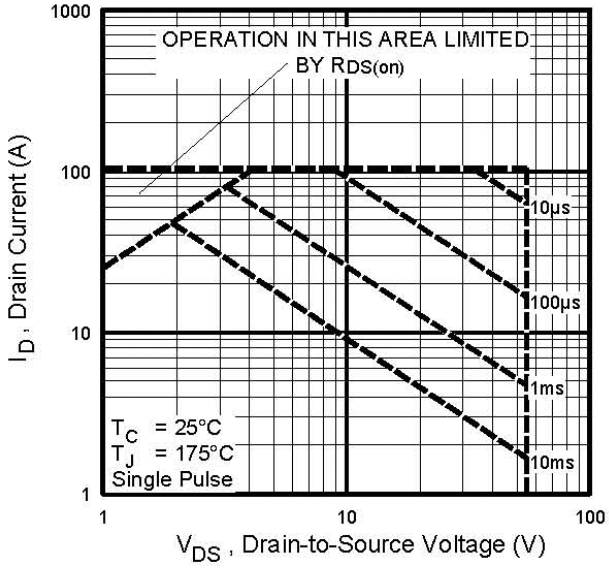


Fig 8. Maximum Safe Operating Area

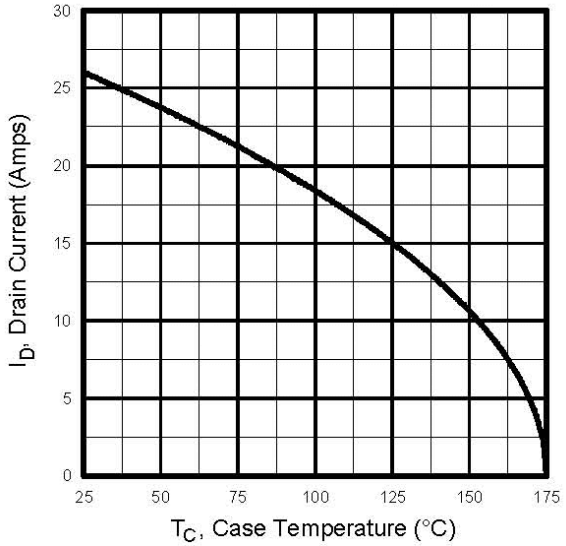


Fig 9. Maximum Drain Current Vs. Case Temperature

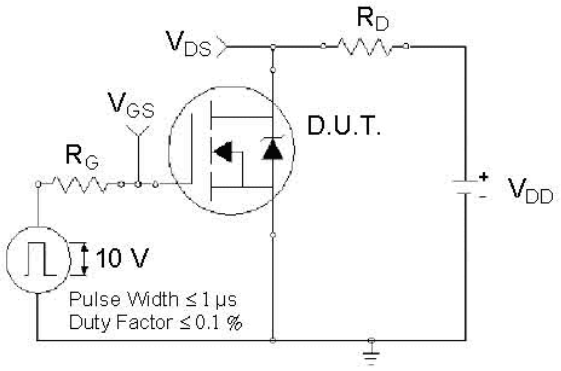


Fig 10a. Switching Time Test Circuit

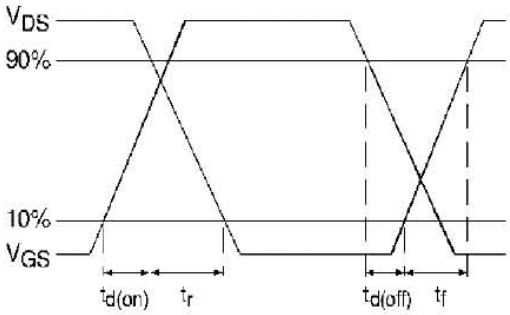


Fig 10b. Switching Time Waveforms

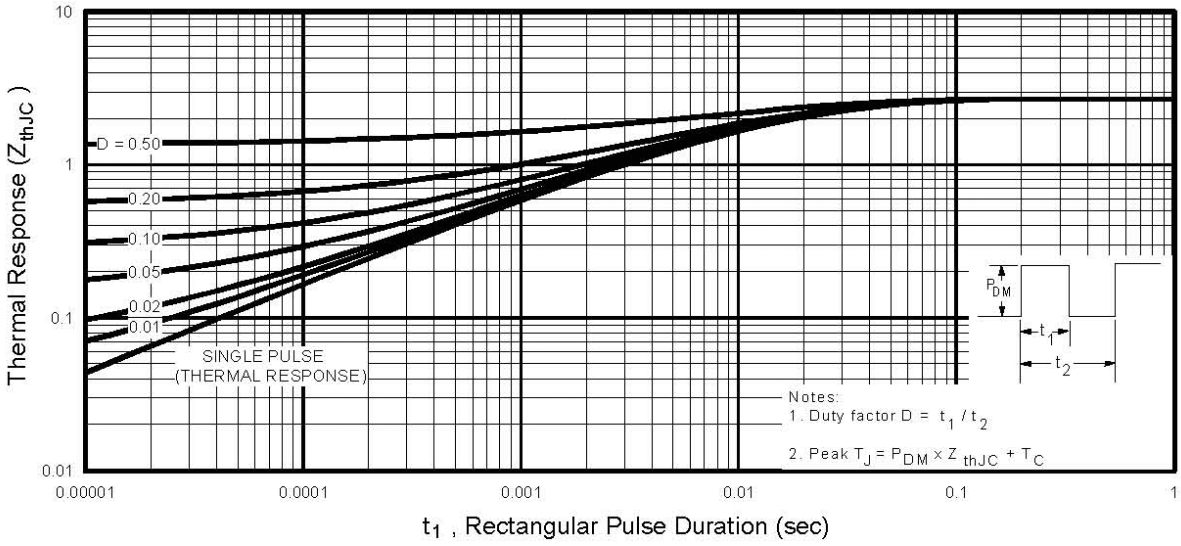


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

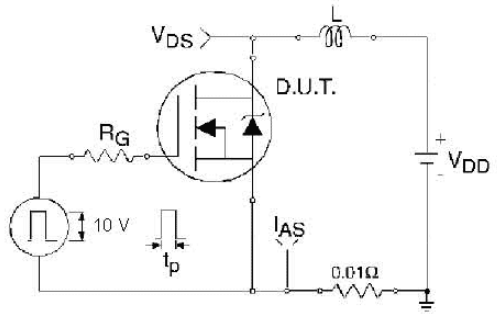


Fig 12a. Unclamped Inductive Test Circuit

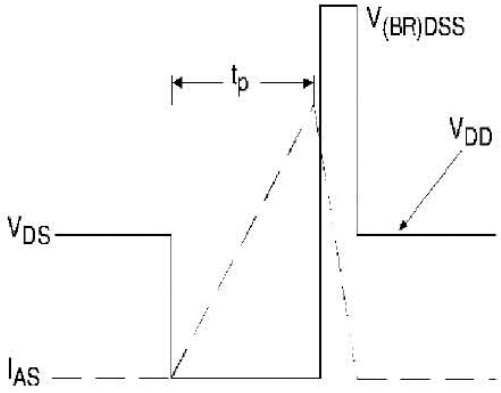


Fig 12b. Unclamped Inductive Waveforms

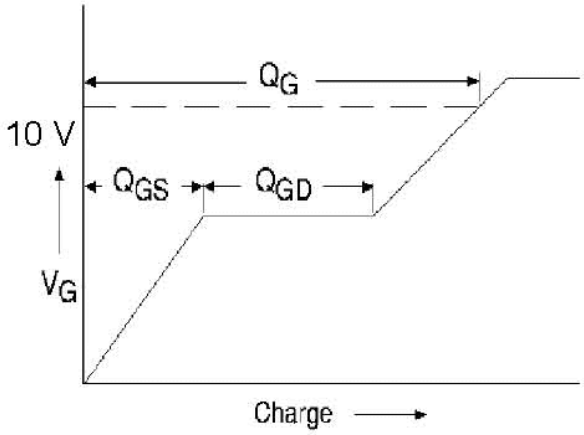


Fig 13a. Basic Gate Charge Waveform

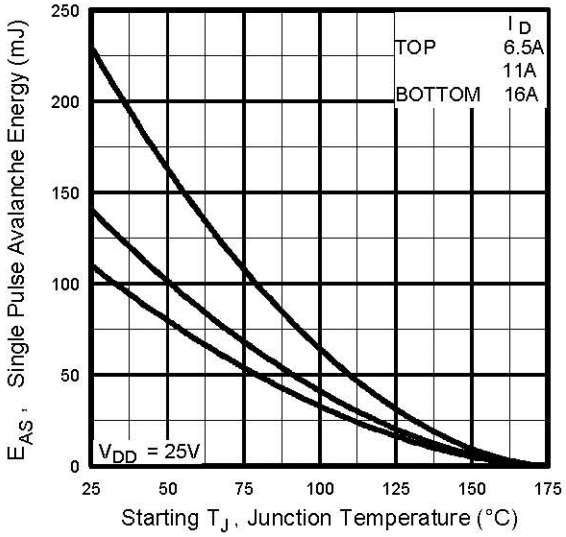


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

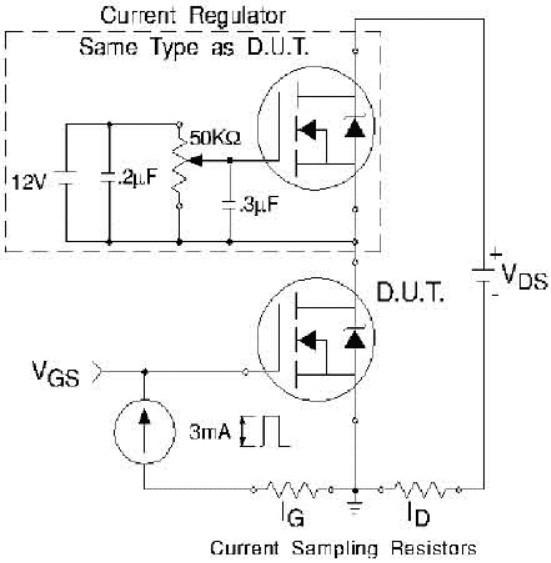


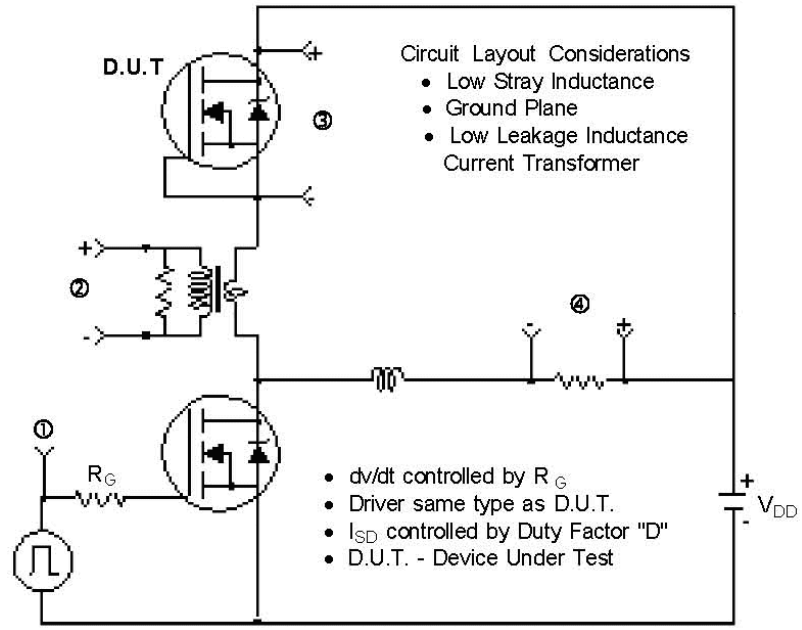
Fig 13b. Gate Charge Test Circuit

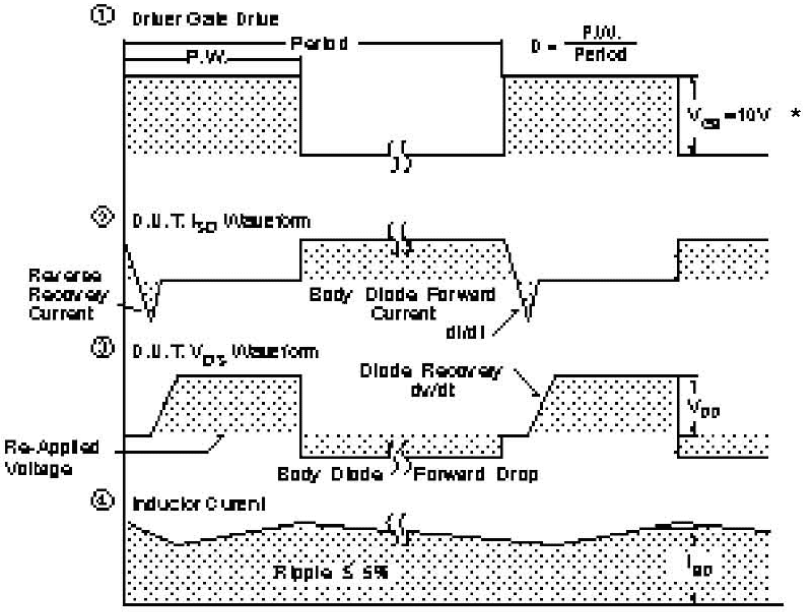
Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit

Appendix B: Package Outline Mechanical Drawing

Appendix C: Part Marking Information

Peak Diode Recovery dv/dt Test Circuit



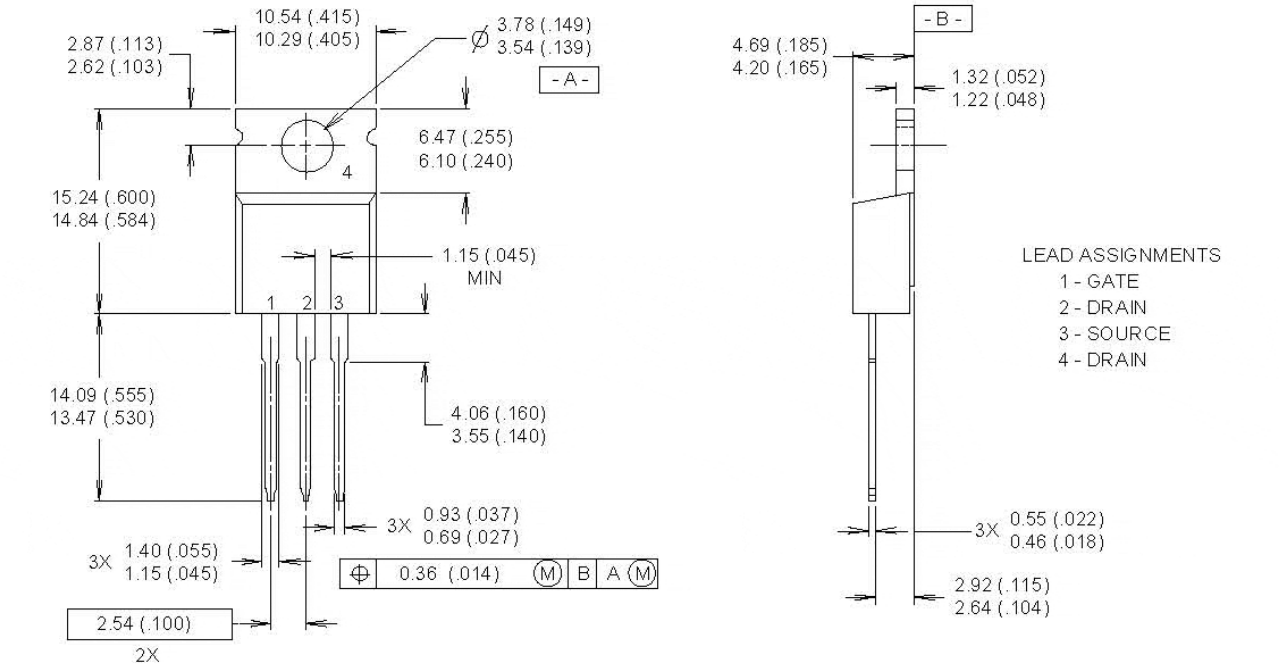


* VGS = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

TO-220AB Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.