

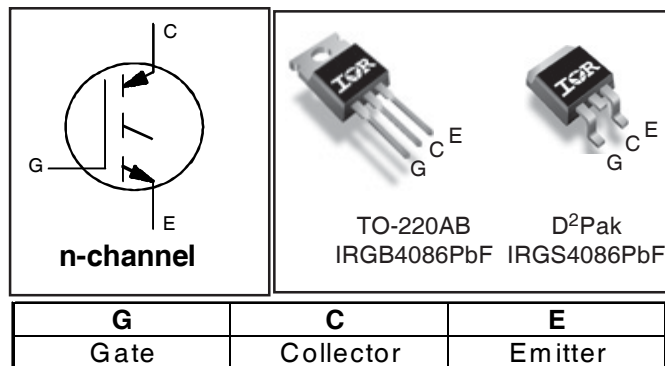
**PDP TRENCH IGBT**

**IRGB4086PbF**  
**IRGS4086PbF**

**Features**

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery Circuits in PDP Applications
- Low  $V_{CE(on)}$  and Energy per Pulse ( $E_{PULSE}^{TM}$ ) for Improved Panel Efficiency
- High Repetitive Peak Current Capability
- Lead Free Package

Key Parameters		
$V_{CE\ min}$	300	V
$V_{CE(ON)}\ typ.\ @\ I_C = 70A$	1.90	V
$I_{RP}\ max\ @\ T_C = 25^\circ C\ ①$	250	A
$T_J\ max$	150	$^\circ C$



**Description**

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low  $V_{CE(on)}$  and low  $E_{PULSE}^{TM}$  rating per silicon area which improve panel efficiency. Additional features are  $150^\circ C$  operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{GE}$	Gate-to-Emitter Voltage	$\pm 30$	V
$I_C\ @\ T_C = 25^\circ C$	Continuous Collector Current, $V_{GE}\ @\ 15V$	70	A
$I_C\ @\ T_C = 100^\circ C$	Continuous Collector, $V_{GE}\ @\ 15V$	40	
$I_{RP}\ @\ T_C = 25^\circ C$	Repetitive Peak Current ①	250	
$P_D\ @\ T_C = 25^\circ C$	Power Dissipation	160	W
$P_D\ @\ T_C = 100^\circ C$	Power Dissipation	63	
	Linear Derating Factor	1.3	$W/^\circ C$
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-40 to + 150	$^\circ C$
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10lb·in (1.1N·m)	N

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Thermal Resistance Junction-to-Case-(each IGBT) ②	—	0.8	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink (flat, greased surface)	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient (typical socket mount) ②④	—	40	
	Weight	6.0 (0.21)	—	g (oz)

Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{CES}$	Collector-to-Emitter Breakdown Voltage	300	—	—	V	$V_{GE} = 0V, I_{CE} = 1\text{ mA}$
$\Delta BV_{CES}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.29	—	V/°C	Reference to $25^\circ\text{C}, I_{CE} = 1\text{ mA}$
$V_{CE(on)}$	Static Collector-to-Emitter Voltage	—	1.29	1.55	V	$V_{GE} = 15V, I_{CE} = 25A$ ③
		—	1.49	1.67		$V_{GE} = 15V, I_{CE} = 40A$ ③
		—	1.90	2.10		$V_{GE} = 15V, I_{CE} = 70A$ ③
		—	2.57	2.96		$V_{GE} = 15V, I_{CE} = 120A$ ③
		—	2.27	—		$V_{GE} = 15V, I_{CE} = 70A, T_J = 150^\circ\text{C}$
$V_{GE(th)}$	Gate Threshold Voltage	2.6	—	5.0	V	$V_{CE} = V_{GE}, I_{CE} = 500\mu\text{A}$
$\Delta V_{GE(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-11	—	mV/°C	
$I_{CES}$	Collector-to-Emitter Leakage Current	—	2.0	25	$\mu\text{A}$	$V_{CE} = 300V, V_{GE} = 0V$
		—	5.0	—		$V_{CE} = 300V, V_{GE} = 0V, T_J = 100^\circ\text{C}$
		—	100	—		$V_{CE} = 300V, V_{GE} = 0V, T_J = 150^\circ\text{C}$
$I_{GES}$	Gate-to-Emitter Forward Leakage	—	—	100	nA	$V_{GE} = 30V$
	Gate-to-Emitter Reverse Leakage	—	—	-100		$V_{GE} = -30V$
$g_{fe}$	Forward Transconductance	—	29	—	S	$V_{CE} = 25V, I_{CE} = 25A$
$Q_g$	Total Gate Charge	—	65	—	nC	$V_{CE} = 200V, I_C = 25A, V_{GE} = 15V$ ③
$Q_{gc}$	Gate-to-Collector Charge	—	22	—		
$t_{d(on)}$	Turn-On delay time	—	36	—	ns	$I_C = 25A, V_{CC} = 196V$ $R_G = 10\Omega, L = 200\mu\text{H}, L_S = 200\text{nH}$ $T_J = 25^\circ\text{C}$
$t_r$	Rise time	—	31	—		
$t_{d(off)}$	Turn-Off delay time	—	112	—		
$t_f$	Fall time	—	65	—		
$t_{d(on)}$	Turn-On delay time	—	30	—	ns	$I_C = 25A, V_{CC} = 196V$ $R_G = 10\Omega, L = 200\mu\text{H}, L_S = 200\text{nH}$ $T_J = 150^\circ\text{C}$
$t_r$	Rise time	—	33	—		
$t_{d(off)}$	Turn-Off delay time	—	145	—		
$t_f$	Fall time	—	98	—		
$t_{st}$	Shoot Through Blocking Time	100	—	—	ns	$V_{CC} = 240V, V_{GE} = 15V, R_G = 5.1\Omega$
$E_{PULSE}$	Energy per Pulse	—	1075	—	$\mu\text{J}$	$L = 220\text{nH}, C = 0.40\mu\text{F}, V_{GE} = 15V$ $V_{CC} = 240V, R_G = 5.1\Omega, T_J = 25^\circ\text{C}$
		—	1432	—		$L = 220\text{nH}, C = 0.40\mu\text{F}, V_{GE} = 15V$ $V_{CC} = 240V, R_G = 5.1\Omega, T_J = 100^\circ\text{C}$
$C_{iss}$	Input Capacitance	—	2250	—	pF	$V_{GE} = 0V$
$C_{oss}$	Output Capacitance	—	110	—		$V_{CE} = 30V$
$C_{rss}$	Reverse Transfer Capacitance	—	58	—		$f = 1.0\text{MHz}$ , See Fig.13
$L_C$	Internal Collector Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.)
$L_E$	Internal Emitter Inductance	—	13	—		from package and center of die contact

## Notes:

- ① Half sine wave with duty cycle = 0.1,  $t_{on} = 2\mu\text{sec}$ .  
 ②  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .

- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .  
 ④ When mounted on 1" square PCB (FR-4 or G-10 Material).  
 For recommended footprint and soldering techniques refer to application note #AN-994.

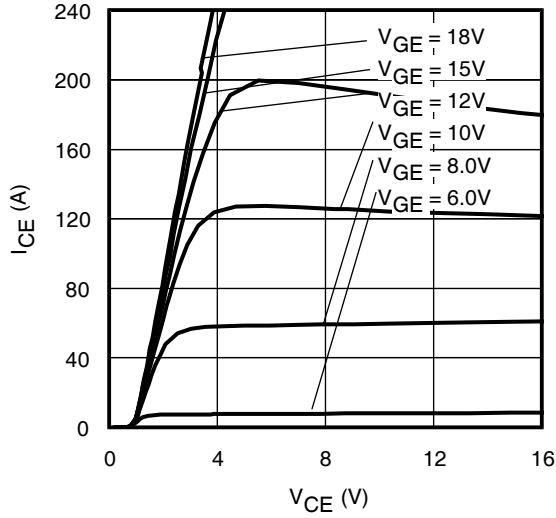


Fig 1. Typical Output Characteristics @ 25°C

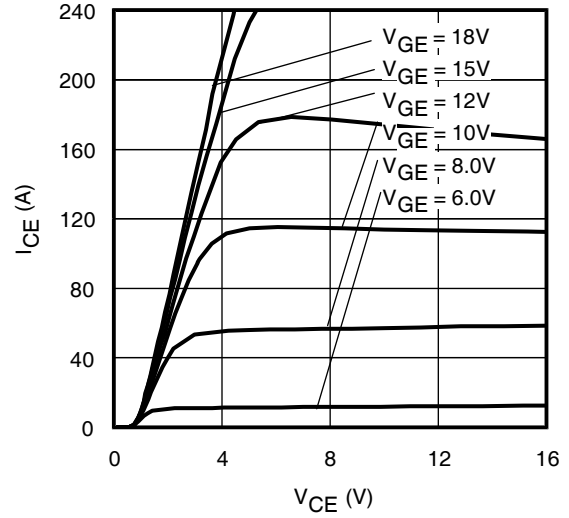


Fig 2. Typical Output Characteristics @ 75°C

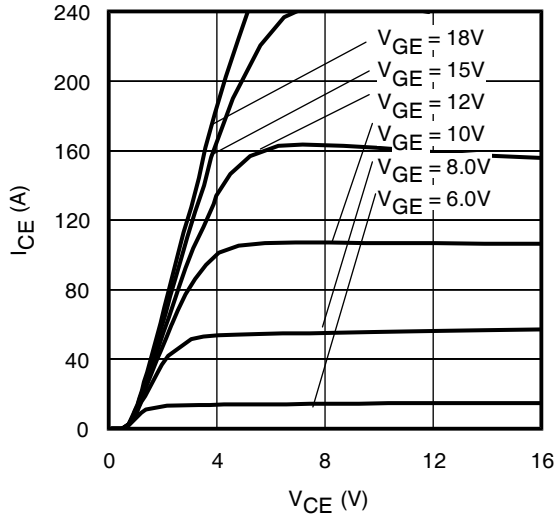


Fig 3. Typical Output Characteristics @ 125°C

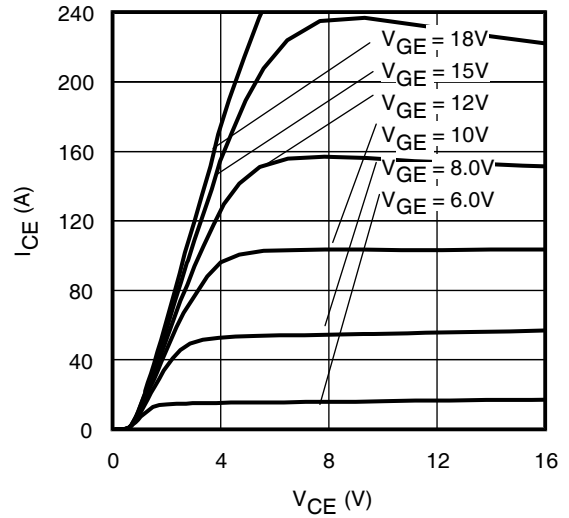


Fig 4. Typical Output Characteristics @ 150°C

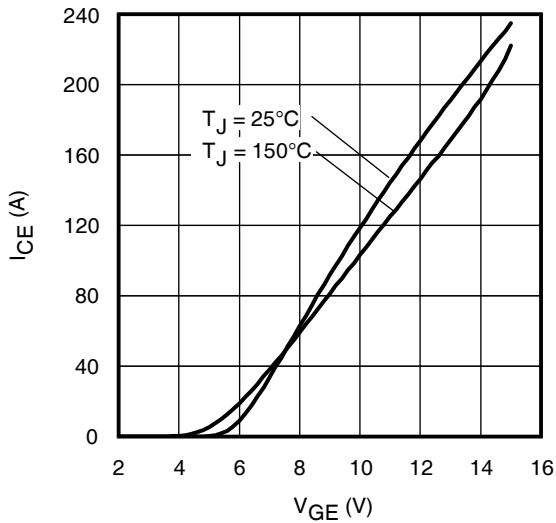


Fig 5. Typical Transfer Characteristics

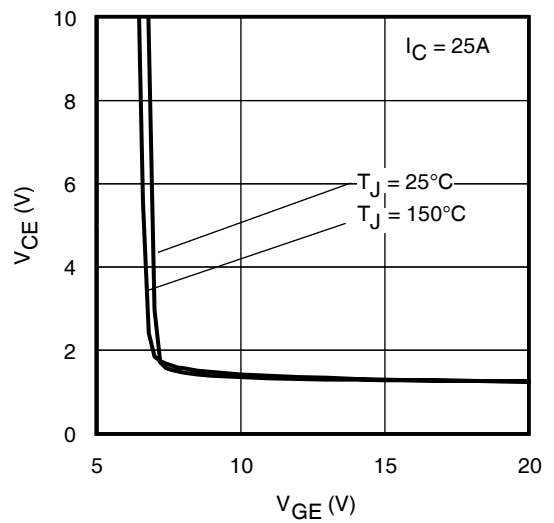


Fig 6.  $V_{CE(ON)}$  vs. Gate Voltage

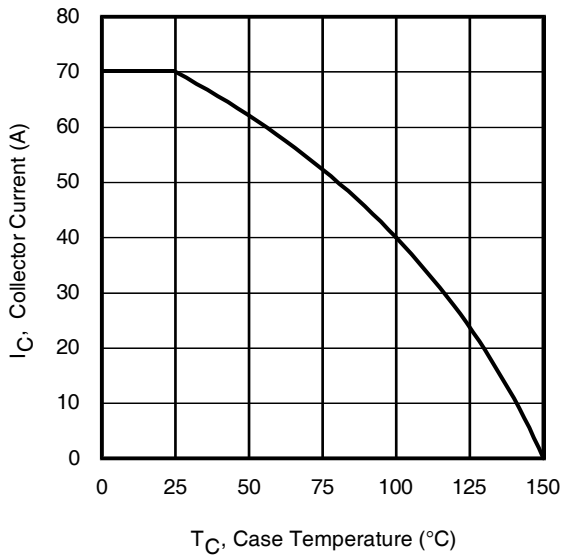


Fig 7. Maximum Collector Current vs. Case Temperature

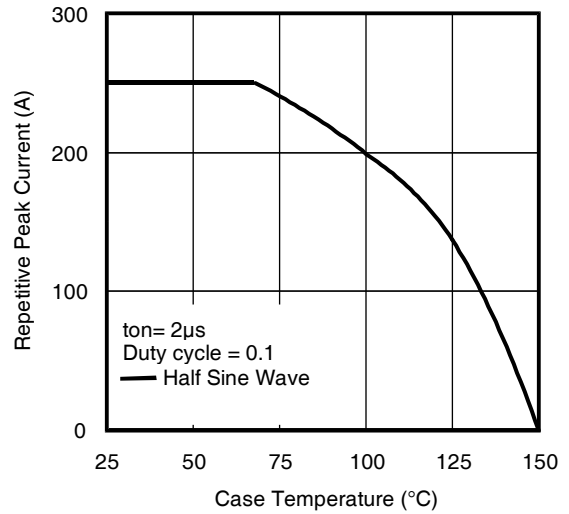


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

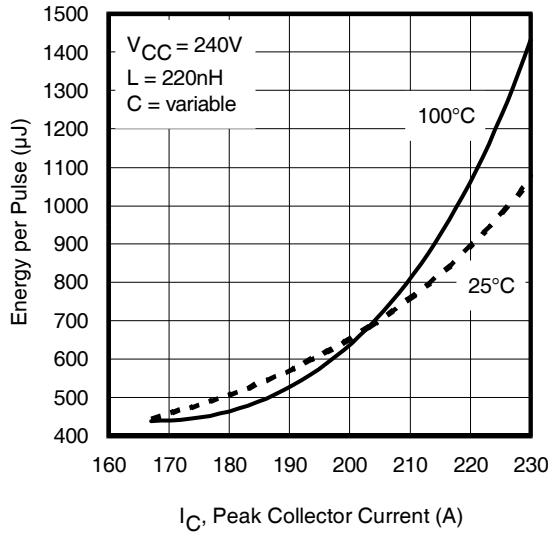


Fig 9. Typical  $E_{PULSE}$  vs. Collector Current

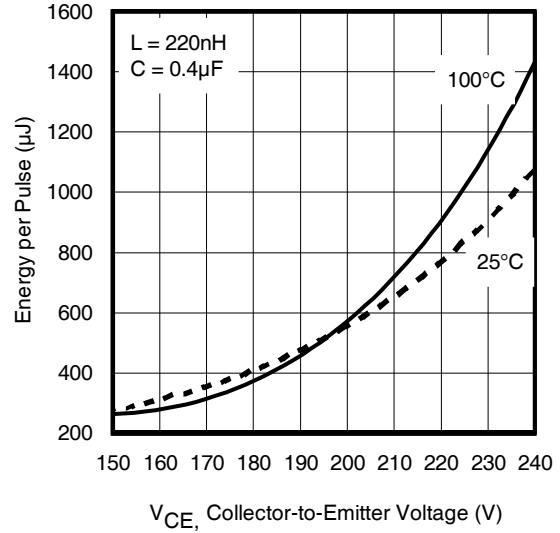


Fig 10. Typical  $E_{PULSE}$  vs. Collector-to-Emitter Voltage

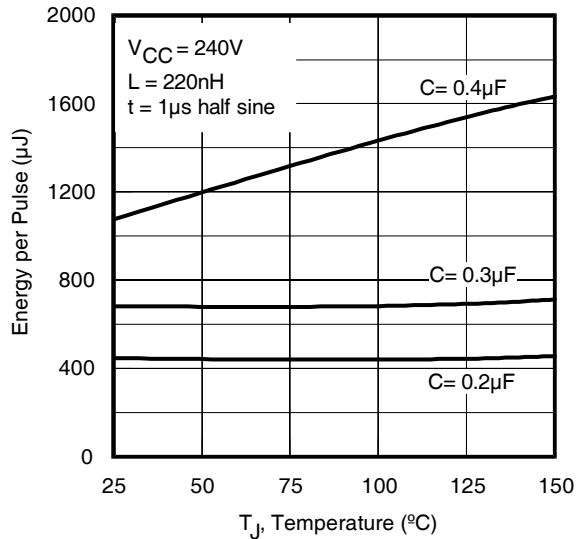


Fig 11.  $E_{PULSE}$  vs. Temperature

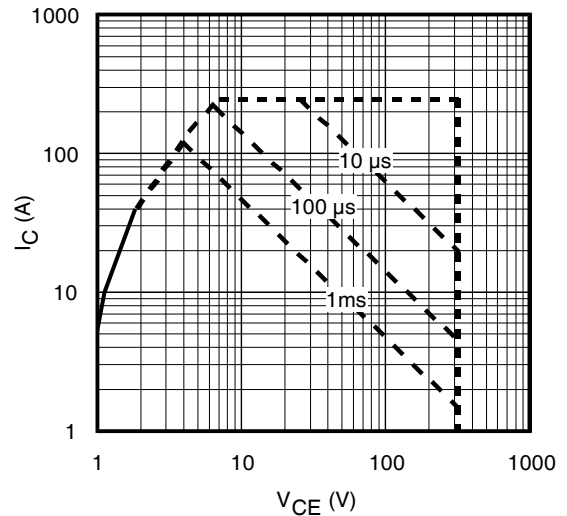


Fig 12. Forward Bias Safe Operating Area

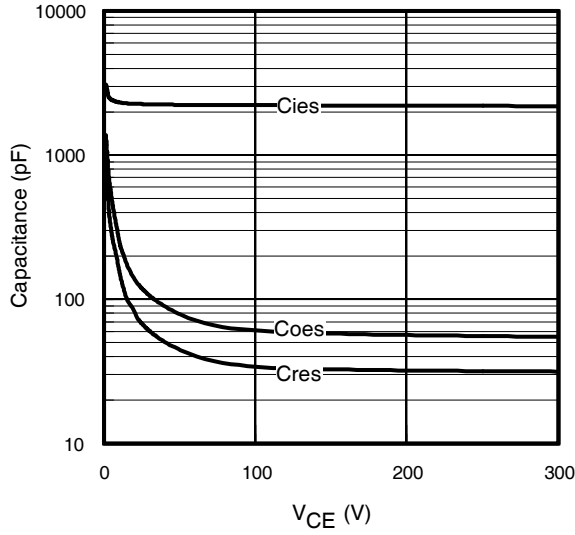


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

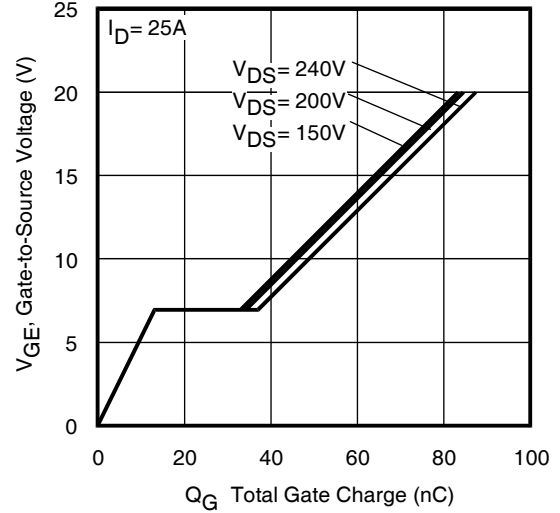


Fig 14. Typical Gate Charge vs. Gate-to-Source Voltage

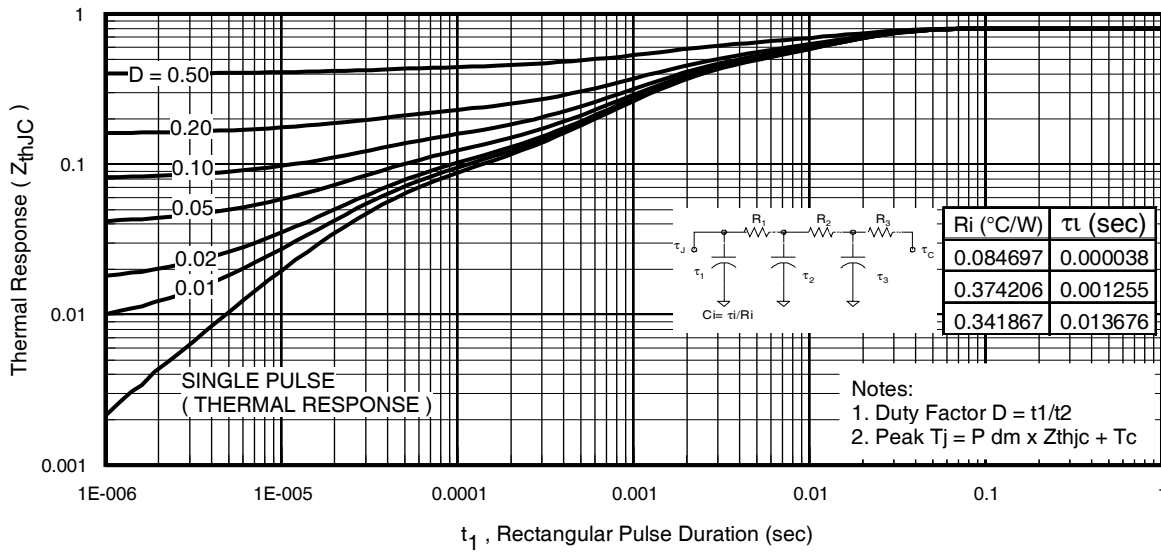
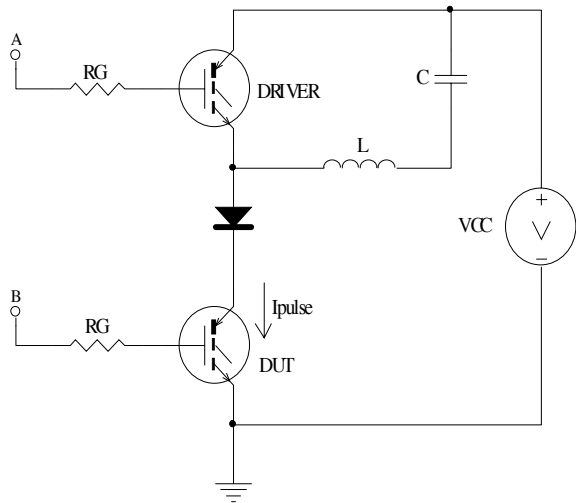
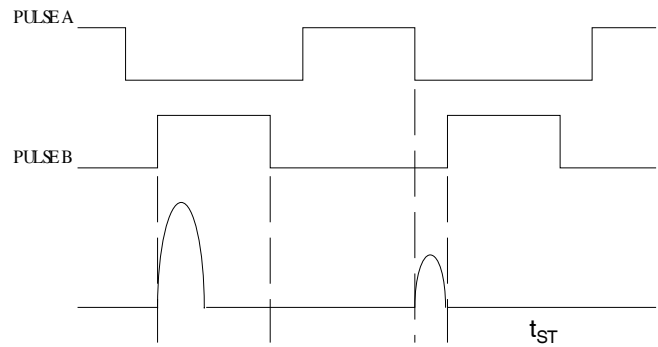


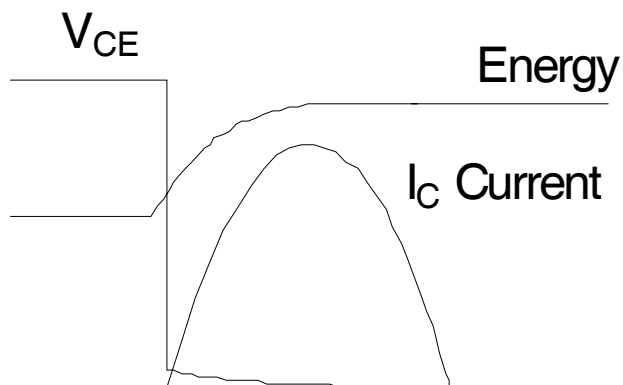
Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case (IGBT)



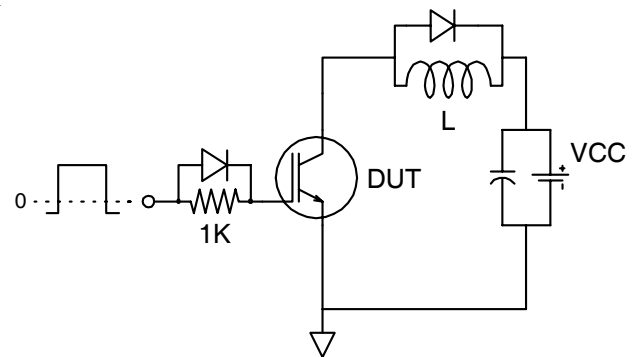
**Fig 16a.**  $t_{st}$  and  $E_{PULSE}$  Test Circuit



**Fig 16b.**  $t_{st}$  Test Waveforms



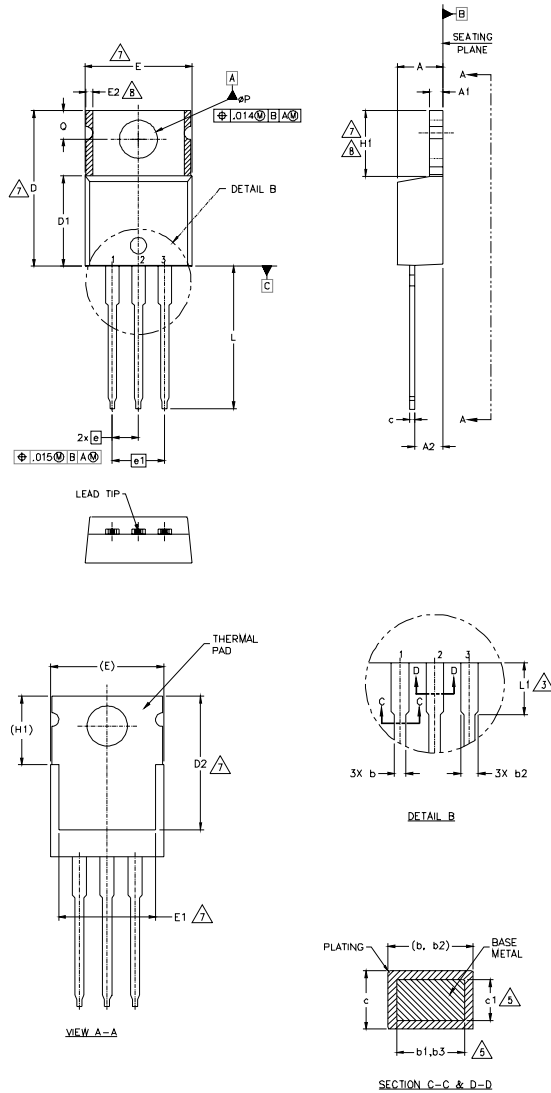
**Fig 16c.**  $E_{PULSE}$  Test Waveforms



**Fig. 17 -** Gate Charge Circuit (turn-off)

### TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

**LEAD ASSIGNMENTS**

- HEXFET**  
 1.- GATE  
 2.- DRAIN  
 3.- SOURCE

**IGBTs, CoPACK**

- 1.- GATE  
 2.- COLLECTOR  
 3.- EMITTER

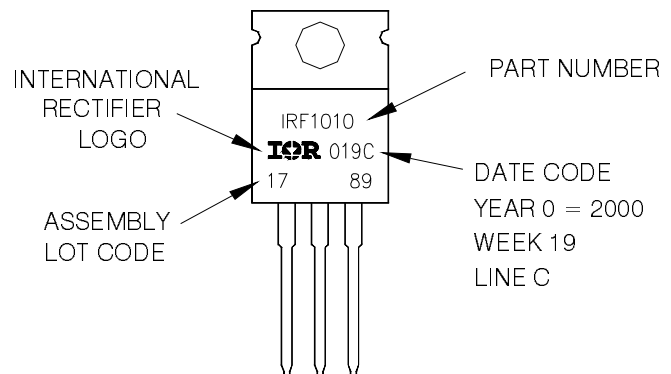
**DIODES**

- 1.- ANODE  
 2.- CATHODE  
 3.- ANODE

### TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 2000  
 IN THE ASSEMBLY LINE "C"

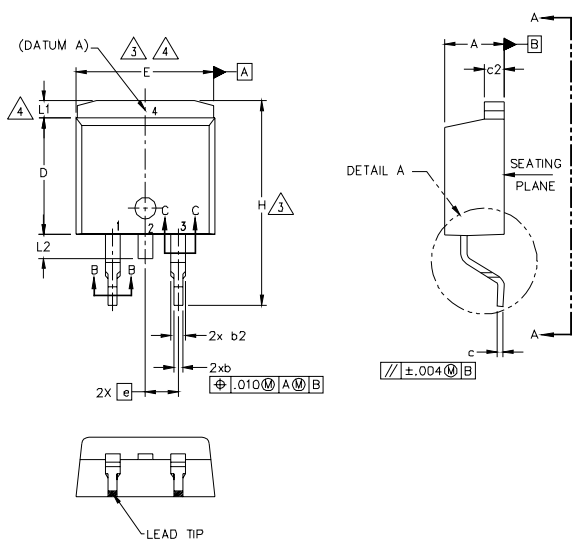
Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

## D<sup>2</sup>Pak Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	-	1.65	-	.066	
L2	1.27	1.78	-	.070	4
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

### LEAD ASSIGNMENTS

#### DIODES

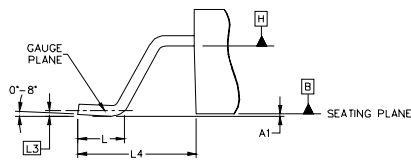
- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

#### HEXFET

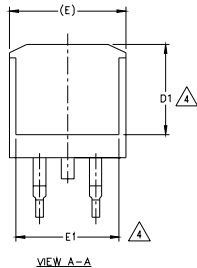
- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

#### IGBTs, CoPACK

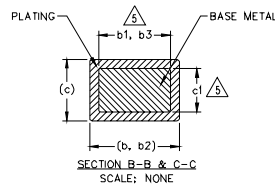
- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER



DETAIL "A"  
ROTATED 90° CW  
SCALE 8:1



VIEW A-A



SECTION B-B & C-C  
SCALE: NONE

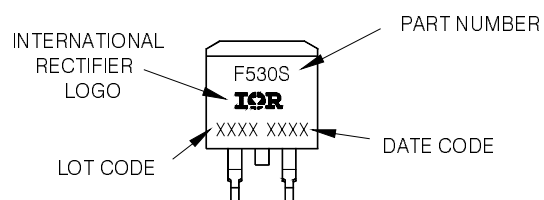
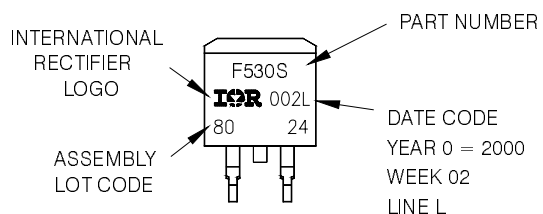
### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

## D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"

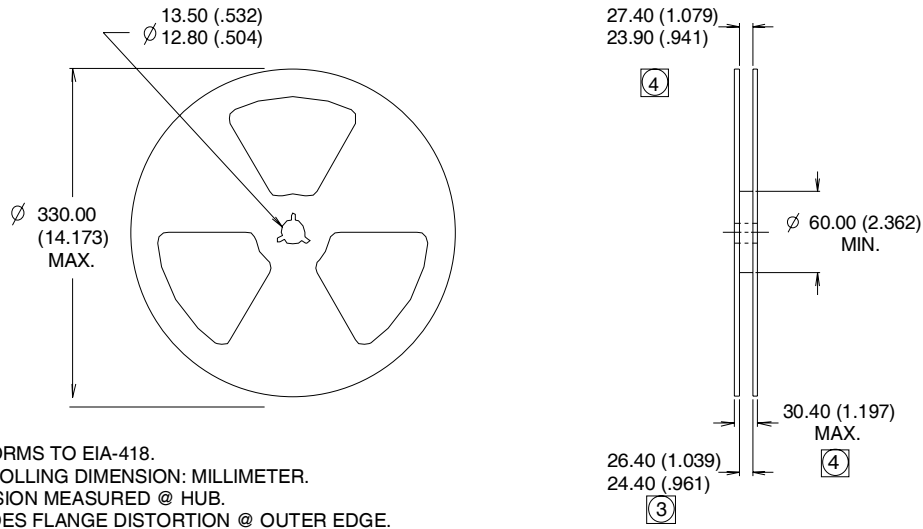
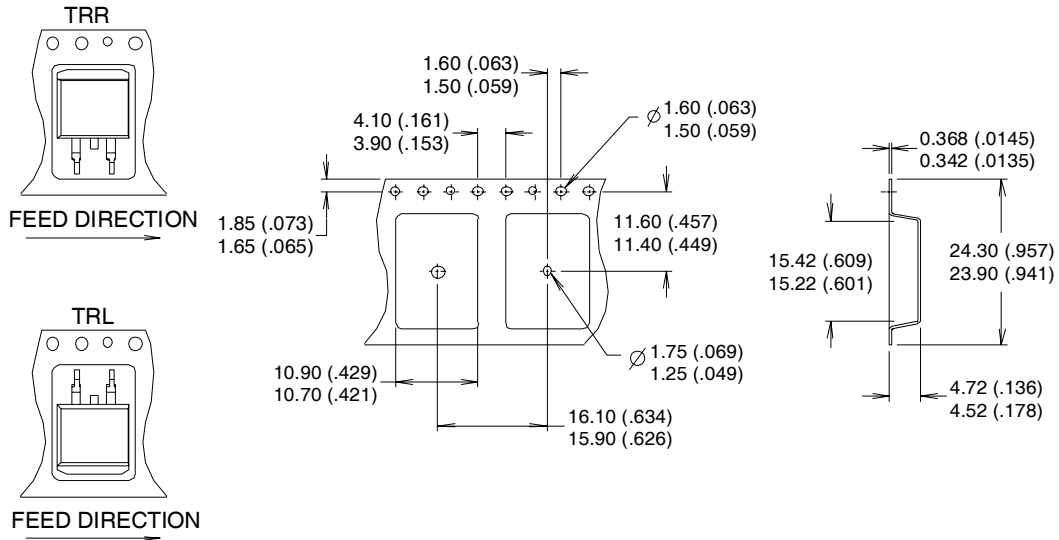
EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
For GB Produced ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>



## D<sup>2</sup>Pak Tape & Reel Information



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
 This product has been designed for the Industrial market.  
 Qualification Standards can be found on IR's Web site.