

**RADIATION HARDENED 60V, Combination 2N-2P-CHANNEL  
 LOGIC LEVEL POWER MOSFET  
 THRU-HOLE (14-LEAD FLAT PACK)**



**Product Summary**

Part Number	Radiation Level	R <sub>DS(on)</sub>	I <sub>D</sub>	CHANNEL
IRHLA7670Z4	100K Rads (Si)	0.60Ω	0.8A	N
		1.36Ω	-0.56A	P
IRHLA7630Z4	300K Rads (Si)	0.60Ω	0.8A	N
		1.36Ω	-0.56A	P



International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

**Features:**

- 5V CMOS and TTL Compatible
- Low R<sub>DS(on)</sub>
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight

**Absolute Maximum Ratings (Per Die)**

**Pre-Irradiation**

	Parameter	N-Channel	P-Channel	Units
I <sub>D</sub> @ V <sub>GS</sub> = ±4.5V, T <sub>C</sub> = 25°C	Continuous Drain Current	0.8	-0.56	A
I <sub>D</sub> @ V <sub>GS</sub> = ±4.5V, T <sub>C</sub> = 100°C	Continuous Drain Current	0.5	-0.35	
I <sub>DM</sub>	Pulsed Drain Current ①	3.2	-2.24	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Max. Power Dissipation	0.6	0.6	W
	Linear Derating Factor	0.005	0.005	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	±10	±10	V
EAS	Single Pulse Avalanche Energy	16 ②	26 ⑦	mJ
I <sub>AR</sub>	Avalanche Current ①	0.8	-0.56	A
EAR	Repetitive Avalanche Energy ①	0.06	0.06	mJ
dv/dt	Peak Diode Recovery dv/dt	10.2 ③	-5.79 ⑧	V/ns
T <sub>J</sub>	Operating Junction	-55 to 150		°C
T <sub>STG</sub>	Storage Temperature Range			
	Lead Temperature	300 (0.63 in./1.6 mm from case for 10s)		
	Weight	0.52 (Typical)		g

For footnotes refer to the last page

Electrical Characteristics For Each N-Channel Device @T<sub>j</sub> = 25°C (Unless Otherwise specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Temperature Coefficient of Breakdown Voltage	—	0.067	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	0.60	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 0.5A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-4.7	—	mV/°C	
g <sub>fs</sub>	Forward Transconductance	0.23	—	—	S	V <sub>DS</sub> = 10V, I <sub>DS</sub> = 0.5A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	1.0	μA	V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V
		—	—	10		V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 10V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -10V
Q <sub>g</sub>	Total Gate Charge	—	—	2.8	nC	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 0.8A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	0.6		V <sub>DS</sub> = 30V
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	—	—	1.6		
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	6.5	ns	V <sub>DD</sub> = 30V, I <sub>D</sub> = 0.8A, V <sub>GS</sub> = 5.0V, R <sub>G</sub> = 24Ω
t <sub>r</sub>	Rise Time	—	—	2.5		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	35		
t <sub>f</sub>	Fall Time	—	—	13		
L <sub>S</sub> + L <sub>D</sub>	Total Inductance	—	20	—	nH	Measured from Drain lead (6mm /0.25in from pack.) to Source lead (6mm/0.25in from pack.)with Source wire internally bonded from Source pin to Drain pad
C <sub>iss</sub>	Input Capacitance	—	141	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	38	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	1.4	—		
R <sub>g</sub>	Gate Resistance	—	8.0	—	Ω	f = 1.0MHz, open drain

## Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	0.8	A	
I <sub>SM</sub>	Pulse Source Current (Body Diode) ①	—	—	3.2		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 0.8A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	55	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 0.8A, di/dt ≤ 100A/μs
Q <sub>RR</sub>	Reverse Recovery Charge	—	—	63	nC	V <sub>DD</sub> ≤ 25V ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .				

## Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R <sub>thJA</sub>	Junction-to-Ambient	—	—	210	°C/W	Typical socket mount

Note: Corresponding Spice and Saber models are available on International Rectifier Website.

For footnotes refer to the last page

**Pre-Irradiation**

**IRHLA7670Z4, 2N7633M2**

**Electrical Characteristics For Each P-Channel Device @Tj = 25°C (Unless Otherwise specified)**

	Parameter	Min	Typ	Max	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	-60	—	—	V	VGS = 0V, ID = -250μA
ΔBVDSS/ΔTJ	Temperature Coefficient of Breakdown Voltage	—	-0.063	—	V/°C	Reference to 25°C, ID = -1.0mA
RDS(on)	Static Drain-to-Source On-State Resistance	—	—	1.36	Ω	VGS = -4.5V, ID = -0.35A ④
VGS(th)	Gate Threshold Voltage	-1.0	—	-2.0	V	VDS = VGS, ID = -250μA
ΔVGS(th)/ΔTJ	Gate Threshold Voltage Coefficient	—	3.2	—	mV/°C	
gfs	Forward Transconductance	0.7	—	—	S	VDS = -10V, IDS = -0.35A ④
IDSS	Zero Gate Voltage Drain Current	—	—	-1.0	μA	VDS = -48V, VGS = 0V
		—	—	-10		VDS = -48V, VGS = 0V, Tj = 125°C
IGSS	Gate-to-Source Leakage Forward	—	—	-100	nA	VGS = -10V
IGSS	Gate-to-Source Leakage Reverse	—	—	100		VGS = 10V
Qg	Total Gate Charge	—	—	2.8	nC	VGS = -4.5V, ID = -0.56A
Qgs	Gate-to-Source Charge	—	—	1.7		VDS = -30V
Qgd	Gate-to-Drain ('Miller') Charge	—	—	1.2		
td(on)	Turn-On Delay Time	—	—	22	ns	VDD = -30V, ID = -0.56A, VGS = -5.0V, RG = 24Ω
tr	Rise Time	—	—	22		
td(off)	Turn-Off Delay Time	—	—	40		
tf	Fall Time	—	—	32		
LS + LD	Total Inductance	—	20	—	nH	Measured from Drain lead (6mm /0.25in from pack.) to Source lead (6mm/0.25in from pack.)with Source wire internally bonded from Source pin to Drain pad
Ciss	Input Capacitance	—	144	—	pF	VGS = 0V, VDS = -25V f = 1.0MHz
Coss	Output Capacitance	—	41	—		
Crss	Reverse Transfer Capacitance	—	6.6	—		
Rg	Gate Resistance	—	55	—		

**Source-Drain Diode Ratings and Characteristics (Per Die)**

	Parameter	Min	Typ	Max	Units	Test Conditions
IS	Continuous Source Current (Body Diode)	—	—	-0.56	A	
ISM	Pulse Source Current (Body Diode) ①	—	—	-2.24		
VSD	Diode Forward Voltage	—	—	-5.0	V	Tj = 25°C, IS = -0.56A, VGS = 0V ④
trr	Reverse Recovery Time	—	—	35	ns	Tj = 25°C, IF = -0.56A, di/dt ≤ -100A/μs
QRR	Reverse Recovery Charge	—	—	9.6	nC	VDD ≤ -25V ④
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

**Thermal Resistance (Per Die)**

	Parameter	Min	Typ	Max	Units	Test Conditions
RthJA	Junction-to-Ambient	—	—	210	°C/W	Typical socket mount

**Note: Corresponding Spice and Saber models are available on International Rectifier Website.**

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table 1. Electrical Characteristics For Each N-Channel Device @Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

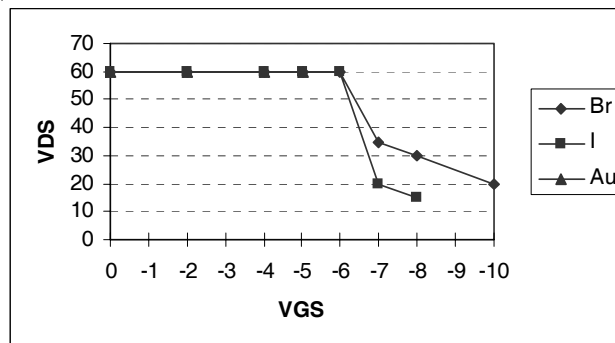
	Parameter	Up to 300K Rads (Si) <sup>1</sup>		Units	Test Conditions
		Min	Max		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	2.0		V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250μA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	100	nA	V <sub>GS</sub> = 10V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	-100		V <sub>GS</sub> = -10V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	1.0	μA	V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance (TO-39) ④	—	0.60	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 0.5A
R <sub>DS(on)</sub>	Static Drain-to-Source On-state Resistance (14-Lead Flat Pack) ④	—	0.60	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 0.5A
V <sub>SD</sub>	Diode Forward Voltage ④	—	1.2	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 0.8A

1. Part numbers IRHLA7670Z4, IRHLA7630Z4

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

**Table 2. Typical Single Event Effect Safe Operating Area (Per Die)**

Ion	LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)							
				@VGS=0V	@VGS=-2V	@VGS=-4V	@VGS=-5V	@VGS=-6V	@VGS=-7V	@VGS=-8V	@VGS=-10V
Br	37	305	39	60	60	60	60	60	35	30	20
I	60	370	34	60	60	60	60	60	20	15	-
Au	84	390	30	60	60	60	60	-	-	-	-



**Fig a. Typical Single Event Effect, Safe Operating Area**

For footnotes refer to the last page

## Radiation Characteristics

## IRHLA7670Z4, 2N7633M2

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table 1. Electrical Characteristics For Each P-Channel Device @Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

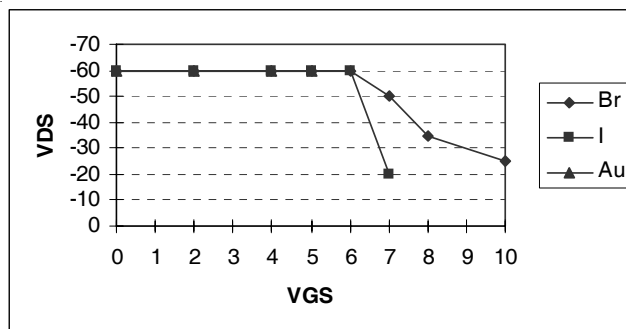
	Parameter	Up to 300K Rads (Si) <sup>1</sup>		Units	Test Conditions
		Min	Max		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-60	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	-1.0	-2.0		V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250μA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	-100	nA	V <sub>GS</sub> = -10V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	100		V <sub>GS</sub> = 10V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	-1.0	μA	V <sub>DS</sub> = -48V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance (TO-39) ④	—	1.25	Ω	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -0.35A
R <sub>DS(on)</sub>	Static Drain-to-Source On-state Resistance (14-Lead Flat Pack) ④	—	1.36	Ω	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -0.35A
V <sub>SD</sub>	Diode Forward Voltage④	—	-5.0	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -0.56A

1. Part numbers IRHLA7670Z4, IRHLA7630Z4

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

**Table 2. Typical Single Event Effect Safe Operating Area (Per Die)**

Ion	LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)							
				@VGS= 0V	@VGS= 2V	@VGS= 4V	@VGS= 5V	@VGS= 6V	@VGS= 7V	@VGS= 8V	@VGS= 10V
Br	37	305	39	-60	-60	-60	-60	-60	-50	-35	-25
I	60	370	34	-60	-60	-60	-60	-60	-20	-	-
Au	84	390	30	-60	-60	-60	-60	-	-	-	-



**Fig a. Typical Single Event Effect, Safe Operating Area**

For footnotes refer to the last page

N-Channel  
Q1, Q3

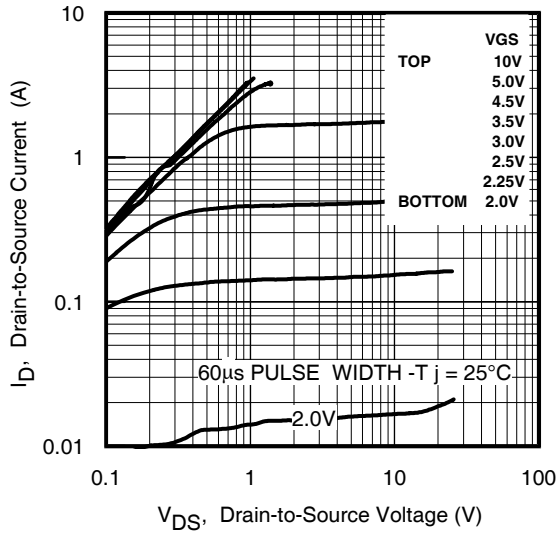


Fig 1. Typical Output Characteristics

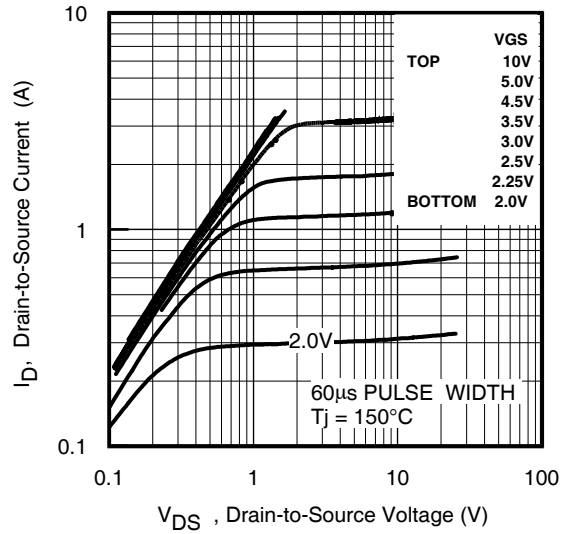


Fig 2. Typical Output Characteristics

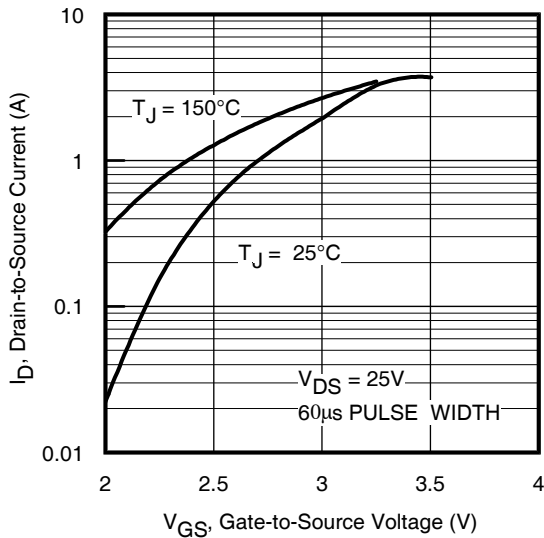


Fig 3. Typical Transfer Characteristics

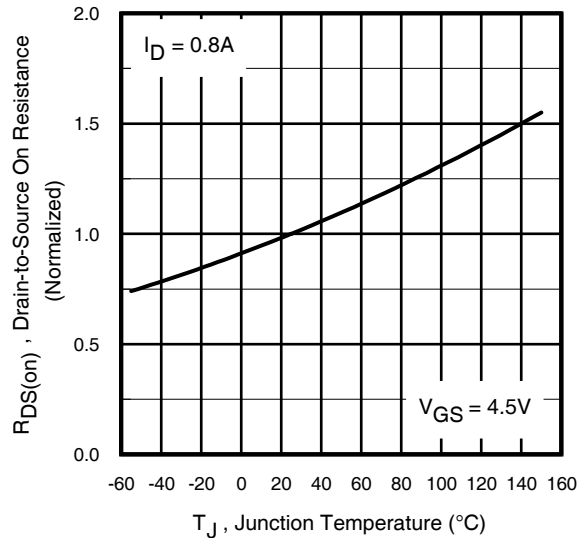


Fig 4. Normalized On-Resistance Vs. Temperature

N-Channel  
Q1,Q3

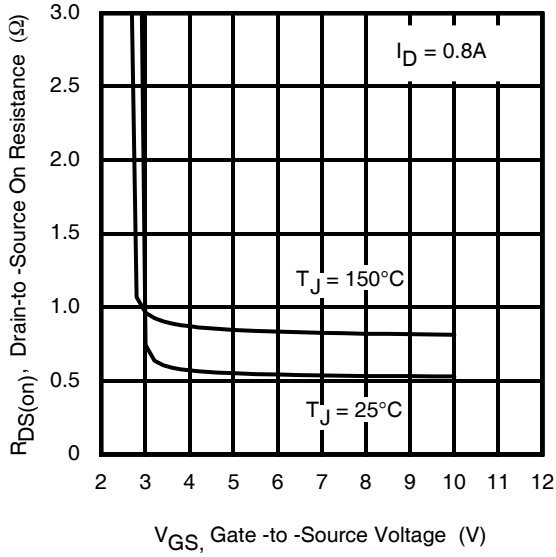


Fig 5. Typical On-Resistance Vs Gate Voltage

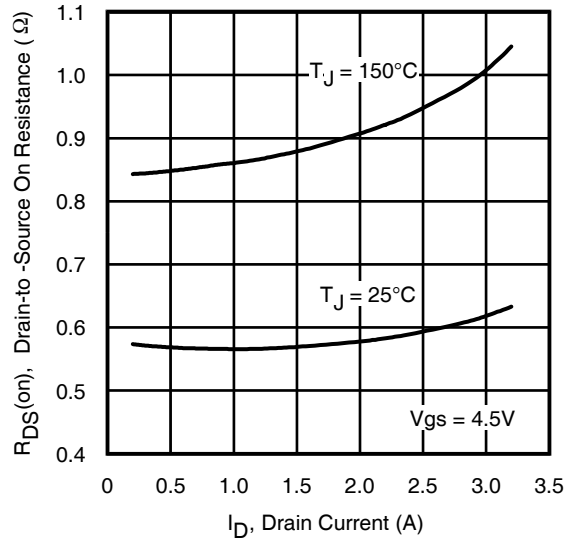


Fig 6. Typical On-Resistance Vs Drain Current

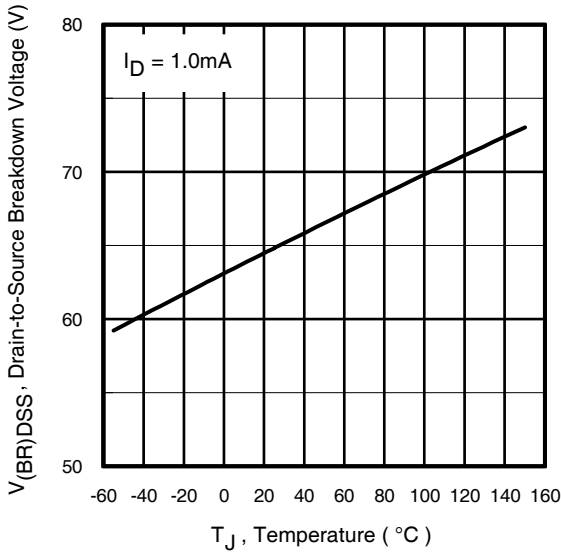


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

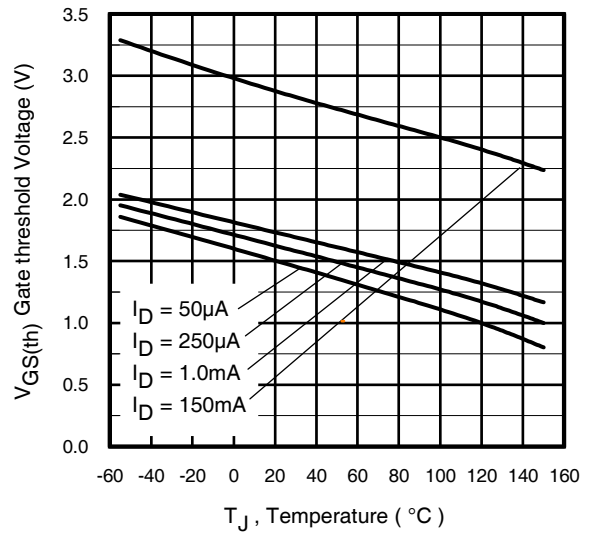


Fig 8. Typical Threshold Voltage Vs Temperature

N-Channel  
Q1,Q3

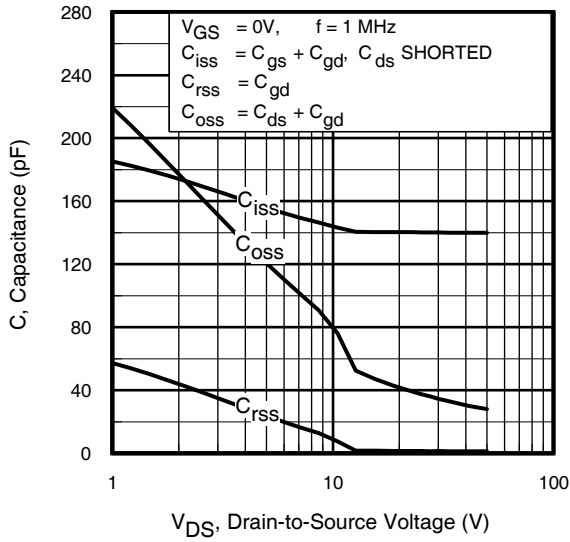


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

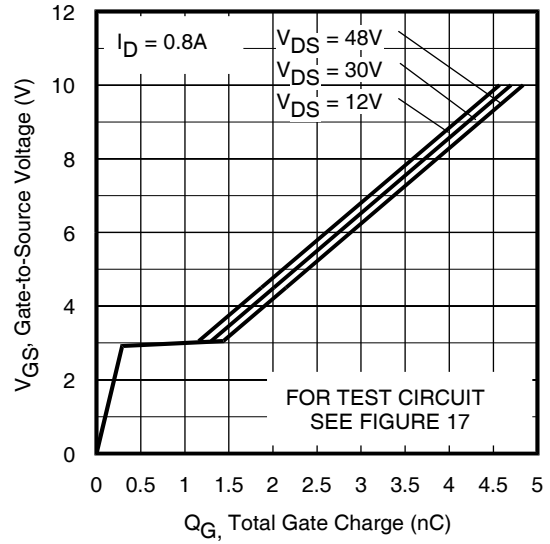


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

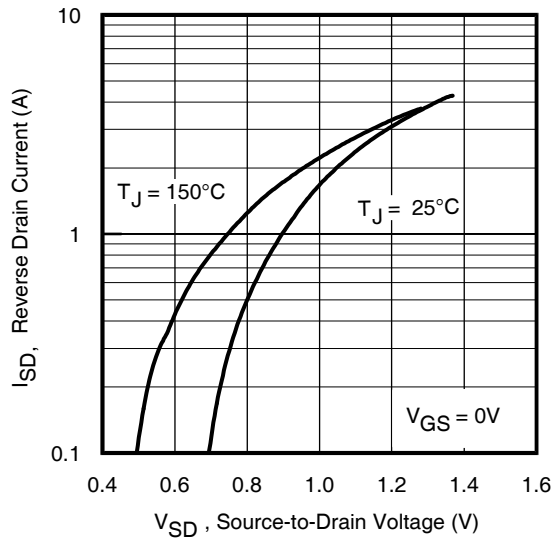


Fig 11. Typical Source-to-Drain Diode Forward Voltage

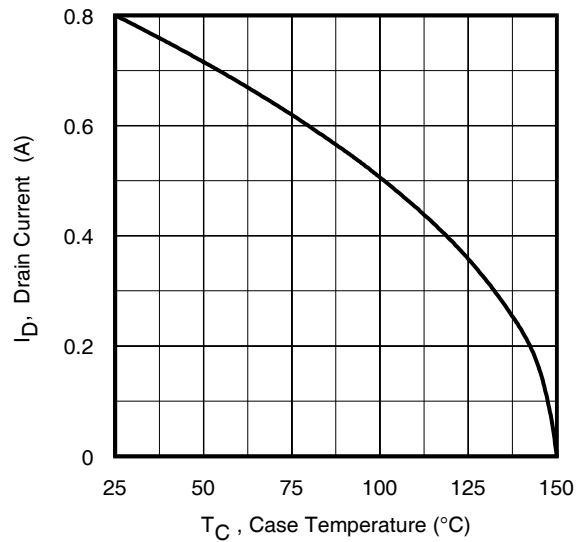


Fig 12. Maximum Drain Current Vs. Case Temperature



N-Channel  
Q1,Q3

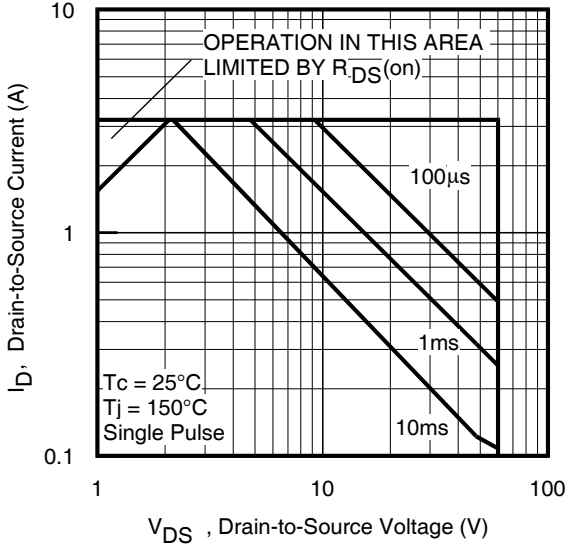


Fig 13. Maximum Safe Operating Area

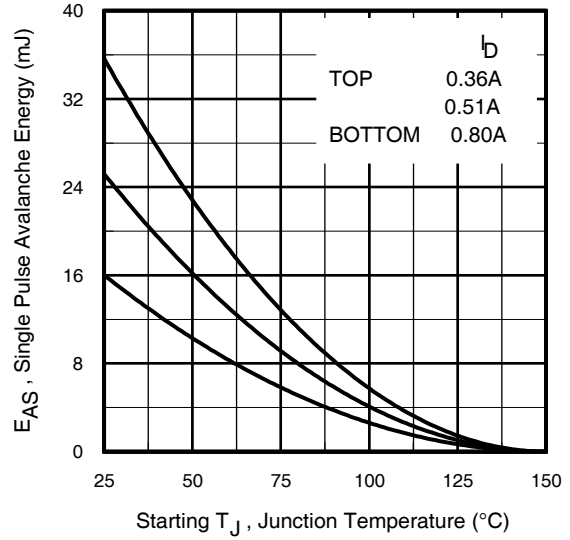


Fig 14. Maximum Avalanche Energy Vs. Drain Current

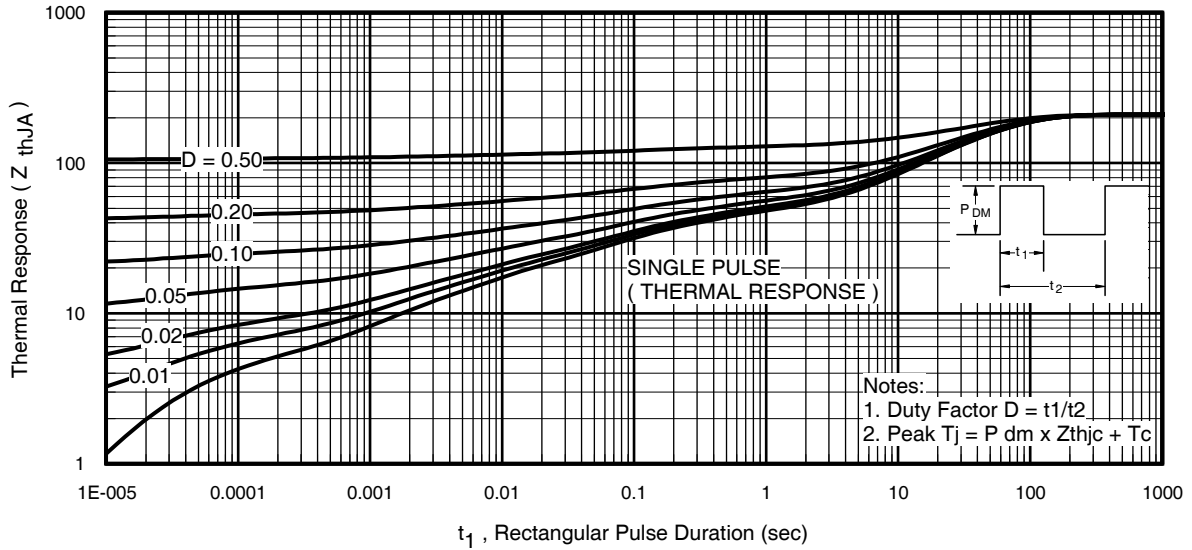


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

IRHLA7670Z4, 2N7633M2

N-Channel  
Q1,Q3

Pre-Irradiation

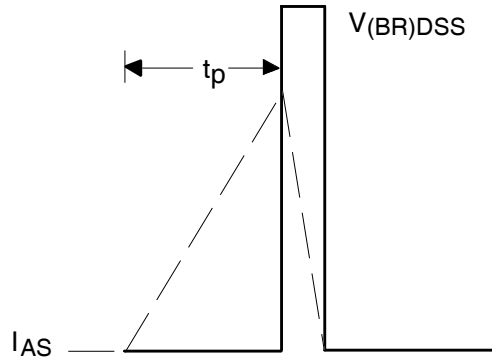
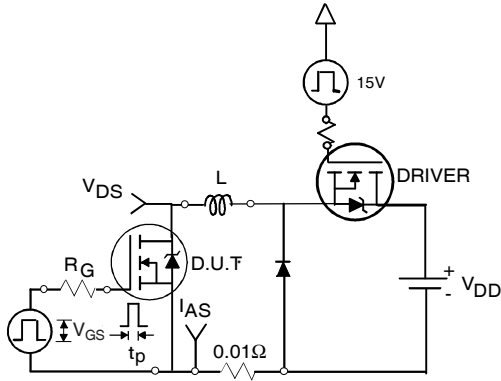


Fig 16a. Unclamped Inductive Test Circuit

Fig 16b. Unclamped Inductive Waveforms

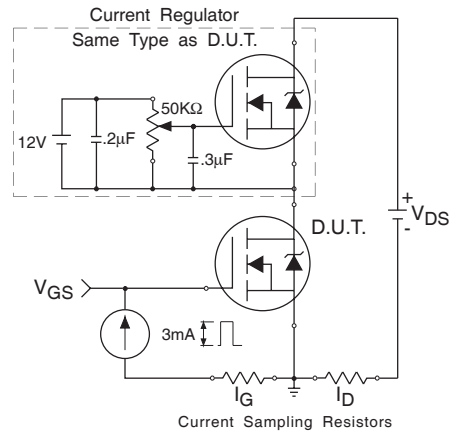
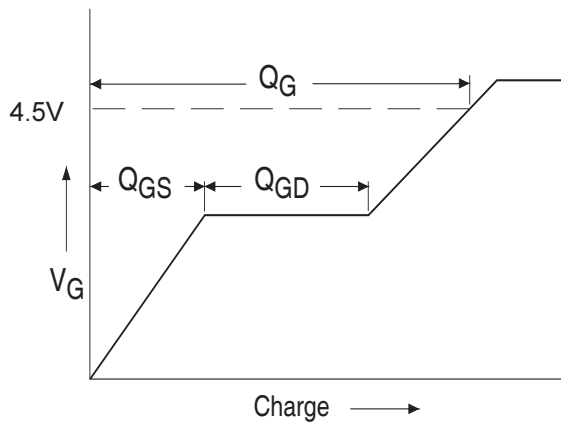


Fig 17a. Basic Gate Charge Waveform

Fig 17b. Gate Charge Test Circuit

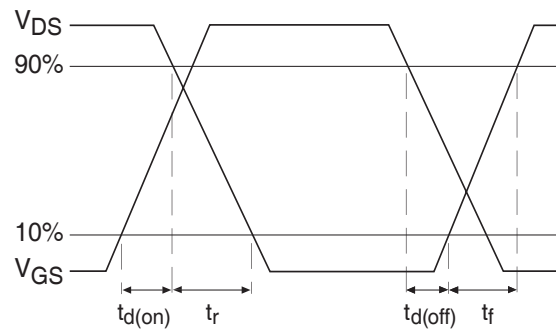
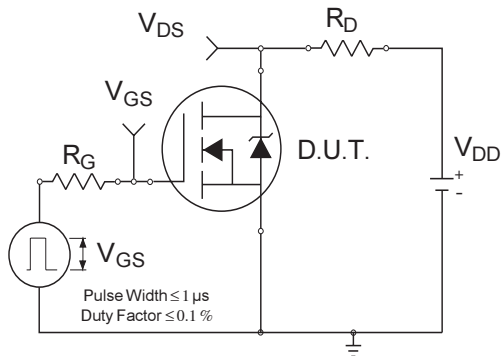


Fig 18a. Switching Time Test Circuit

Fig 18b. Switching Time Waveforms

P-Channel  
Q2,Q4

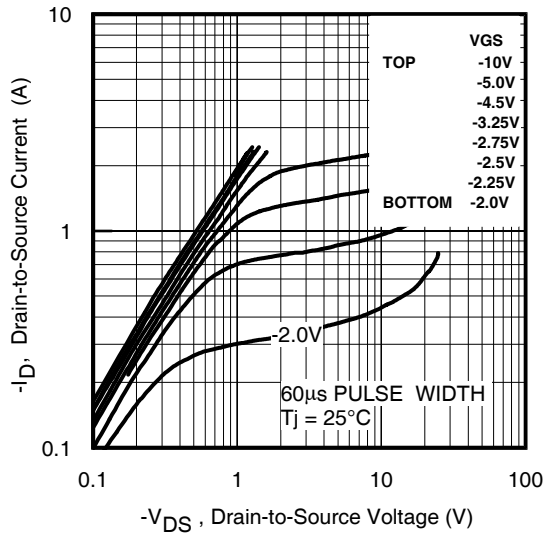


Fig 19. Typical Output Characteristics

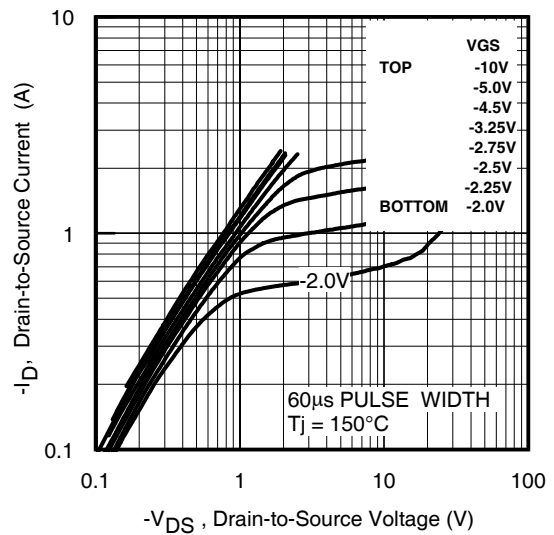


Fig 20. Typical Output Characteristics

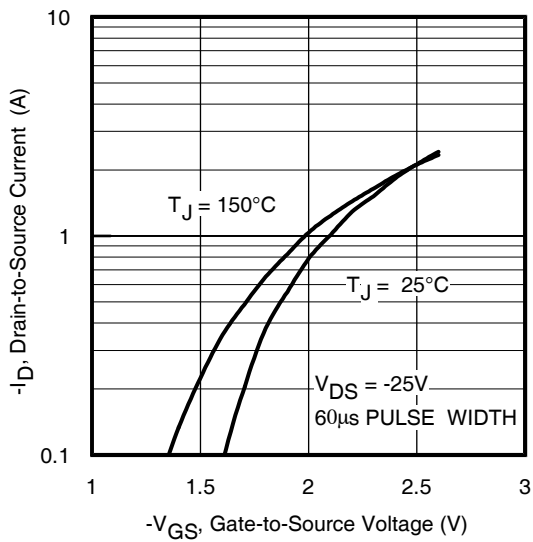


Fig 21. Typical Transfer Characteristics

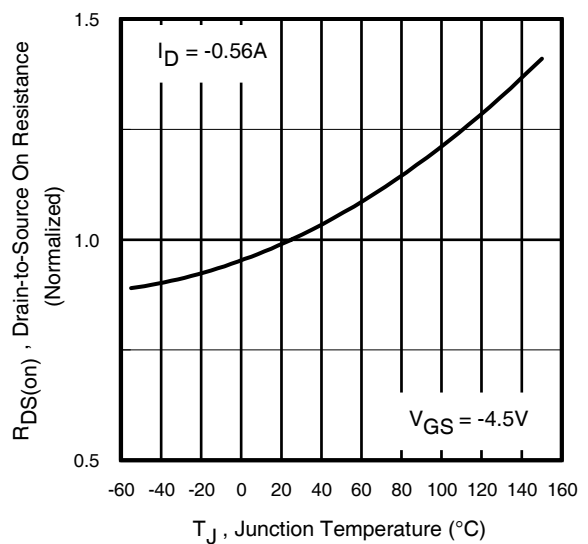


Fig 22. Normalized On-Resistance Vs. Temperature

P-Channel  
Q2,Q4

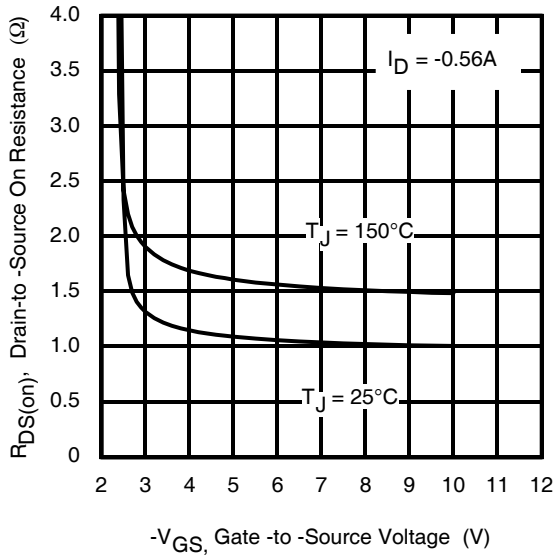


Fig 23. Typical On-Resistance Vs Gate Voltage

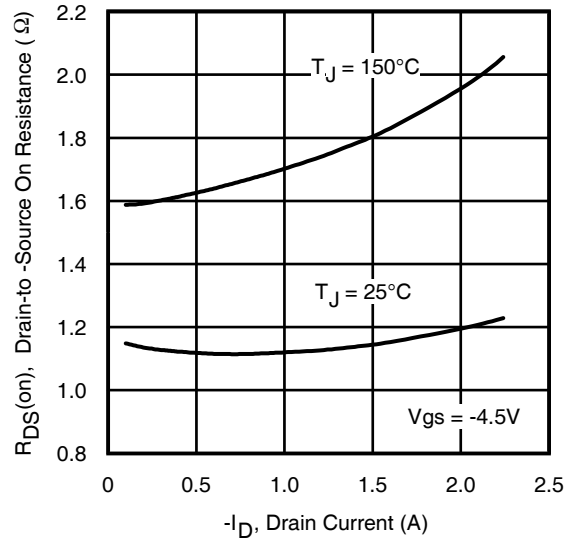


Fig 24. Typical On-Resistance Vs Drain Current

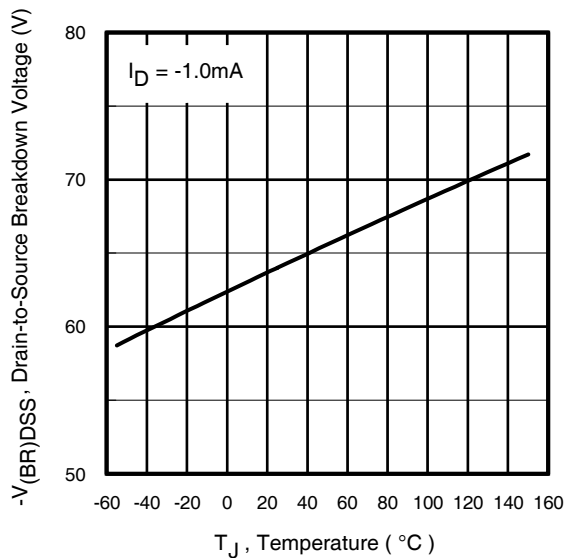


Fig 25. Typical Drain-to-Source Breakdown Voltage Vs Temperature

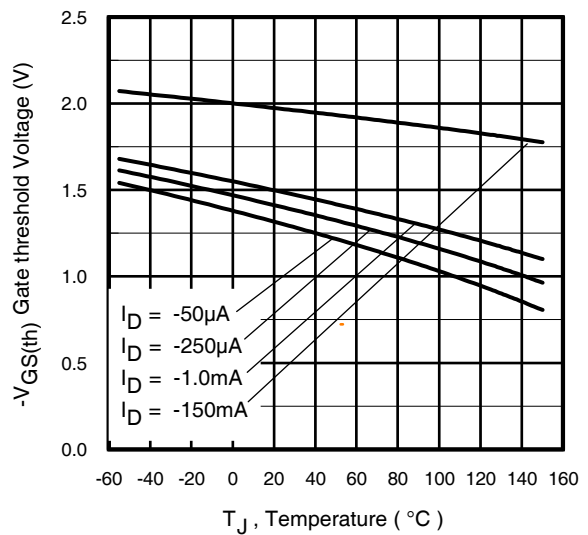


Fig 26. Typical Threshold Voltage Vs Temperature

P-Channel  
Q2,Q4

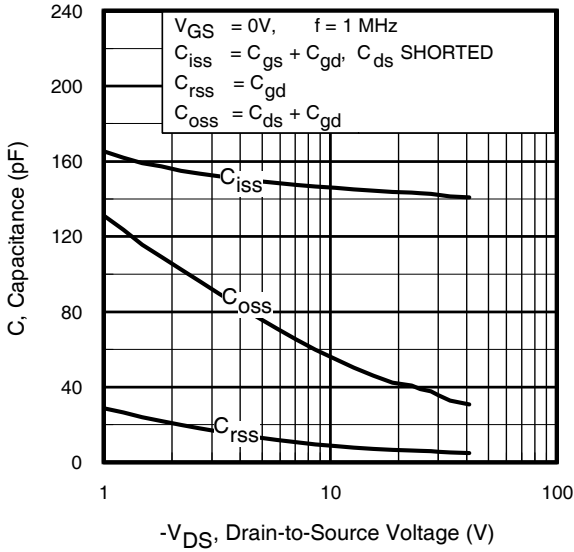


Fig 27. Typical Capacitance Vs. Drain-to-Source Voltage

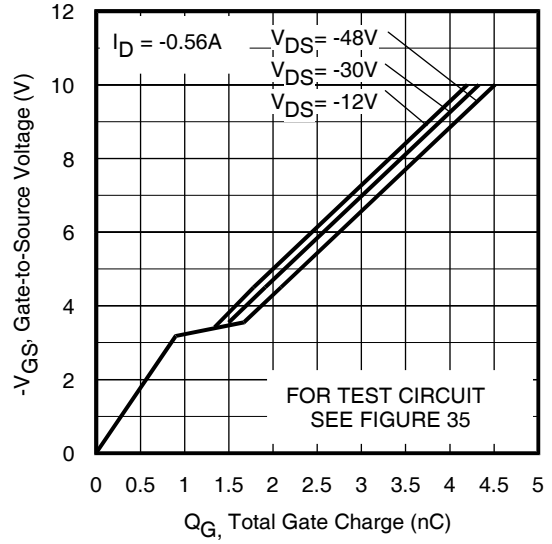


Fig 28. Typical Gate Charge Vs. Gate-to-Source Voltage

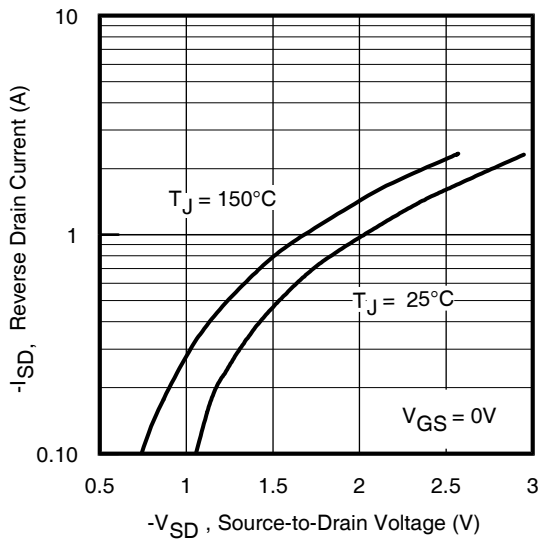


Fig 29. Typical Source-Drain Diode Forward Voltage

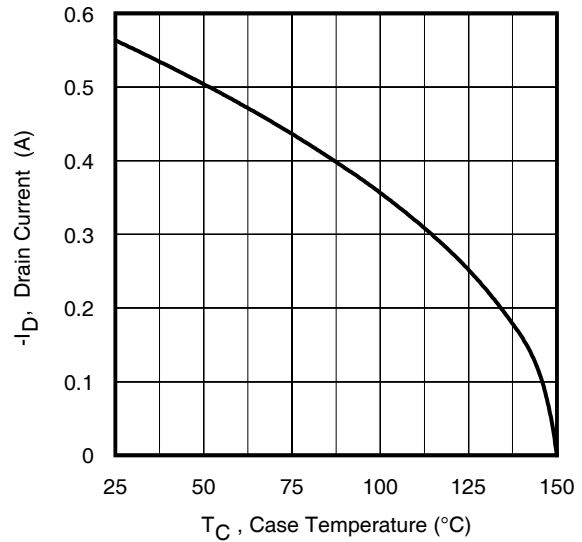


Fig 30. Maximum Drain Current Vs. Case Temperature

P-Channel  
Q2,Q4

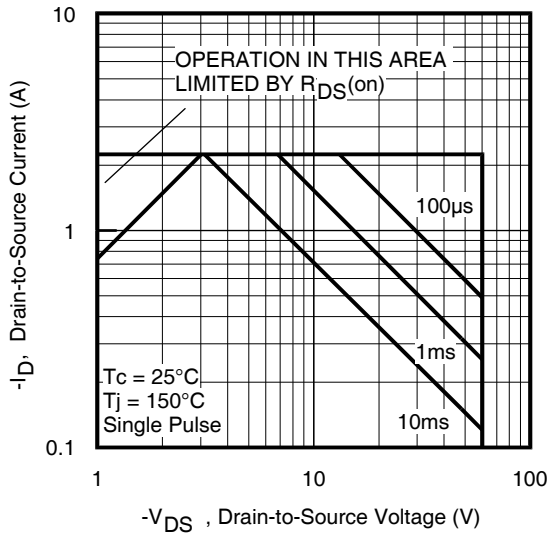


Fig 31. Maximum Safe Operating Area

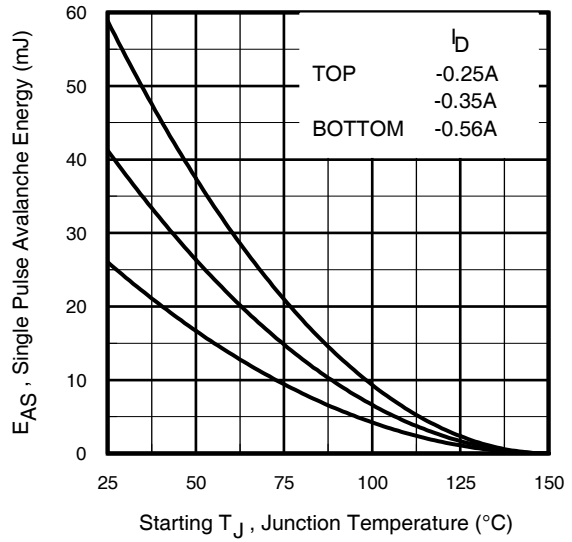


Fig 32. Maximum Avalanche Energy Vs. Drain Current

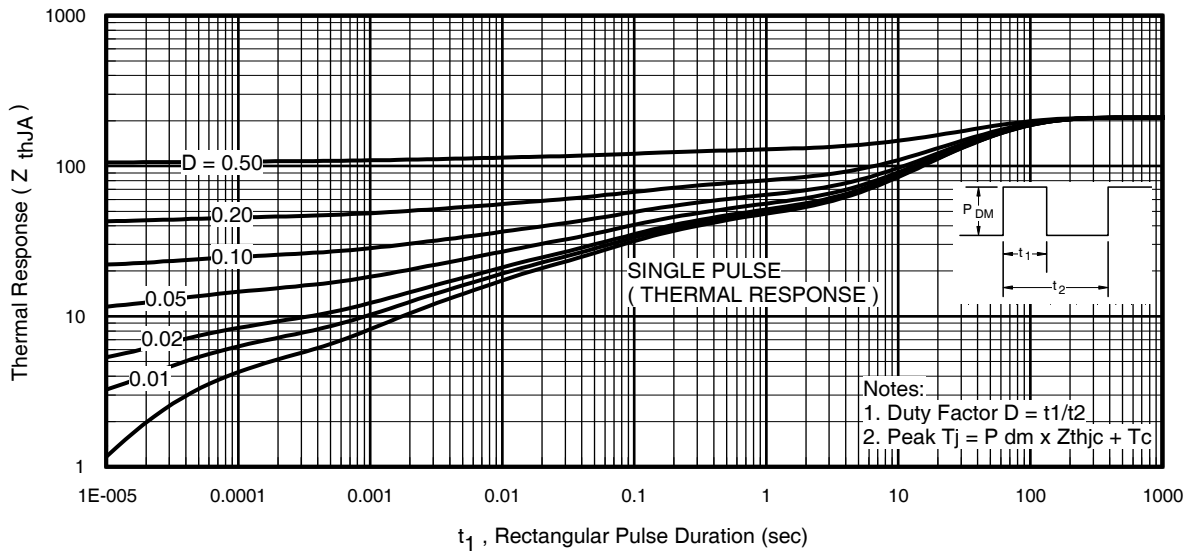


Fig 33. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Pre-Irradiation

IRHLA7670Z4, 2N7633M2

P-Channel  
Q2,Q4

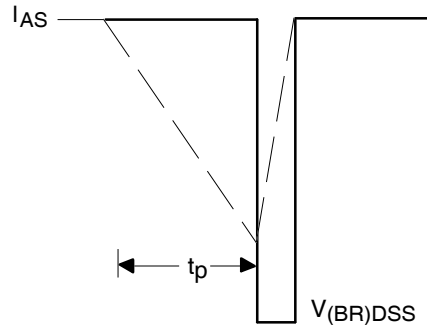
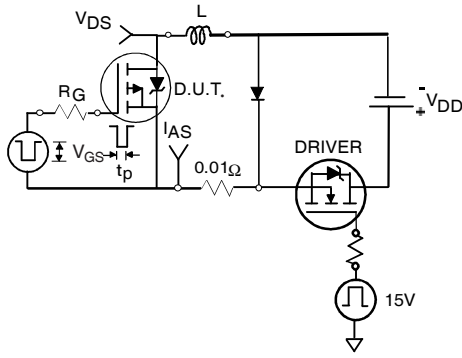


Fig 34a. Unclamped Inductive Test Circuit

Fig 34b. Unclamped Inductive Waveforms

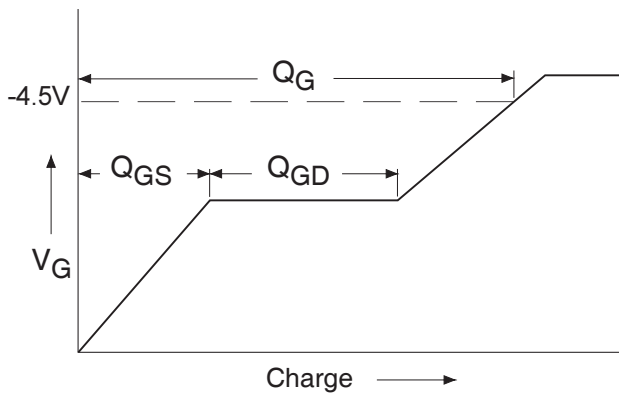


Fig 35a. Basic Gate Charge Waveform

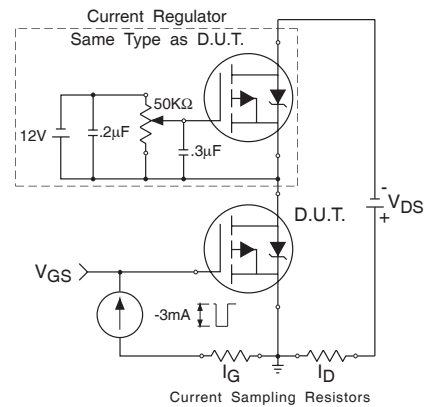


Fig 35b. Gate Charge Test Circuit

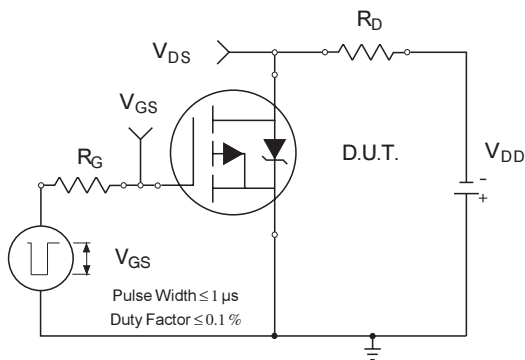


Fig 36a. Switching Time Test Circuit

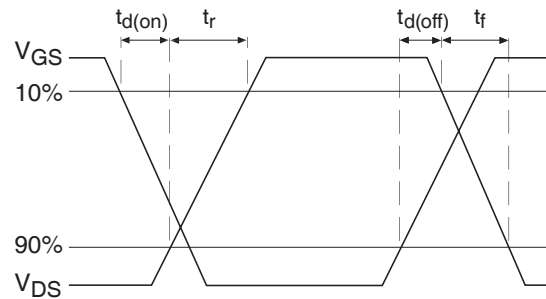


Fig 36b. Switching Time Waveforms

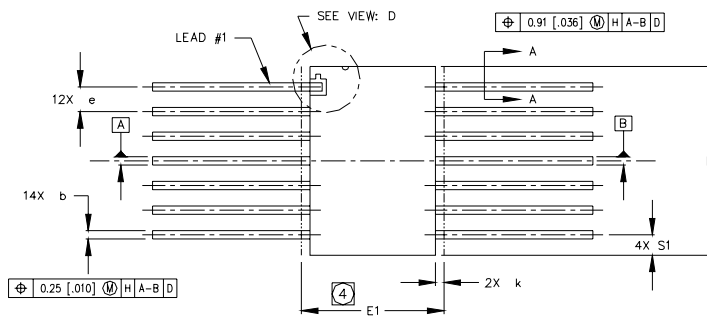
# IRHLA7670Z4, 2N7633M2

# Pre-Irradiation

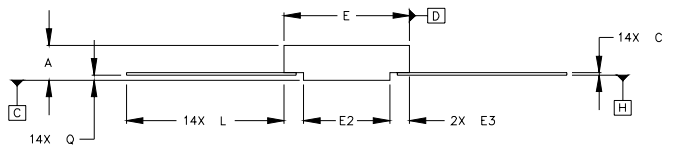
## Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ②  $V_{DD} = 25V$ , starting  $T_J = 25^\circ C$ ,  $L = 50mH$ , Peak  $I_L = 0.8A$ ,  $V_{GS} = 10V$
- ③  $I_{SD} \leq 0.8A$ ,  $di/dt \leq 230A/\mu s$ ,  $V_{DD} \leq 60V$ ,  $T_J \leq 150^\circ C$
- ④ Pulse width  $\leq 300 \mu s$ ; Duty Cycle  $\leq 2\%$
- ⑤ **Total Dose Irradiation with  $V_{GS}$  Bias.**  
 $\pm 10$  volt  $V_{GS}$  applied and  $V_{DS} = 0$  during irradiation per MIL-STD-750, method 1019, condition A
- ⑥ **Total Dose Irradiation with  $V_{DS}$  Bias.**  
 $\pm 48$  volt  $V_{DS}$  applied and  $V_{GS} = 0$  during irradiation per MIL-STD-750, method 1019, condition A
- ⑦  $V_{DD} = -25V$ , starting  $T_J = 25^\circ C$ ,  $L = 166mH$ , Peak  $I_L = -0.56A$ ,  $V_{GS} = -10V$
- ⑧  $I_{SD} \leq -0.56A$ ,  $di/dt \leq -161A/\mu s$ ,  $V_{DD} \leq -60V$ ,  $T_J \leq 150^\circ C$

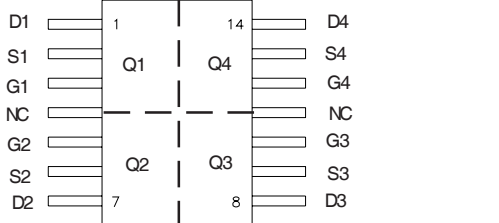
## Case Outline and Dimensions — 14 Lead FlatPack



SYMBOL	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.14	2.92	.045	.115
b	0.38	0.56	.015	.022
b1	0.38	0.48	.015	.019
c	0.10	0.23	.004	.009
c1	0.10	0.15	.004	.006
D	---	9.91	---	.390
E	5.97	6.60	.235	.260
E1	---	7.37	---	.290
E2	3.18	---	.125	---
E3	0.76	---	.030	---
e	1.27	BSC	.050	BSC
k	0.20	0.38	.008	.015
L	6.86	9.40	.270	.370
Q	0.18	0.33	.007	.013
S1	0.13	---	.005	---
M	---	0.04	---	.0015



### LEAD ASSIGNMENT

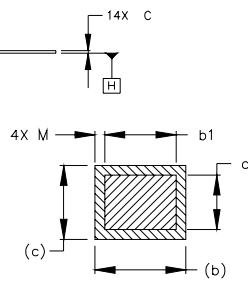


### LEGEND

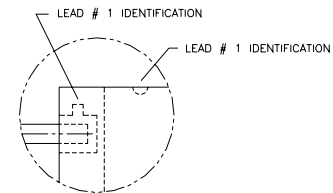
D = DRAIN, S = SOURCE, G = GATE, NC = NO CONNECTION

### CHANNELS

N Channel = Q1 and Q3, P Channel = Q2 and Q4



### SECTION A-A



### VIEW D

LOCATION OF LEAD #1 IDENTIFICATION MARKS

### NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- ④ THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. OUTLINE CONFORMS TO MIL-STD-1835C, OUTLINE CDFP3-F14 EXCEPT FOR DIMENSION Q.

International  
**IR** Rectifier

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TAC Fax: (310) 252-7903

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Data and specifications subject to change without notice. 03/2008

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