

**RADIATION HARDENED
 LOGIC LEVEL POWER MOSFET
 THRU-HOLE (14-LEAD FLAT PACK)**

**2N7630M2
 IRHLA7970Z4
 60V, Quad P-CHANNEL
 R7™ TECHNOLOGY**

Product Summary

Part Number	Radiation Level	RDS(on)	ID
IRHLA7970Z4	100K Rads (Si)	1.36Ω	-0.56A
IRHLA7930Z4	300K Rads (Si)	1.36Ω	-0.56A



International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity. These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

Features:

- 5V CMOS and TTL Compatible
- Low RDS(on)
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight
- Complimentary N-Channel Available - IRHLA770Z4

Absolute Maximum Ratings (Per Die)

Pre-Irradiation

	Parameter		Units
ID @ VGS = -4.5V, TC=25°C	Continuous Drain Current	-0.56	A
ID @ VGS = -4.5V, TC=100°C	Continuous Drain Current	-0.35	
IDM	Pulsed Drain Current ①	-2.24	
PD @ TC = 25°C	Max. Power Dissipation	0.6	W
	Linear Derating Factor	0.005	W/°C
VGS	Gate-to-Source Voltage	±10	V
EAS	Single Pulse Avalanche Energy ②	26	mJ
IAR	Avalanche Current ①	-0.56	A
EAR	Repetitive Avalanche Energy ①	0.06	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.79	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.63 in./1.6 mm from case for 10s)	
	Weight	0.52 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics For Each P-Channel Device @T_j = 25°C (Unless Otherwise specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
B _V D _{SS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔB _V D _{SS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	-0.063	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	1.36	Ω	V _{GS} = -4.5V, I _D = -0.35A ^④
V _{GS(th)}	Gate Threshold Voltage	-1.0	—	-2.0	V	V _{DS} = V _{GS} , I _D = -250μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	3.2	—	mV/°C	
g _{fs}	Forward Transconductance	0.7	—	—	S	V _{DS} = -10V, I _{DS} = -0.35A ^④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	μA	V _{DS} = -48V, V _{GS} = 0V
		—	—	-10		V _{DS} = -48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V _{GS} = 10V
Q _g	Total Gate Charge	—	—	2.8	nC	V _{GS} = -4.5V, I _D = -0.56A
Q _{gs}	Gate-to-Source Charge	—	—	1.7		V _{DS} = -30V
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	1.2		
t _{d(on)}	Turn-On Delay Time	—	—	22	ns	V _{DD} = -30V, I _D = -0.56A, V _{GS} = -5.0V, R _G = 24Ω
t _r	Rise Time	—	—	22		
t _{d(off)}	Turn-Off Delay Time	—	—	40		
t _f	Fall Time	—	—	32		
L _S + L _D	Total Inductance	—	20	—	nH	Measured from Drain lead (6mm /0.25in from pack.) to Source lead (6mm/0.25in from pack.)with Source wire internally bonded from Source pin to Drain pad
C _{iss}	Input Capacitance	—	144	—	pF	V _{GS} = 0V, V _{DS} = -25V f = 1.0MHz
C _{oss}	Output Capacitance	—	41	—		
C _{rss}	Reverse Transfer Capacitance	—	6.6	—		
R _g	Gate Resistance	—	55	—		

Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-0.56	A	
I _{SM}	Pulse Source Current (Body Diode) ^①	—	—	-2.24		
V _{SD}	Diode Forward Voltage	—	—	-5.0	V	T _j = 25°C, I _S = -0.56A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	—	35	ns	T _j = 25°C, I _F = -0.56A, di/dt ≤ -100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	9.6	nC	V _{DD} ≤ -25V ^④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJA}	Junction-to-Ambient	—	—	210	°C/W	Typical socket mount

Note: Corresponding Spice and Saber models are available International Rectifier Website.

For footnotes refer to the last page

Radiation Characteristics

IRHLA7970Z4, 2N7630M2

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics For Each P-Channel Device @Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 300K Rads (Si) ¹		Units	Test Conditions
		Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	-60	—	V	V _{GS} = 0V, I _D = -250μA
V _{GS(th)}	Gate Threshold Voltage	-1.0	-2.0		V _{GS} = V _{DS} , I _D = -250μA
I _{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	V _{GS} = -10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	100		V _{GS} = 10V
I _{DSS}	Zero Gate Voltage Drain Current	—	-1.0	μA	V _{DS} = -48V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source On-State Resistance (TO-39)	—	1.25	Ω	V _{GS} = -4.5V, I _D = -0.35A
R _{DS(on)}	Static Drain-to-Source On-state Resistance (14-Lead Flat Pack)	—	1.36	Ω	V _{GS} = -4.5V, I _D = -0.35A
V _{SD}	Diode Forward Voltage ④	—	-5.0	V	V _{GS} = 0V, I _D = -0.56A

1. Part numbers IRHLA7970Z4, IRHLA7930Z4

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area (Per Die)

Ion	LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)							
				@VGS= 0V	@VGS= 2V	@VGS= 4V	@VGS= 5V	@VGS= 6V	@VGS= 7V	@VGS= 8V	@VGS= 10V
Br	37	305	39	-60	-60	-60	-60	-60	-50	-35	-25
I	60	370	34	-60	-60	-60	-60	-60	-20	-	-
Au	84	390	30	-60	-60	-60	-60	-	-	-	-

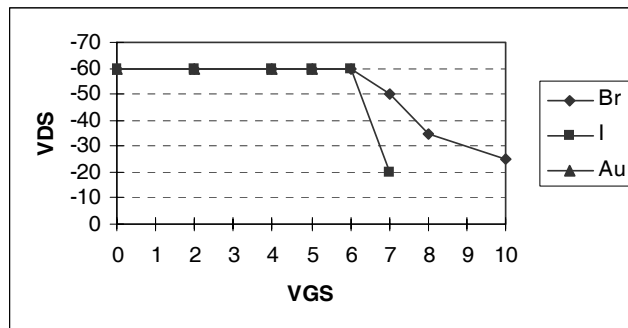


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the last page

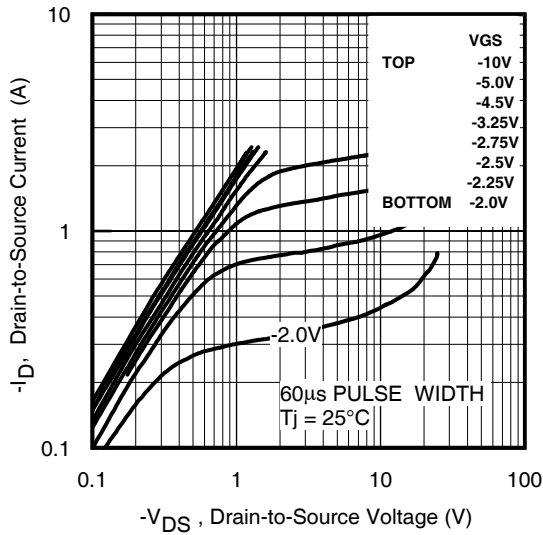


Fig 1. Typical Output Characteristics

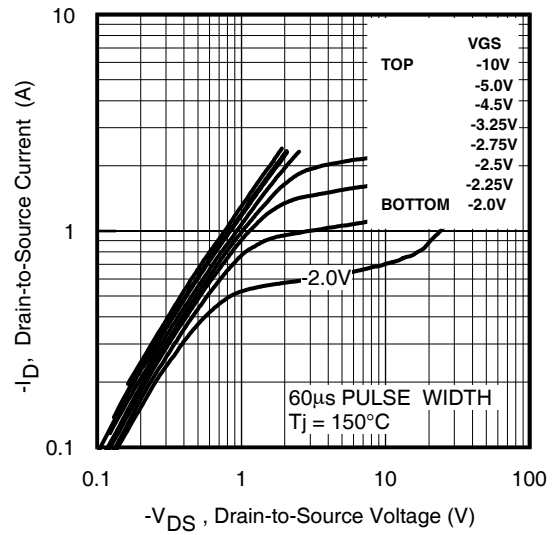


Fig 2. Typical Output Characteristics

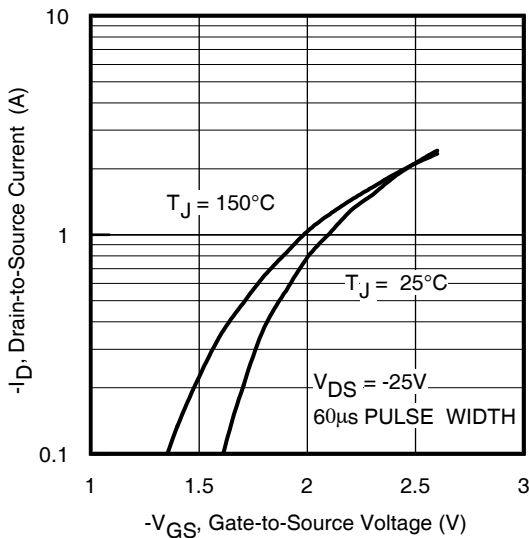


Fig 3. Typical Transfer Characteristics

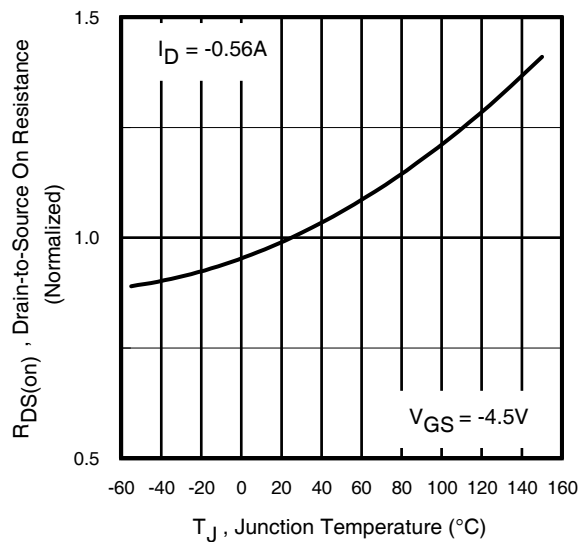


Fig 4. Normalized On-Resistance Vs. Temperature

Pre-Irradiation

IRHLA7970Z4, 2N7630M2

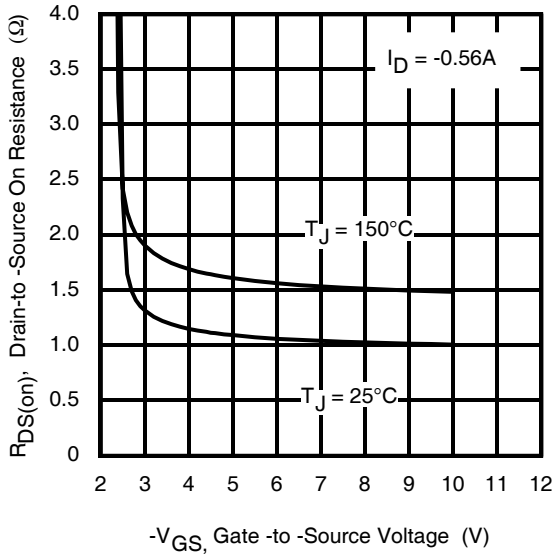


Fig 5. Typical On-Resistance Vs Gate Voltage

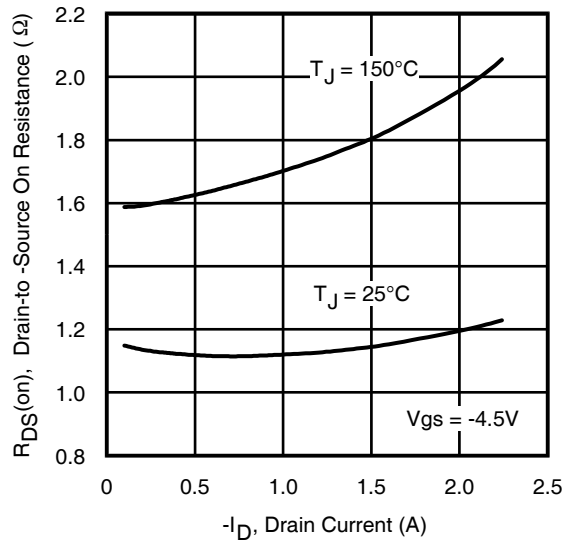


Fig 6. Typical On-Resistance Vs Drain Current

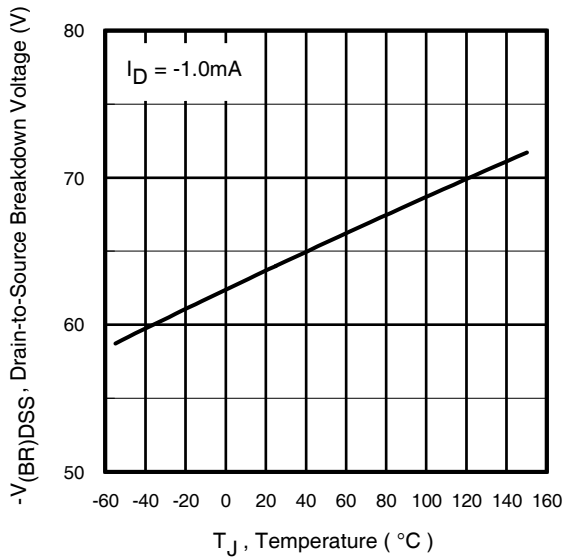


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

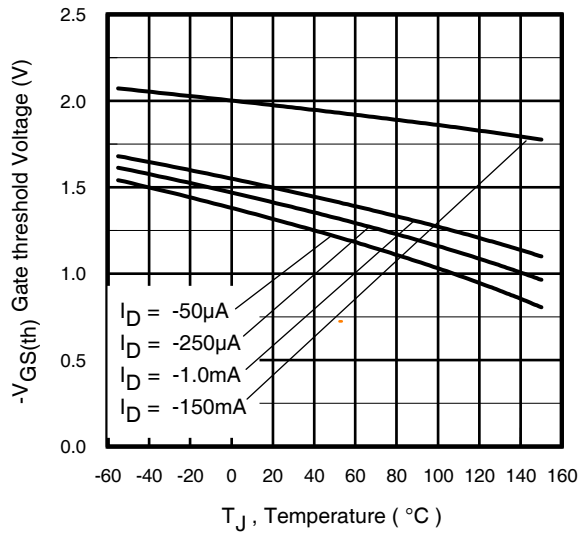


Fig 8. Typical Threshold Voltage Vs Temperature

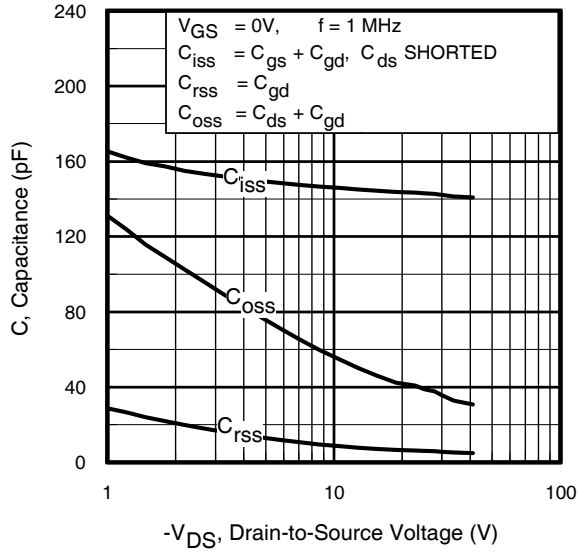


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

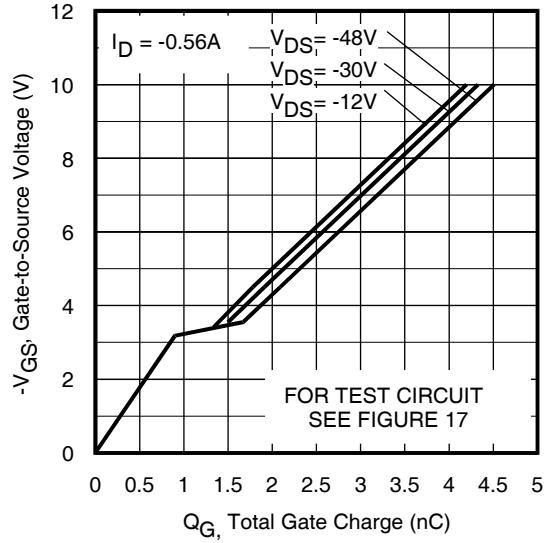


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

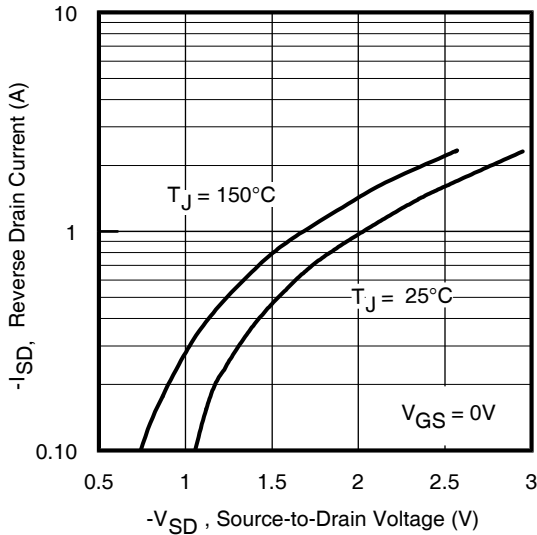


Fig 11. Typical Source-Drain Diode Forward Voltage

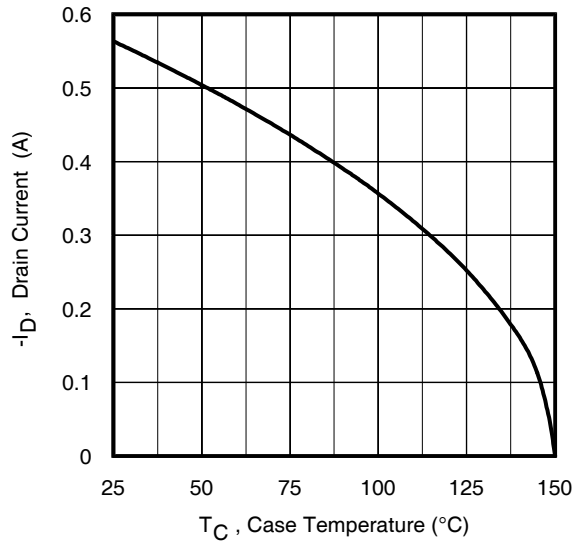


Fig 12. Maximum Drain Current Vs. Case Temperature

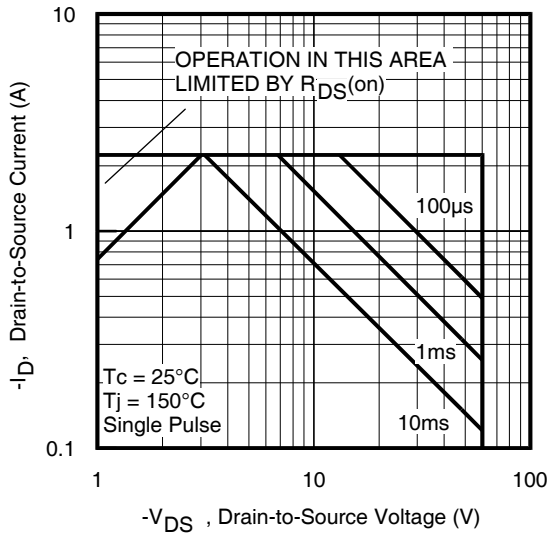


Fig 13. Maximum Safe Operating Area

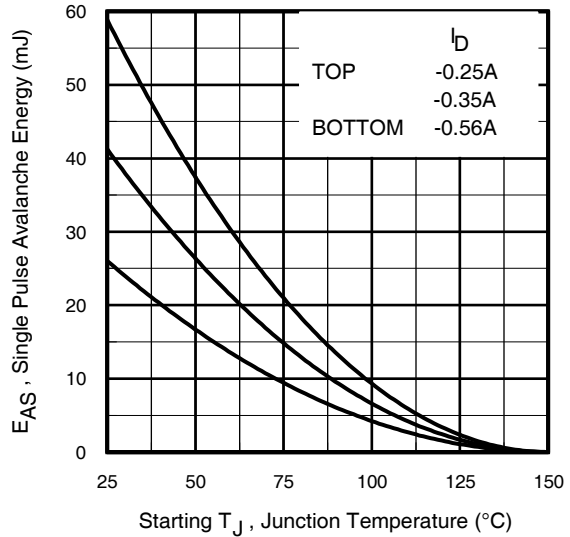


Fig 14. Maximum Avalanche Energy Vs. Drain Current

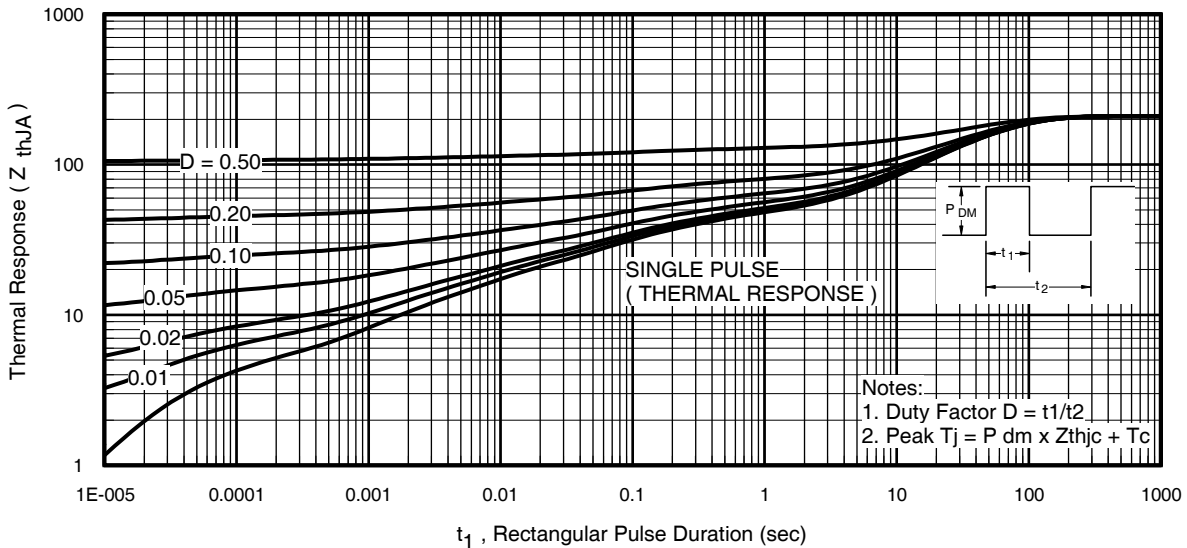


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

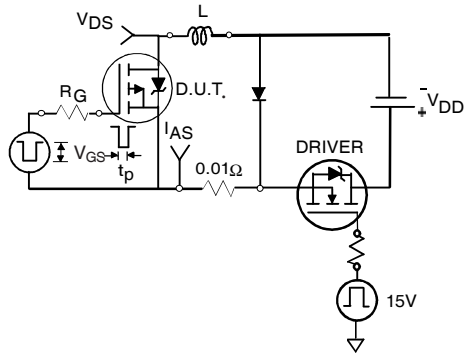


Fig 16a. Unclamped Inductive Test Circuit

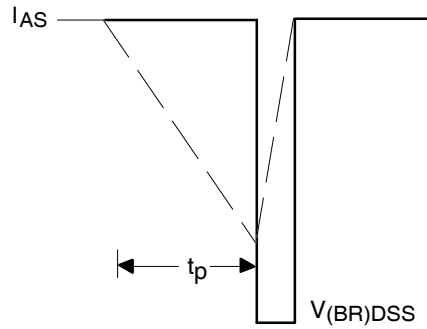


Fig 16b. Unclamped Inductive Waveforms

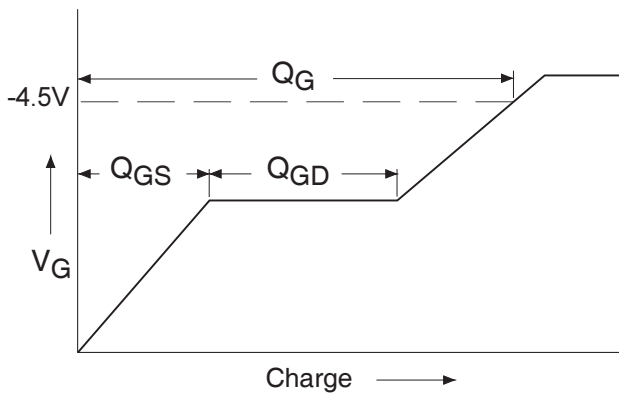


Fig 17a. Basic Gate Charge Waveform

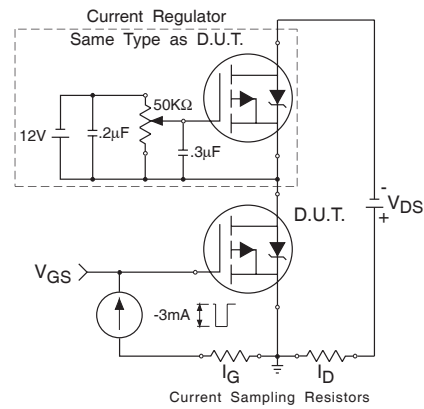


Fig 17b. Gate Charge Test Circuit

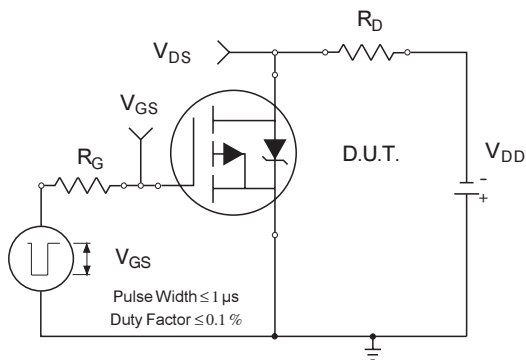


Fig 18a. Switching Time Test Circuit

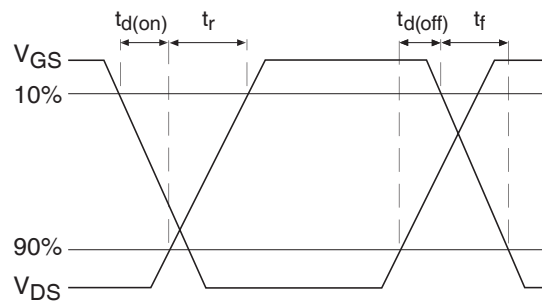


Fig 18b. Switching Time Waveforms

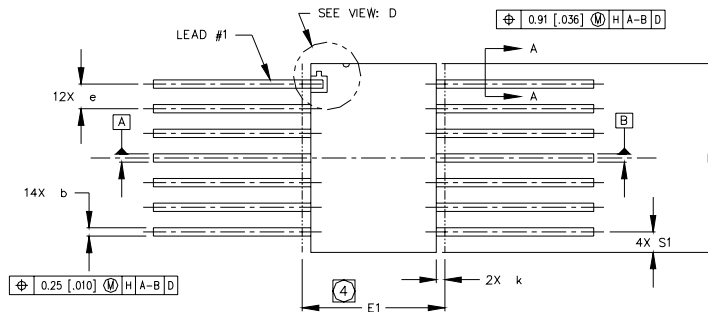
Pre-Irradiation

IRHLA7970Z4, 2N7630M2

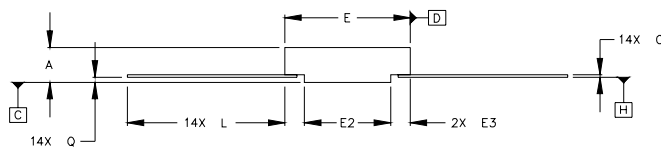
Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -25V$, starting $T_J = 25^\circ C$, $L = 166mH$
Peak $I_L = -0.56A$, $V_{GS} = -10V$
- ③ $I_{SD} \leq -0.56A$, $di/dt \leq -161A/\mu s$,
 $V_{DD} \leq -60V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
-10 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
-48 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

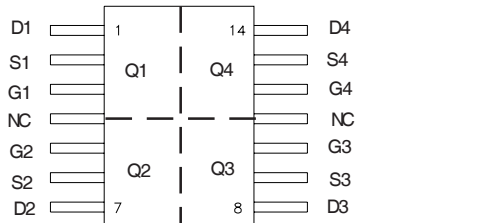
Case Outline and Dimensions — 14-Lead Flat Pack



SYMBOL	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.14	2.92	.045	.115
b	0.38	0.56	.015	.022
b1	0.38	0.48	.015	.019
c	0.10	0.23	.004	.009
c1	0.10	0.15	.004	.006
D	---	9.91	---	.390
E	5.97	6.60	.235	.260
E1	---	7.37	---	.290
E2	3.18	---	.125	---
E3	0.76	---	.030	---
e	1.27	BSC	.050	BSC
k	0.20	0.38	.008	.015
L	6.86	9.40	.270	.370
Q	0.18	0.33	.007	.013
S1	0.13	---	.005	---
M	---	0.04	---	.0015



LEAD ASSIGNMENT

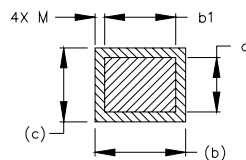


LEGEND

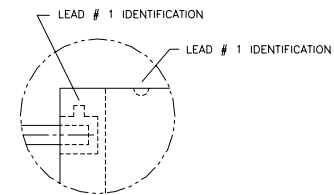
D = DRAIN, S = SOURCE, G = GATE, NC = NO CONNECTION

CHANNELS

P Channel = Q1, Q2, Q3 and Q4



SECTION A-A



VIEW D
LOCATION OF LEAD #1 IDENTIFICATION MARKS

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- ④ THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. OUTLINE CONFORMS TO MIL-STD-1835C, OUTLINE CDFP3-F14 EXCEPT FOR DIMENSION Q.

International
IR Rectifier

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Data and specifications subject to change without notice. 03/2008