

**RADIATION HARDENED
LOGIC LEVEL POWER MOSFET
SURFACE MOUNT (LCC-6)**

2N7627UC
IRHLUC7970Z4
60V, DUAL P-CHANNEL
TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	Id
IRHLUC7970Z4	100K Rads (Si)	1.60Ω	-0.65A
IRHLUC7930Z4	300K Rads (Si)	1.60Ω	-0.65A

International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.



Features:

- 5V CMOS and TTL Compatible
- Low RDS(on)
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight
- Complimentary N-Channel Available - IRHLUC770Z4

Absolute Maximum Ratings (Per Die)

Pre-Irradiation

	Parameter		Units
Id @ VGS = -4.5V, TC = 25°C	Continuous Drain Current	-0.65	A
Id @ VGS = -4.5V, TC = 100°C	Continuous Drain Current	-0.41	
IDM	Pulsed Drain Current ①	-2.6	
PD @ TC = 25°C	Max. Power Dissipation	1.0	W
	Linear Derating Factor	0.01	W/°C
VGS	Gate-to-Source Voltage	±10	V
EAS	Single Pulse Avalanche Energy ②	34	mJ
IAR	Avalanche Current ①	-0.65	A
EAR	Repetitive Avalanche Energy ①	0.1	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.6	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Pckg. Mounting SurfaceTemp	300 (for 5s)	
	Weight	0.2 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics For P-Channel Die @T_j = 25°C (Unless Otherwise specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	-0.06	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	1.60	Ω	V _{GS} = -4.5V, I _D = -0.41A ④
V _{GS(th)}	Gate Threshold Voltage	-1.0	—	-2.0	V	V _{DS} = V _{GS} , I _D = -250μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	3.6	—	mV/°C	
g _{fs}	Forward Transconductance	0.5	—	—	S	V _{DS} = -10V, I _{DS} = -0.41A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	μA	V _{DS} = -48V, V _{GS} = 0V
		—	—	-10		V _{DS} = -48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V _{GS} = 10V
Q _g	Total Gate Charge	—	—	3.6	nC	V _{GS} = -4.5V, I _D = -0.65A
Q _{gs}	Gate-to-Source Charge	—	—	1.5		V _{DS} = -30V
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	1.8		
t _{d(on)}	Turn-On Delay Time	—	—	23	ns	V _{DD} = -30V, I _D = -0.65A,
t _r	Rise Time	—	—	22		V _{GS} = -5.0V, R _G = 24Ω
t _{d(off)}	Turn-Off Delay Time	—	—	32		
t _f	Fall Time	—	—	26		
L _S + L _D	Total Inductance	—	33	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	147	—	pF	V _{GS} = 0V, V _{DS} = -25V
C _{oss}	Output Capacitance	—	46	—		f = 1.0MHz
C _{rss}	Reverse Transfer Capacitance	—	8.1	—		
R _g	Gate Resistance	—	52	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics (Per P Channel Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-0.65	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	-2.6		
V _{SD}	Diode Forward Voltage	—	—	-5.0	V	T _j = 25°C, I _S = -0.65A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	35	ns	T _j = 25°C, I _F = -0.65A, di/dt ≤ -100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	9.8	nC	V _{DD} ≤ -25V ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance (Per P Channel Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJA}	Junction-to-Ambient	—	—	125	°C/W	Typical socket mount

Note: Corresponding Spice and Saber models are available on International Rectifier Website.

For footnotes refer to the last page

Radiation Characteristics

IRHLUC7970Z4, 2N7627UC

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics For P-Channel Device @Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Upto 300K Rads (Si) ¹		Units	Test Conditions
		Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	-60	—	V	V _{GS} = 0V, I _D = -250μA
V _{GS(th)}	Gate Threshold Voltage	-1.0	-2.0		V _{GS} = V _{DSS} , I _D = -250μA
I _{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	V _{GS} = -10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	100		V _{GS} = 10V
I _{DSS}	Zero Gate Voltage Drain Current	—	-1.0	μA	V _{DS} = -48V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	1.40	Ω	V _{GS} = -4.5V, I _D = -0.41A
R _{DS(on)}	Static Drain-to-Source On-state ④ Resistance (LCC-6)	—	1.60	Ω	V _{GS} = -4.5V, I _D = -0.41A
V _{SD}	Diode Forward Voltage ④	—	-5.0	V	V _{GS} = 0V, I _D = -0.65A

1. Part numbers IRHLUC7970Z4, IRHLUC7930Z4

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)					
			@VGS= 0V	@VGS= 2V	@VGS= 4V	@VGS= 5V	@VGS= 6V	@VGS= 7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	-60	-60	-60	-60	-60	-50
62 ± 5%	355 ± 7.5%	33 ± 7.5%	-60	-60	-60	-60	-60	-
85 ± 5%	380 ± 7.5%	29 ± 7.5%	-60	-60	-60	-60	-	-

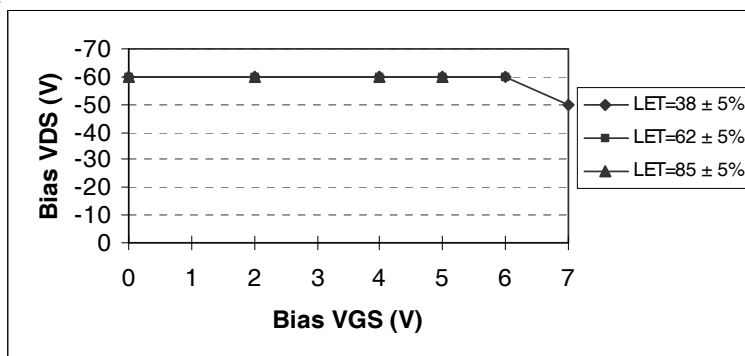
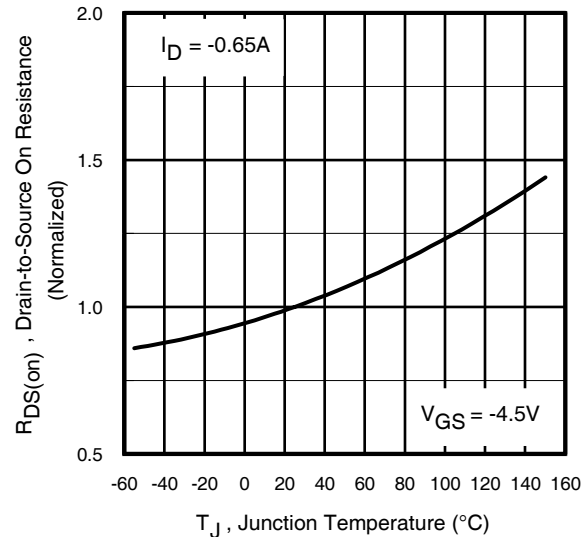
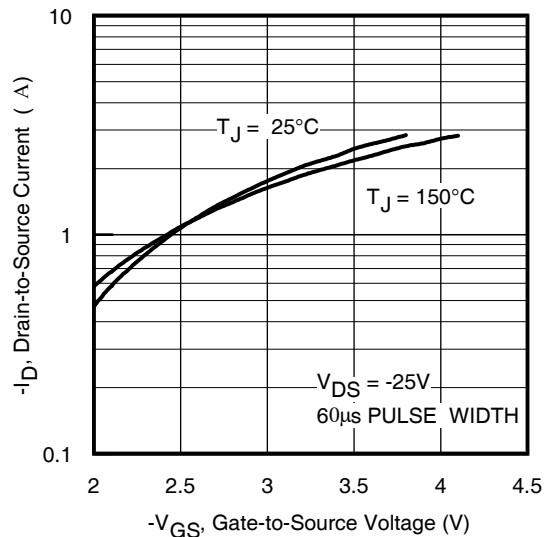
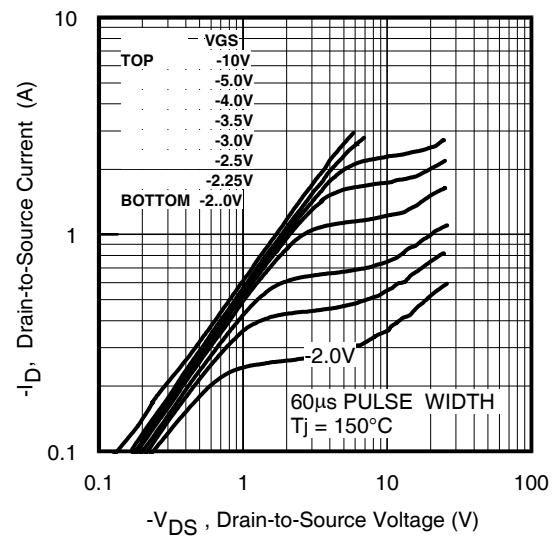
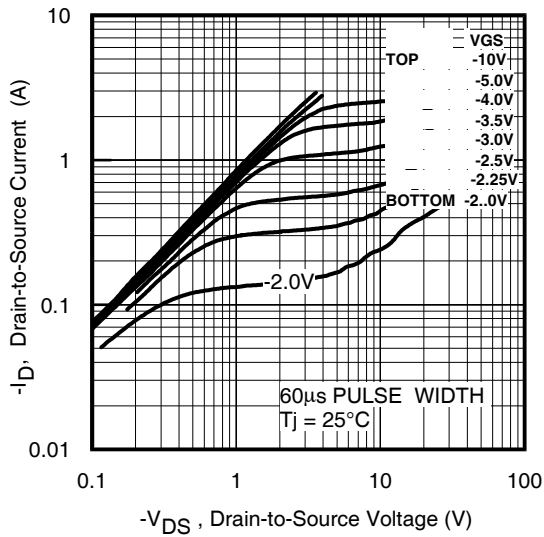


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the last page



Pre-Irradiation

IRHLUC7970Z4, 2N7627UC

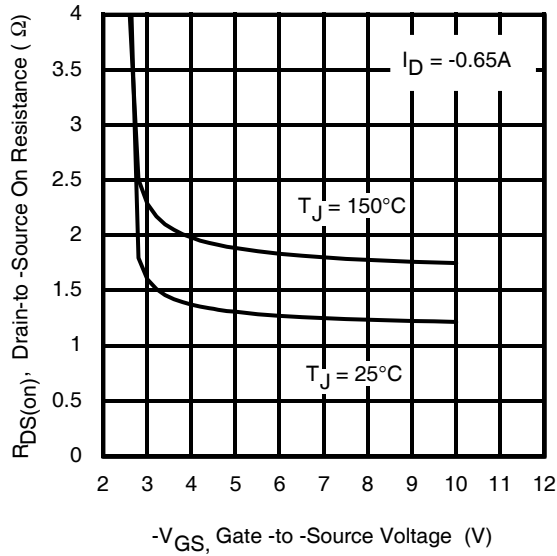


Fig 5. Typical On-Resistance Vs Gate Voltage

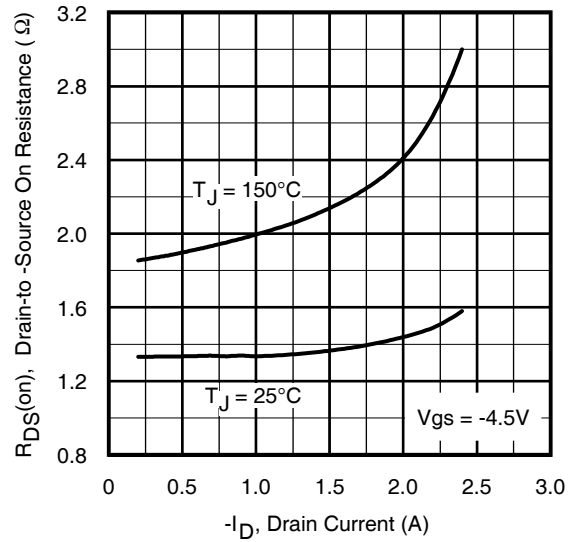


Fig 6. Typical On-Resistance Vs Drain Current

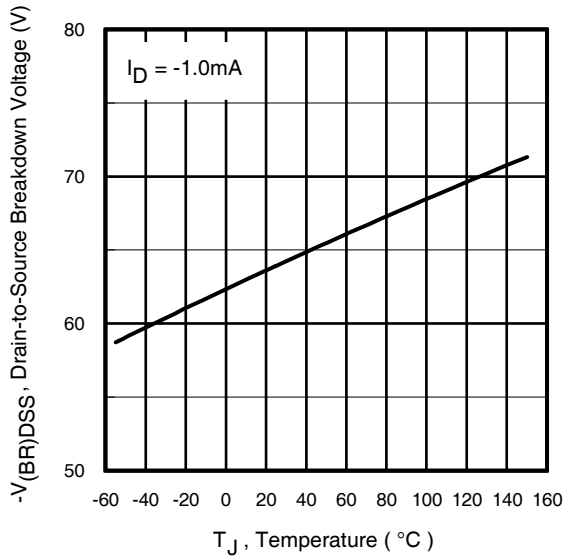


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

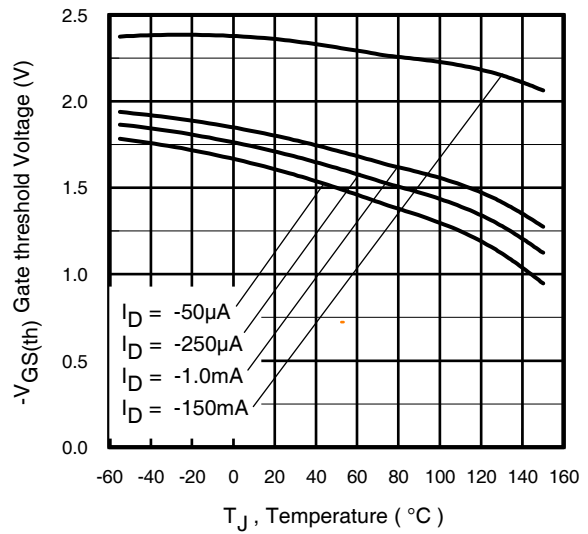


Fig 8. Typical Threshold Voltage Vs Temperature

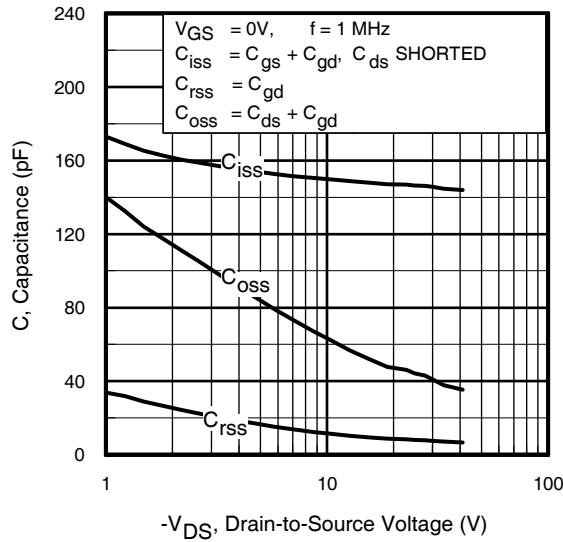


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

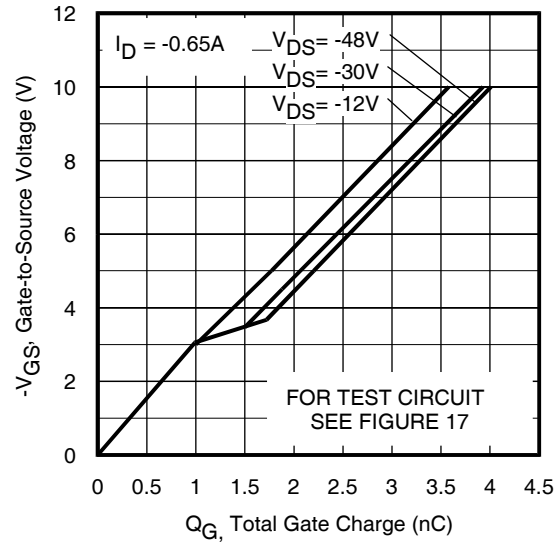


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

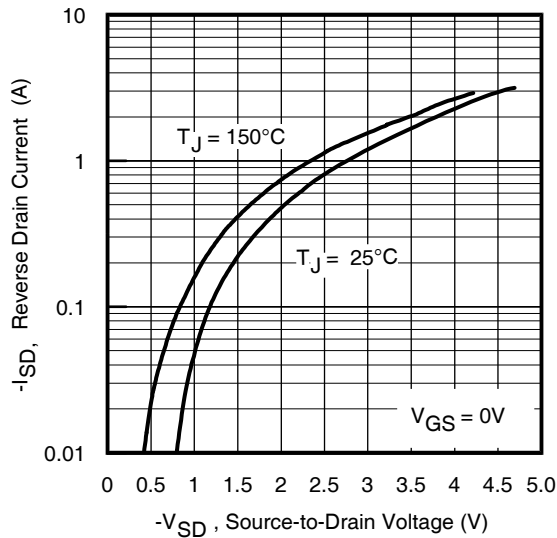


Fig 11. Typical Source-Drain Diode Forward Voltage

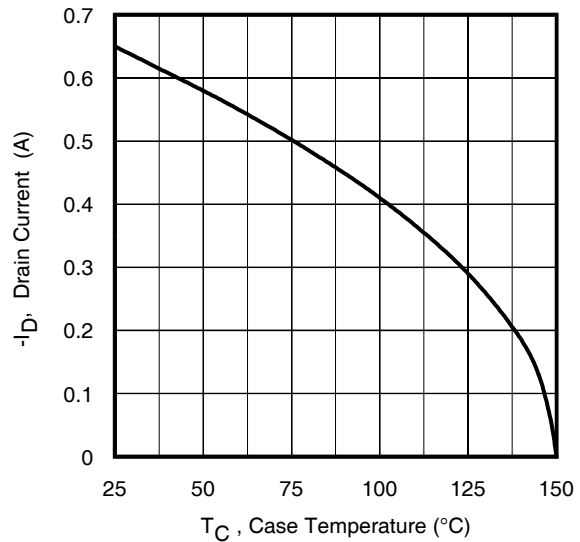


Fig 12. Maximum Drain Current Vs. Case Temperature

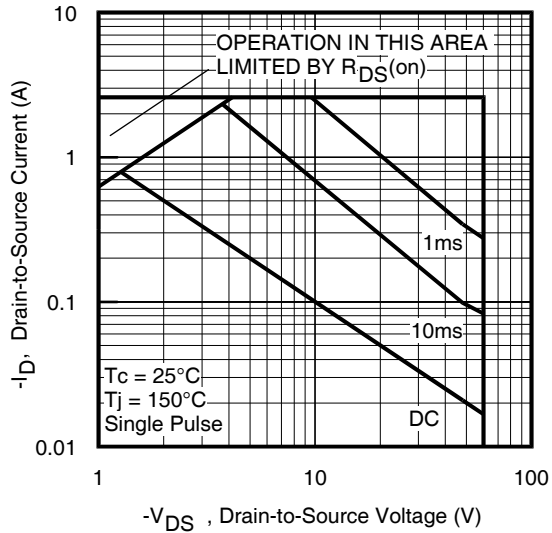


Fig 13. Maximum Safe Operating Area

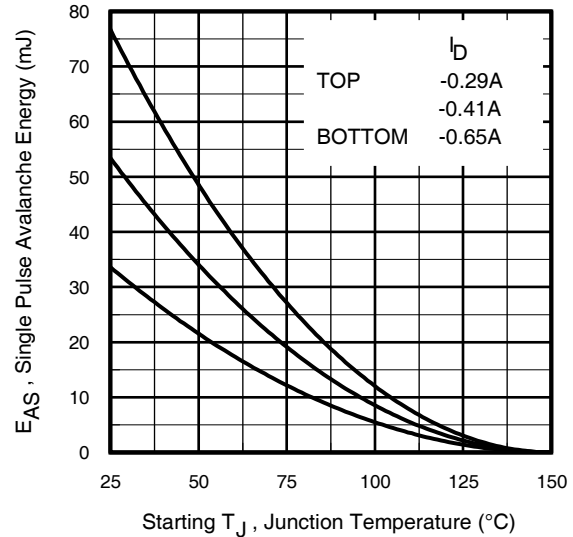


Fig 14. Maximum Avalanche Energy Vs. Drain Current

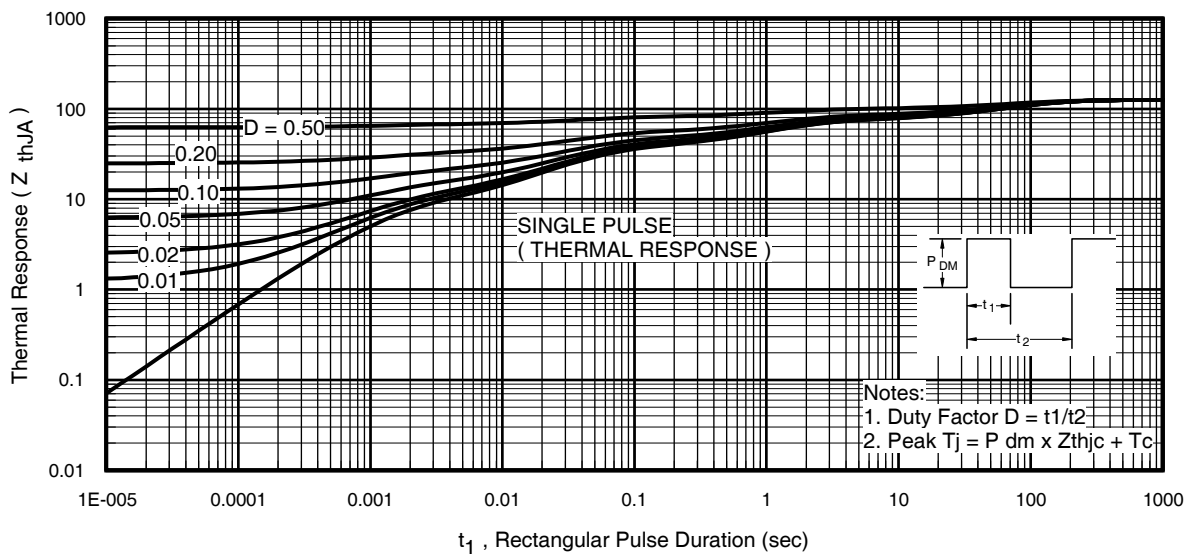


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

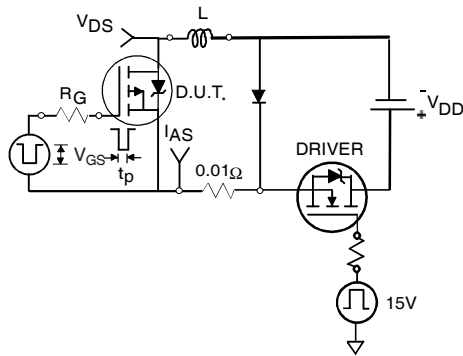


Fig 16a. Unclamped Inductive Test Circuit

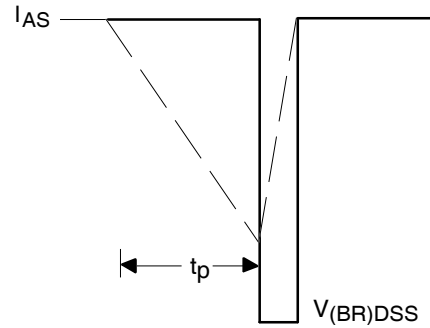


Fig 16b. Unclamped Inductive Waveforms

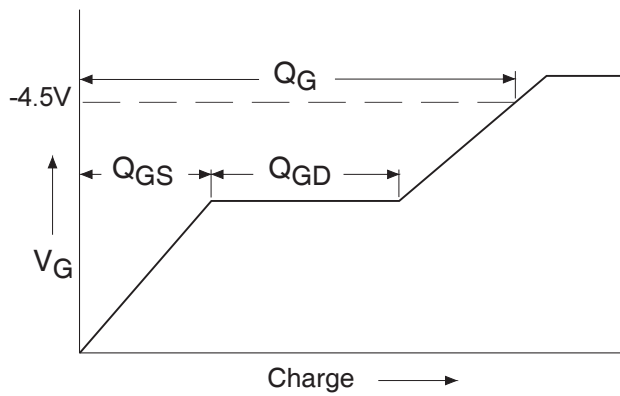


Fig 17a. Basic Gate Charge Waveform

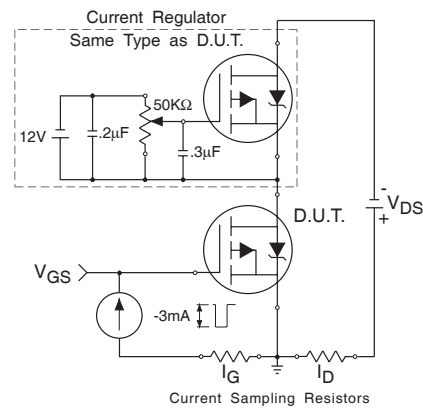


Fig 17b. Gate Charge Test Circuit

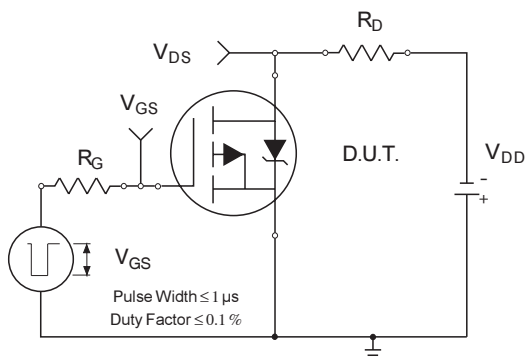


Fig 18a. Switching Time Test Circuit

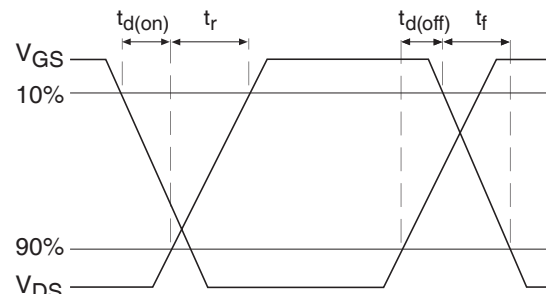


Fig 18b. Switching Time Waveforms

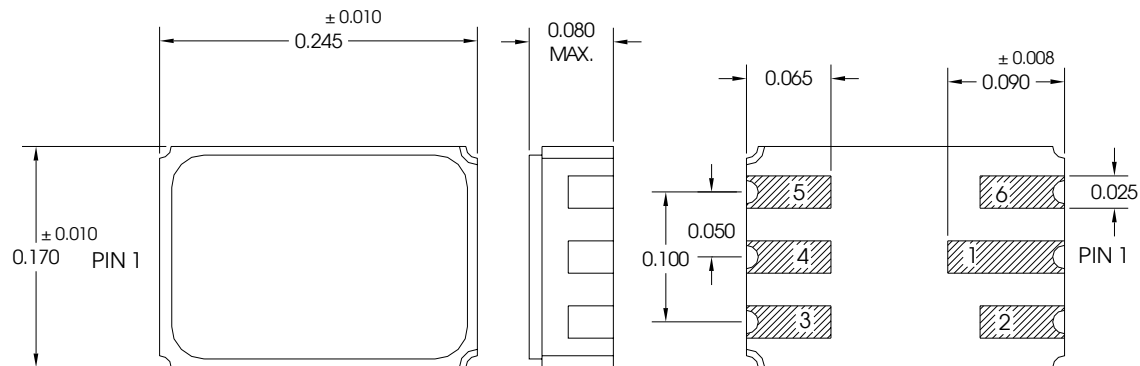
Pre-Irradiation

IRHLUC7970Z4, 2N7627UC

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -25V$, starting $T_J = 25^\circ C$, $L = 161mH$, Peak $I_L = -0.65A$, $V_{GS} = -10V$
- ③ $I_{SD} \leq -0.65A$, $di/dt \leq -150A/\mu s$, $V_{DD} \leq -60V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
-10volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
-48 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A

Case Outline and Dimensions — LCC-6



NOTES:

1. OUTLINE CONFORMS TO MIL-PRF-19500/255L
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. CONTROLLING DIMENSION: INCH.

DIE 1 & 2 (P Ch)

PIN NAME	PIN #
DRAIN	- 1 & 4
GATE	- 2 & 5
SOURCE	- 6 & 3

International
IOR Rectifier

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Data and specifications subject to change without notice. 10/2010