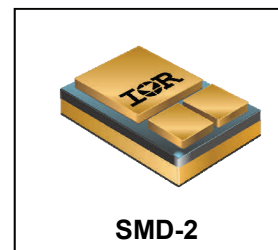


**RADIATION HARDENED  
POWER MOSFET  
SURFACE MOUNT (SMD-2)**

**100V, P-CHANNEL**  
**REF: MIL-PRF-19500/713**  
**R5 TECHNOLOGY**

**Product Summary**

Part Number	Radiation Level	RDS(on)	I <sub>D</sub>	QPL Part Number
IRHNA597160	100 kRads(Si)	0.049Ω	-47A	JANSR2N7550U2
IRHNA593160	300 kRads(Si)	0.049Ω	-47A	JANSF2N7550U2



**Description**

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm<sup>2</sup>)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

**Features**

- Single Event Effect (SEE) Hardened
- Ultra Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight

**Absolute Maximum Ratings**

**Pre-Irradiation**

Symbol	Parameter	Value	Units
I <sub>D1</sub> @ V <sub>GS</sub> = -12V, T <sub>C</sub> = 25°C	Continuous Drain Current	-47	A
I <sub>D2</sub> @ V <sub>GS</sub> = -12V, T <sub>C</sub> = 100°C	Continuous Drain Current	-30	
I <sub>DM</sub> @ T <sub>C</sub> = 25°C	Pulsed Drain Current ①	-188	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	400	mJ
I <sub>AR</sub>	Avalanche Current ①	-47	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-10	V/ns
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (for 5sec)	
	Weight	3.3 (Typical)	

For Footnotes, refer to the page 2.

**Electrical Characteristics @ T<sub>J</sub> = 25°C (Unless Otherwise Specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	-0.1	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	0.049	Ω	V <sub>GS</sub> = -12V, I <sub>D2</sub> = -30A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2.0	—	-4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -1.0mA
G <sub>fs</sub>	Forward Transconductance	24	—	—	S	V <sub>DS</sub> = -15V, I <sub>D2</sub> = -30A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	-10	μA	V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V
		—	—	-25		V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	-100	nA	V <sub>GS</sub> = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V <sub>GS</sub> = 20V
Q <sub>G</sub>	Total Gate Charge	—	—	170	nC	I <sub>D1</sub> = -47A
Q <sub>GS</sub>	Gate-to-Source Charge	—	—	65		V <sub>DS</sub> = -50V
Q <sub>GD</sub>	Gate-to-Drain ('Miller') Charge	—	—	30		V <sub>GS</sub> = -12V
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	30	ns	V <sub>DD</sub> = -50V
t <sub>r</sub>	Rise Time	—	—	100		I <sub>D1</sub> = -47A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	100		R <sub>G</sub> = 2.35Ω
t <sub>f</sub>	Fall Time	—	—	120		V <sub>GS</sub> = -12V
L <sub>s</sub> + L <sub>D</sub>	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C <sub>iss</sub>	Input Capacitance	—	6240	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	1570	—		V <sub>DS</sub> = -25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	115	—		f = 1.0MHz

**Source-Drain Diode Ratings and Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-47	A	
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	-188		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-5.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = -47A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	230	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = -47A, V <sub>DD</sub> ≤ -50V
Q <sub>rr</sub>	Reverse Recovery Charge	—	—	1.6	μC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>s</sub> +L <sub>D</sub> )				

**Thermal Resistance**

Symbol	Parameter	Min.	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	—	0.50	°C/W
R <sub>θPCB</sub>	Junction-to-PC Board (soldered to 1 inch square cu clad board)	—	1.6	—	

**Footnotes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V<sub>DD</sub> = -50V, starting T<sub>J</sub> = 25°C, L = 0.36mH, Peak I<sub>L</sub> = -47A, V<sub>GS</sub> = -12V
- ③ I<sub>SD</sub> ≤ -47A, di/dt ≤ -450A/μs, V<sub>DD</sub> ≤ -100V, T<sub>J</sub> ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ Total Dose Irradiation with V<sub>GS</sub> Bias. -12 volt V<sub>GS</sub> applied and V<sub>DS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V<sub>DS</sub> Bias. -80 volt V<sub>DS</sub> applied and V<sub>GS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

## Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

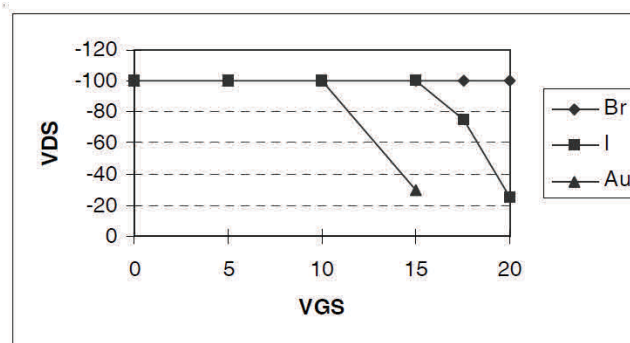
Symbol	Parameter	100 kRads (Si) <sup>1</sup>		300 kRads (Si) <sup>2</sup>		Units	Test Conditions
		Min.	Max.	Min.	Max.		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-100	—	-100	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -1.0mA
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2.0	-4.0	-2.0	-5.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -1.0mA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	V <sub>GS</sub> = -20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	100	—	100	nA	V <sub>GS</sub> = 20V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	-10	—	-10	μA	V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.05	—	0.05	Ω	V <sub>GS</sub> = -12V, I <sub>D2</sub> = -30A
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (SMD-2)	—	0.049	—	0.049	Ω	V <sub>GS</sub> = -12V, I <sub>D2</sub> = -30A
V <sub>SD</sub>	Diode Forward Voltage	—	-5.0	—	-5.0	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -47A

1. Part number IRHNA597160 (JANSR2N7550U2)
2. Part numbers IRHNA593160 (JANSF2N7550U2)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

**Table 2. Typical Single Event Effect Safe Operating Area**

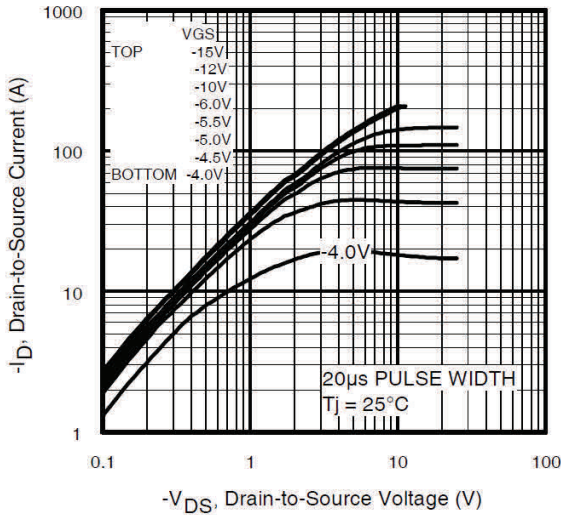
Ion	LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)					
				@VGS= 0V	@VGS= 5V	@VGS= 10V	@VGS= 15V	@VGS= 17.5V	@VGS= 20V
Br	37.9	252.6	33.1	-100	-100	-100	-100	-100	-100
I	59.7	314	30.5	-100	-100	-100	-100	-75	-25
Au	82.3	350	28.4	-100	-100	-100	-30	—	—



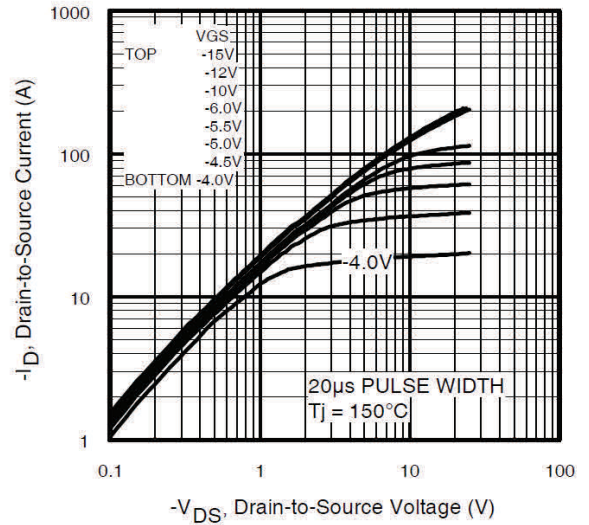
**Fig a.** Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

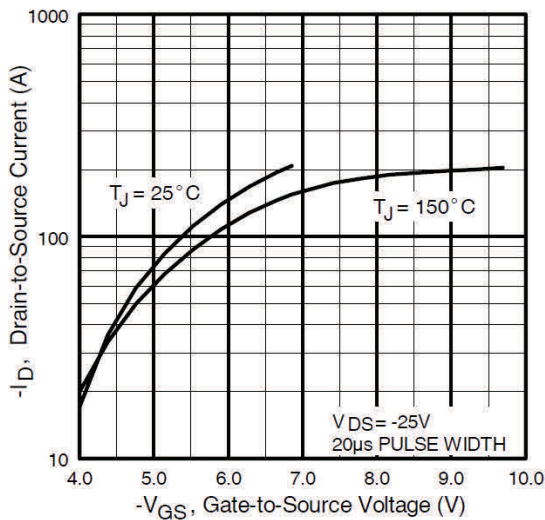
**Pre-Irradiation**



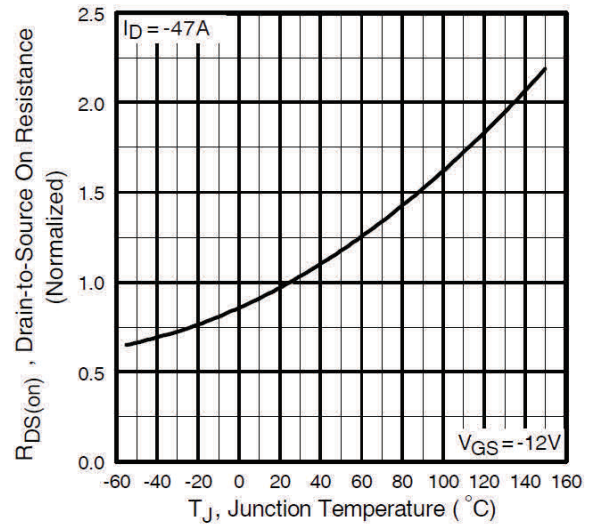
**Fig 1.** Typical Output Characteristics



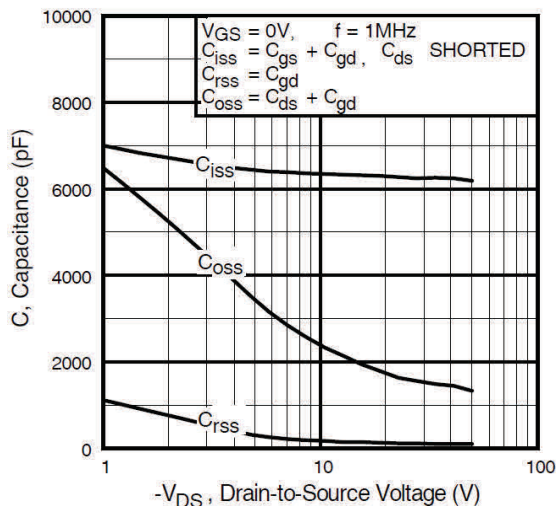
**Fig 2.** Typical Output Characteristics



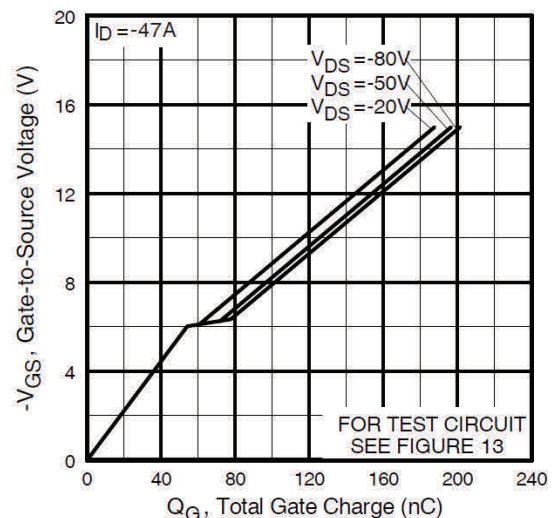
**Fig 3.** Typical Transfer Characteristics



**Fig 4.** Normalized On-Resistance Vs. Temperature

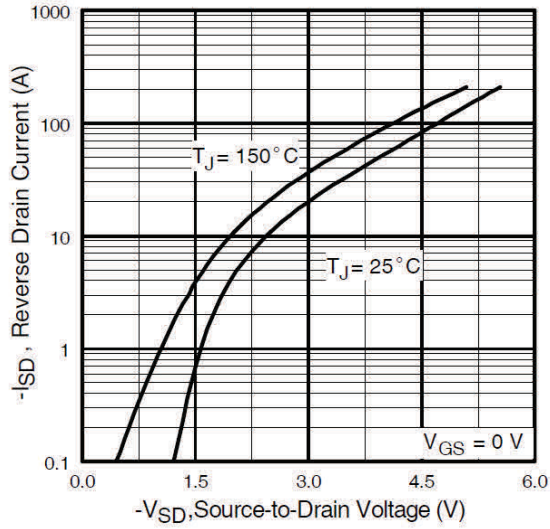


**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

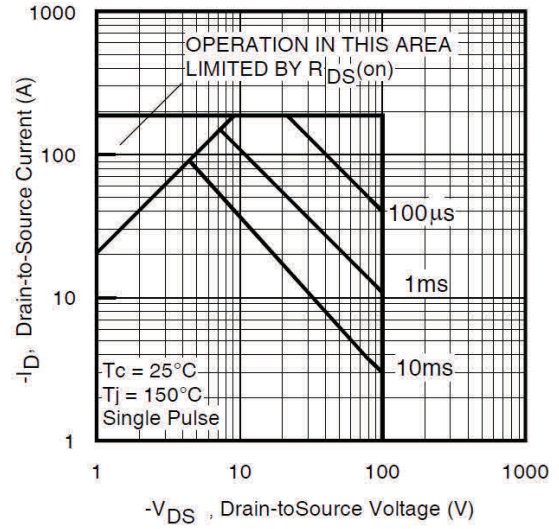


**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

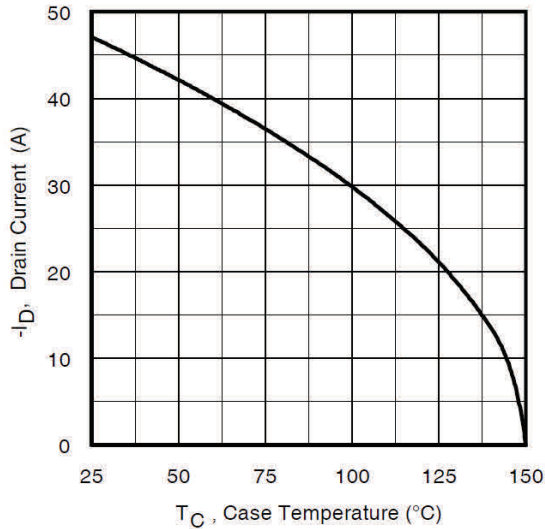
**Pre-Irradiation**



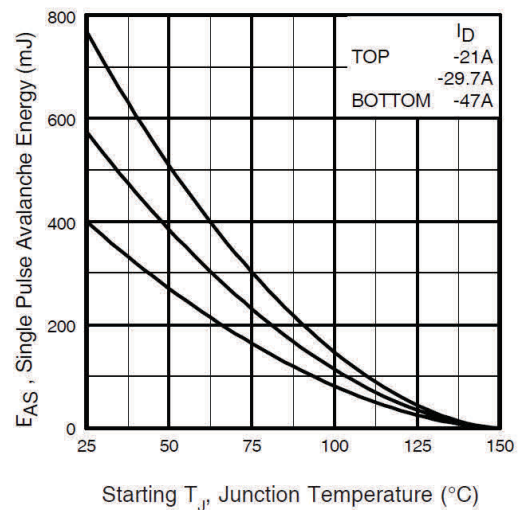
**Fig 7.** Typical Source-Drain Diode Forward Voltage



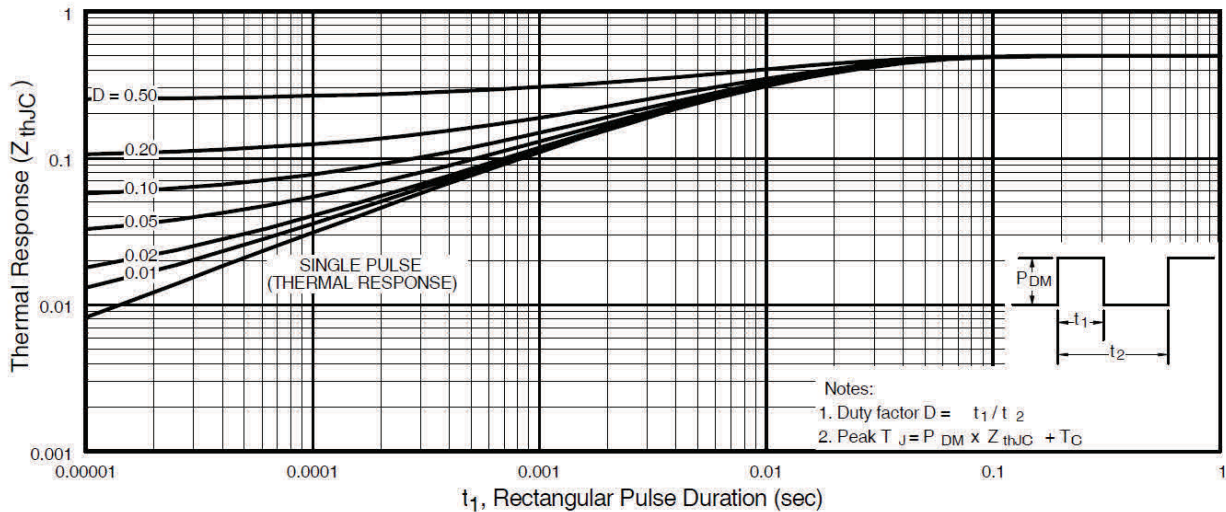
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current Vs. Case Temperature

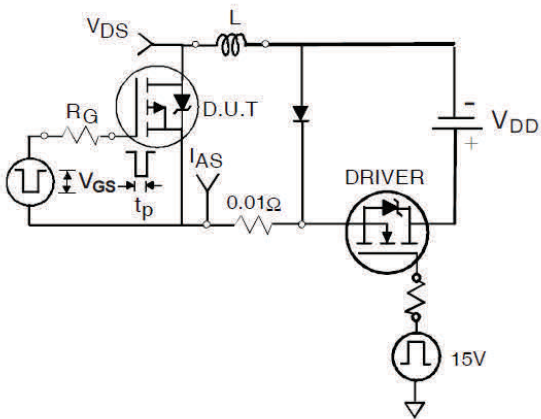


**Fig 10.** Maximum Avalanche Energy Vs. Drain Current

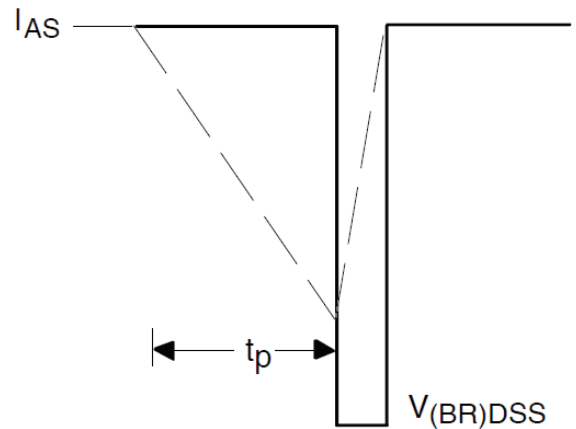


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

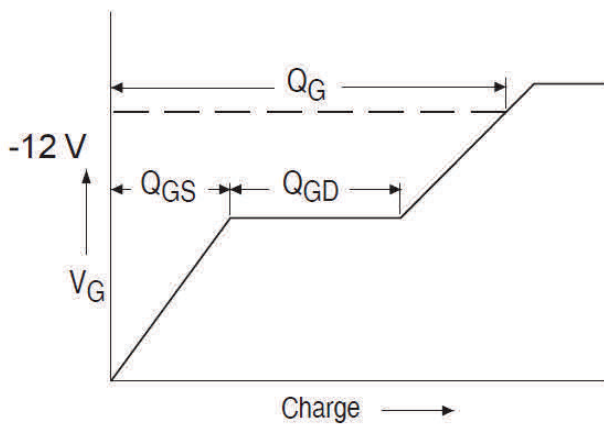




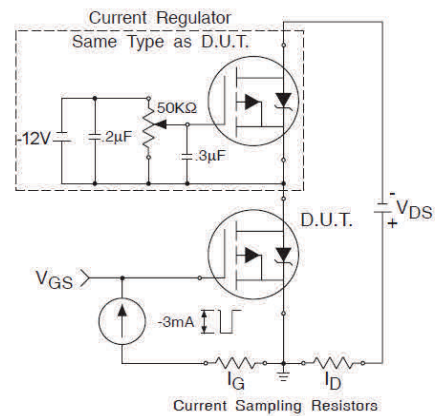
**Fig 12a.** Unclamped Inductive Test Circuit



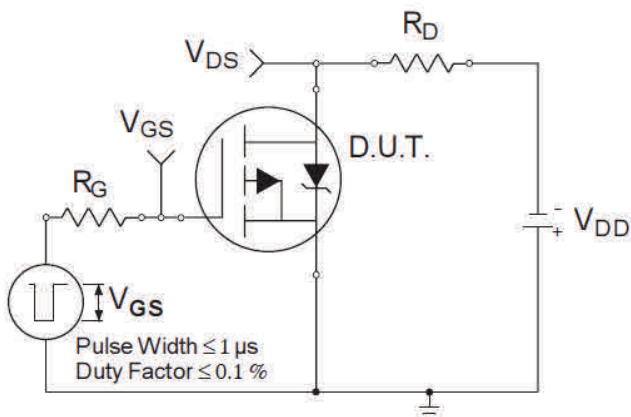
**Fig 12b.** Unclamped Inductive Waveforms



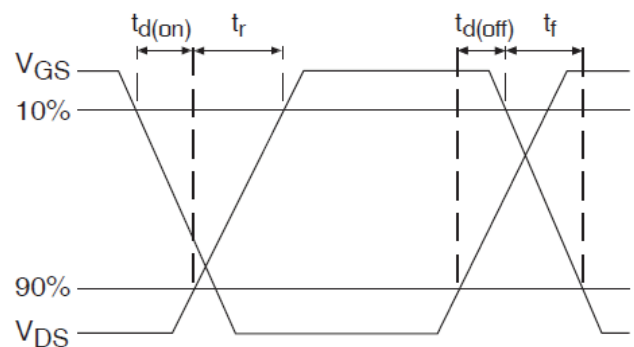
**Fig 13a.** Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

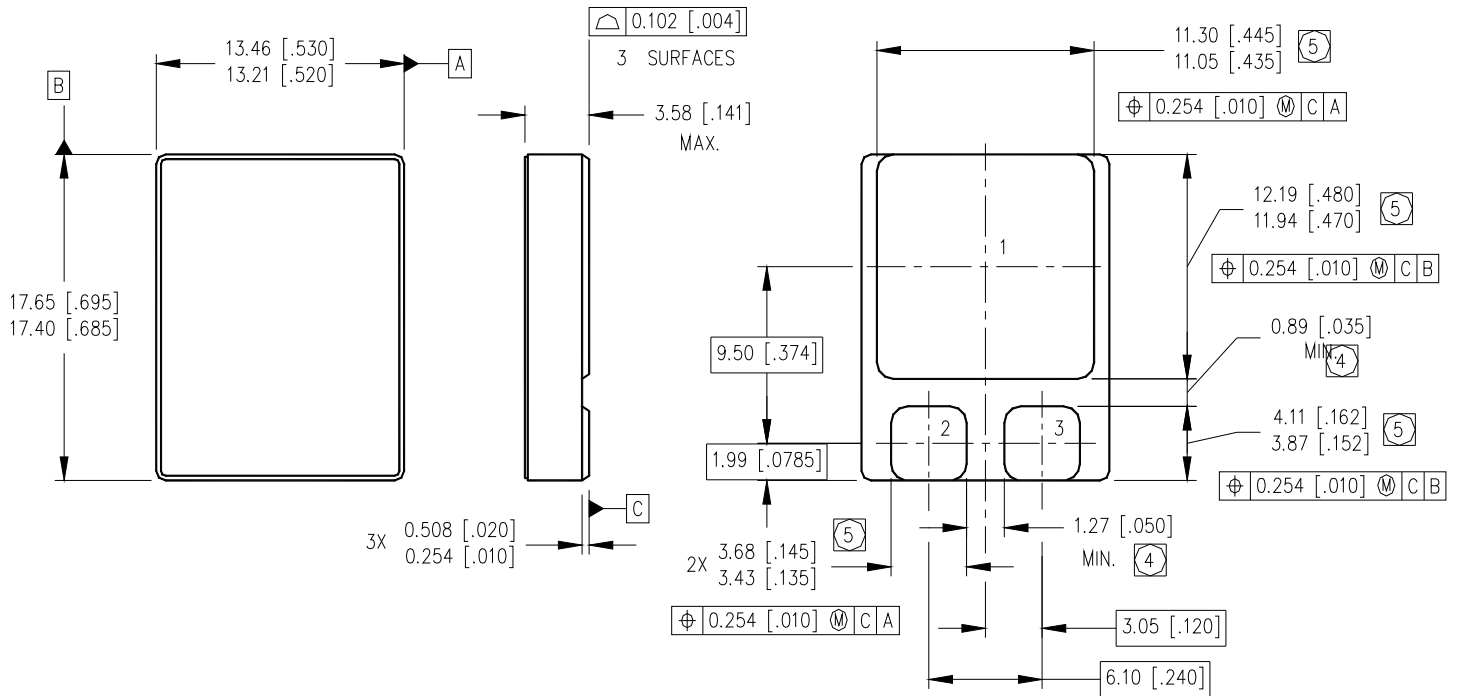


**Fig 14a.** Switching Time Test Circuit



**Fig 14b.** Switching Time Waveforms

**Case Outline and Dimensions — SMD-2**



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

- ④ DIMENSION INCLUDES METALLIZATION FLASH.
- ⑤ DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

MOSFET

- 1 = DRAIN
- 2 = GATE
- 3 = SOURCE

### **IMPORTANT NOTICE**

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