

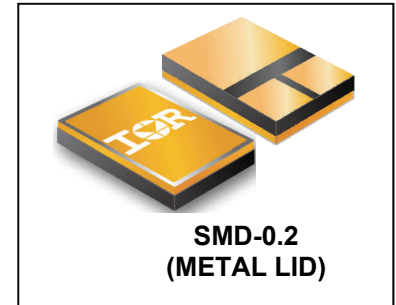
**RADIATION HARDENED
POWER MOSFET
SURFACE MOUNT (SMD-0.2)**

**250V, N-CHANNEL
R5 TECHNOLOGY**

Product Summary

Part Number	Radiation Level	RDS(on)	I _D
IRHNM57214SE	100 kRads(Si)	1.7Ω	2.4A

Refer to page 9 for additional part number -
IRHNMC57214SE (Ceramic Lid)



Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm²)). The combination of low R_{DS(on)} and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Low R_{DS(on)}
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight
- ESD Rating: Class 1B per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I _{D1} @ V _{GS} = 12V, T _C = 25°C	Continuous Drain Current	3.7	A
I _{D2} @ V _{GS} = 12V, T _C = 100°C	Continuous Drain Current	2.4	
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	14.8	
P _D @ T _C = 25°C	Maximum Power Dissipation	40	W
	Linear Derating Factor	0.32	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy ②	34	mJ
I _{AR}	Avalanche Current ①	3.7	A
E _{AR}	Repetitive Avalanche Energy ①	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.7	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	0.25 (Typical)	

For Footnotes refer to the page 2.

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.27	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	1.7	Ω	V _{GS} = 12V, I _{D2} = 2.4A ④
V _{GS(th)}	Gate Threshold Voltage	2.5	—	4.5	V	V _{DS} = V _{GS} , I _D = 1.0mA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-9.1	—	mV/°C	
G _{fs}	Forward Transconductance	2.0	—	—	S	V _{DS} = 15V, I _{D2} = 2.4A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	V _{DS} = 200V, V _{GS} = 0V
		—	—	25		V _{DS} = 200V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _G	Total Gate Charge	—	—	9.1	nC	I _{D1} = 3.7A
Q _{GS}	Gate-to-Source Charge	—	—	2.9		V _{DS} = 125V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	4.3		V _{GS} = 12V
t _{d(on)}	Turn-On Delay Time	—	—	6.3	ns	V _{DD} = 125V
t _r	Rise Time	—	—	6.3		I _{D1} = 3.7A
t _{d(off)}	Turn-Off Delay Time	—	—	16.8		R _G = 7.5Ω
t _f	Fall Time	—	—	14		V _{GS} = 12V
L _S + L _D	Total Inductance	—	6.8	—	nH	Measured from the center of drain pad to center of source pad
C _{iSS}	Input Capacitance	—	308	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	51	—		V _{DS} = 25V
C _{rSS}	Reverse Transfer Capacitance	—	1.2	—		f = 1.0MHz
R _G	Gate Resistance	—	6.6	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	3.7	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	14.8		
V _{SD}	Diode Forward Voltage	—	—	1.0	V	T _J = 25°C, I _S = 3.7A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	145	ns	T _J = 25°C, I _F = 3.7A, V _{DD} ≤ 25V
Q _{rr}	Reverse Recovery Charge	—	—	857	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	3.12	°C/W

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = 50V, starting T_J = 25°C, L = 5.0mH, Peak I_L = 3.7A, V_{GS} = 12V
- ③ I_{SD} ≤ 3.7A, di/dt ≤ 1018A/μs, V_{DD} ≤ 250V, T_J ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ Total Dose Irradiation with V_{GS} Bias. 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V_{DS} Bias. 200 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 100 kRads (Si) ²		Units	Test Conditions
		Min.	Max.		
BV _{DSS}	Drain-to-Source Breakdown Voltage	250	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.5	V	V _{DS} = V _{GS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100	nA	V _{GS} = -20V
I _{DSS}	Zero Gate Voltage Drain Current	—	10	μA	V _{DS} = 200V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	1.7	Ω	V _{GS} = 12V, I _{D2} = 2.4A
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (SMD-0.2)	—	1.7	Ω	V _{GS} = 12V, I _{D2} = 2.4A
V _{SD}	Diode Forward Voltage ④	—	1.0	V	V _{GS} = 0V, I _S = 3.7A

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	V _{DS} (V)				
				@V _{GS} =0V	@V _{GS} =-5V	@V _{GS} =-10V	@V _{GS} =-15V	@V _{GS} =-20V
Br	36.7	309	39.5	250	250	250	250	250
I	59.8	341	32.5	250	250	250	250	240
Au	82.3	350	28.4	250	250	225	175	50

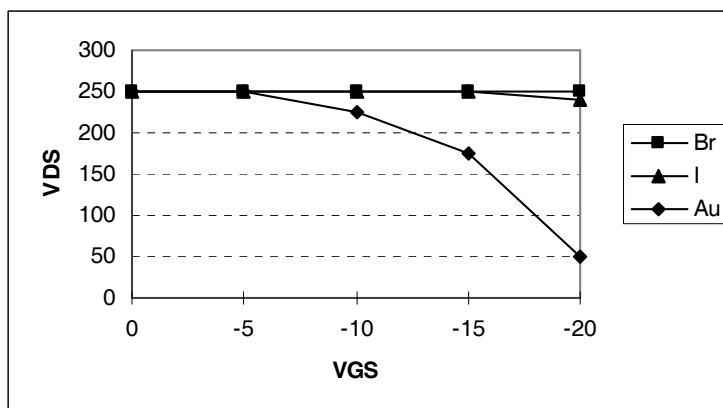


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

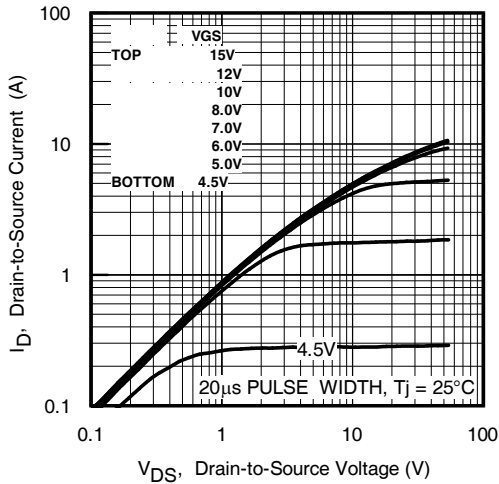


Fig 1. Typical Output Characteristics

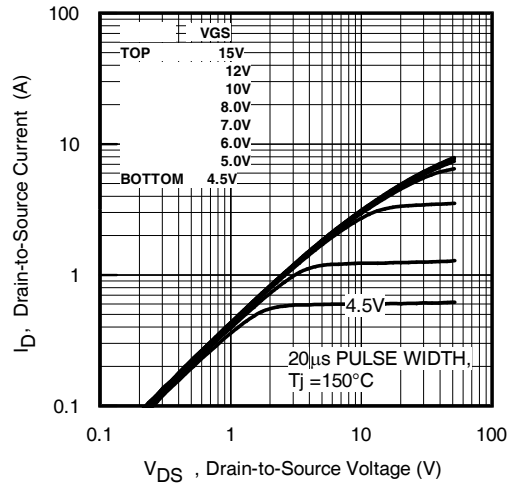


Fig 2. Typical Output Characteristics

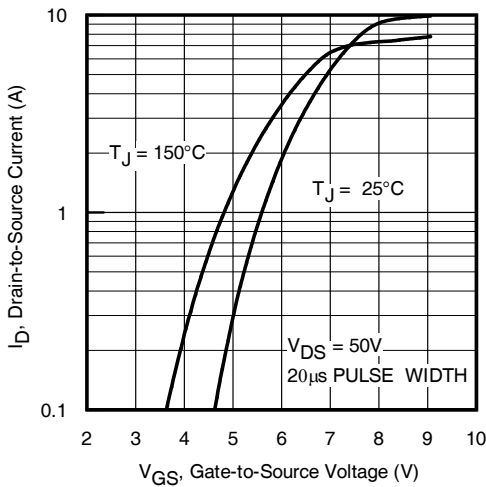


Fig 3. Typical Transfer Characteristics

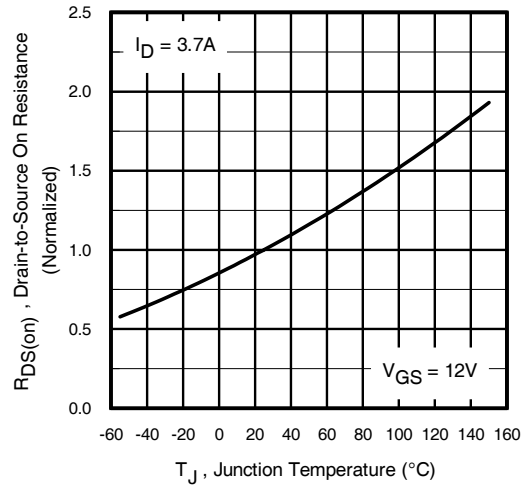


Fig 4. Normalized On-Resistance Vs. Temperature

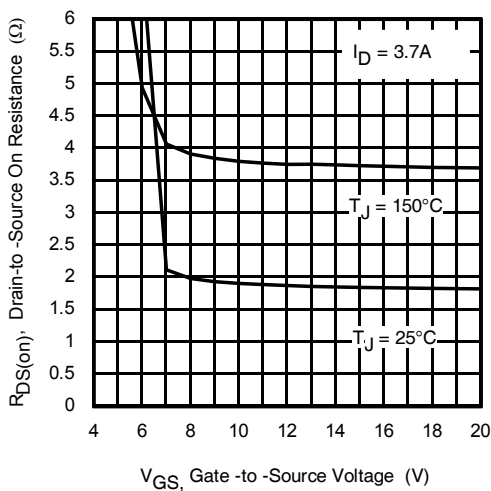


Fig 5. Typical On-Resistance Vs Gate Voltage

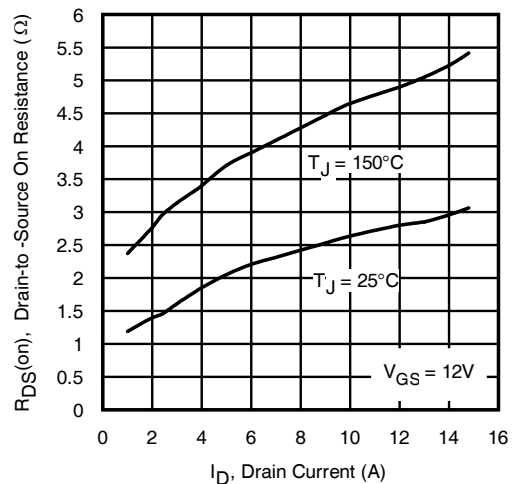


Fig 6. Typical On-Resistance Vs Drain Current

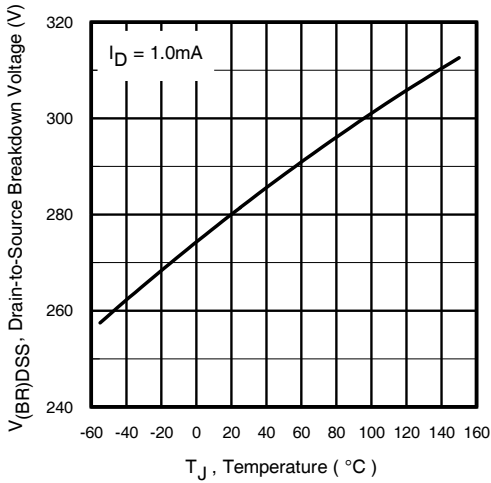


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

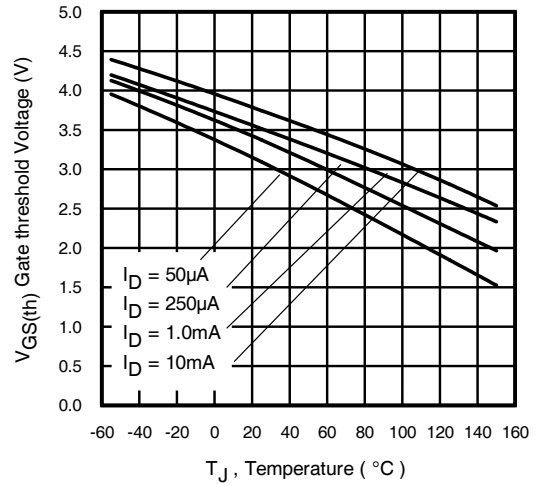


Fig 8. Typical Threshold Voltage Vs Temperature

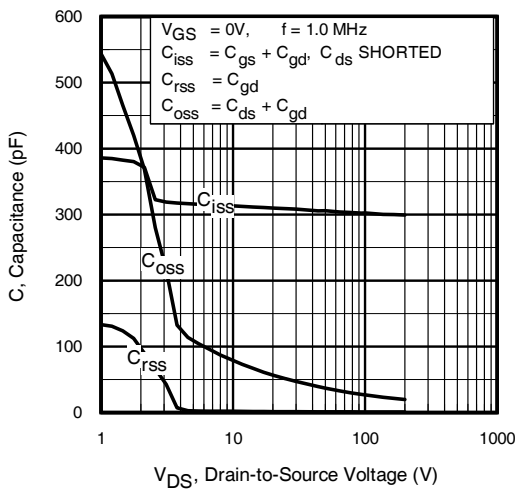


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

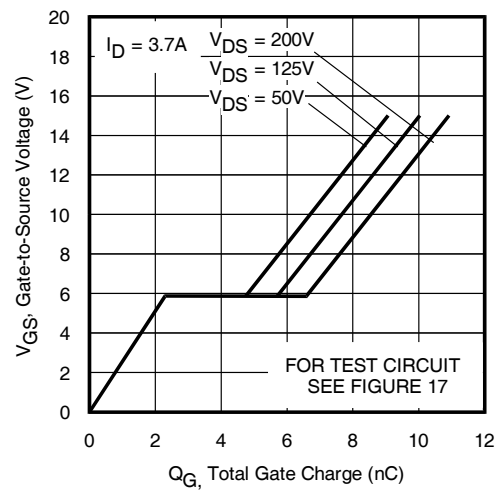


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

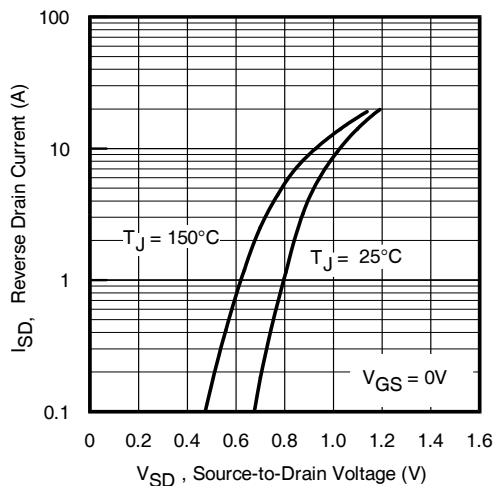


Fig 11. Typical Source-Drain Diode Forward Voltage

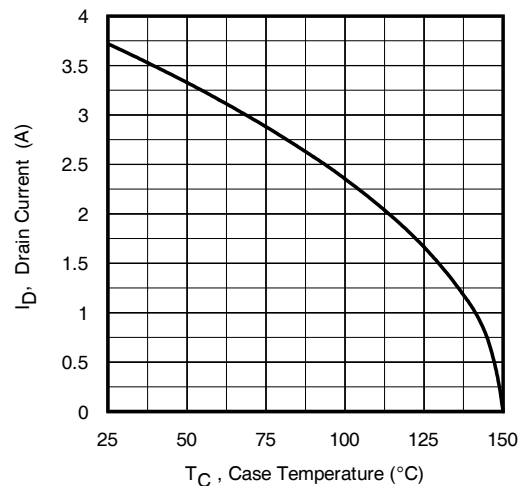


Fig 12. Maximum Drain Current Vs. Case Temperature

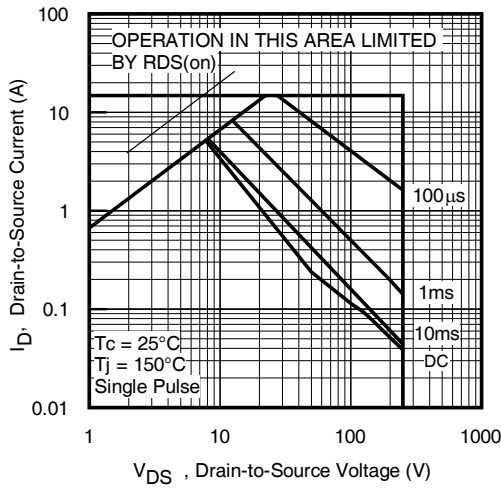


Fig 13. Maximum Safe Operating Area

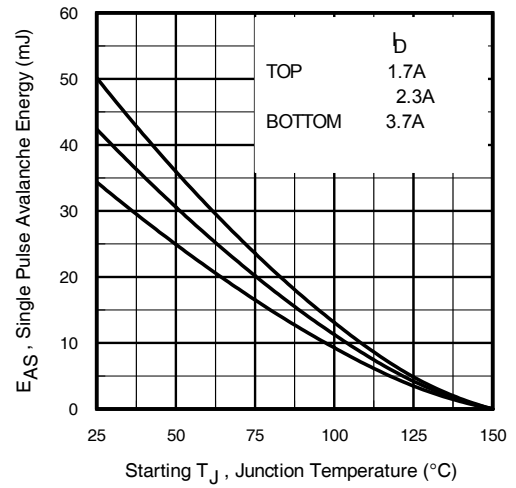


Fig 14. Maximum Avalanche Energy Vs. Drain Current

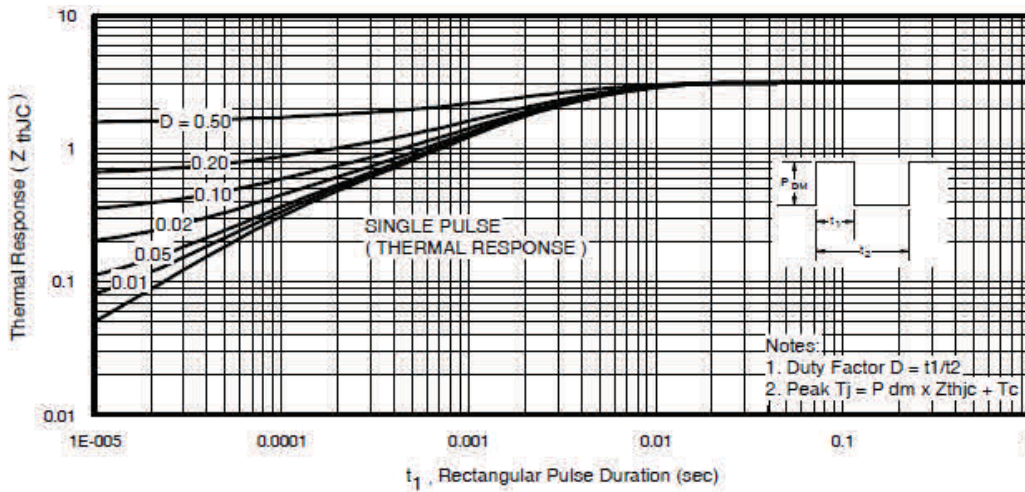


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

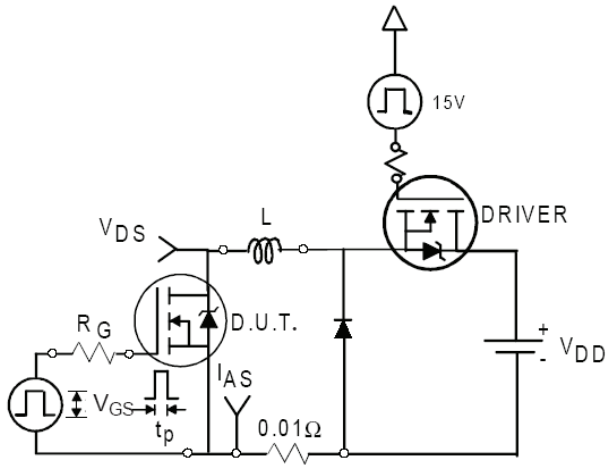


Fig 16a. Unclamped Inductive Test Circuit

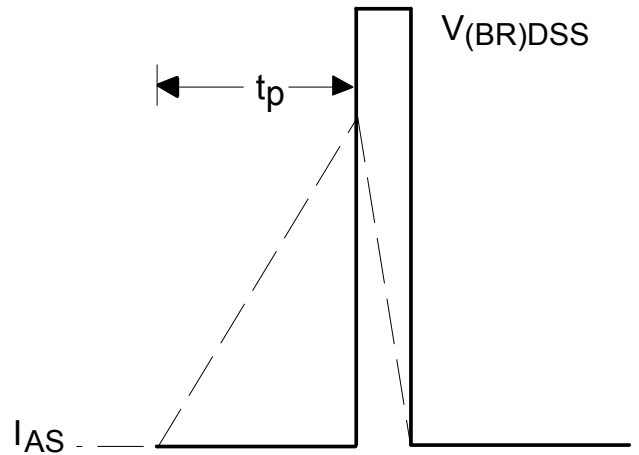


Fig 16b. Unclamped Inductive Waveforms

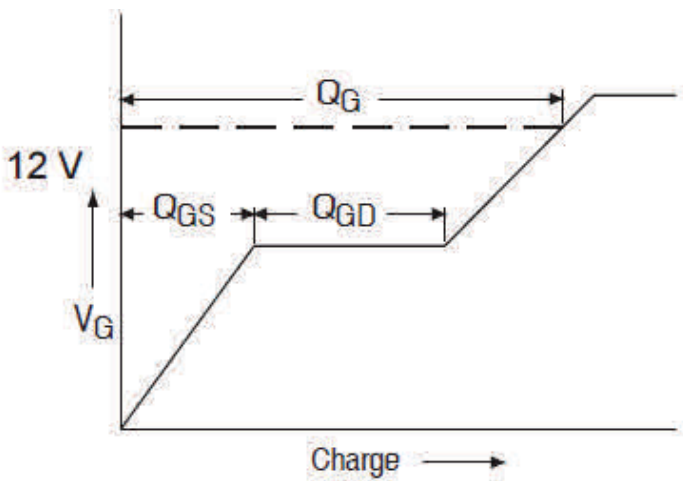


Fig 17a. Basic Gate Charge Waveform

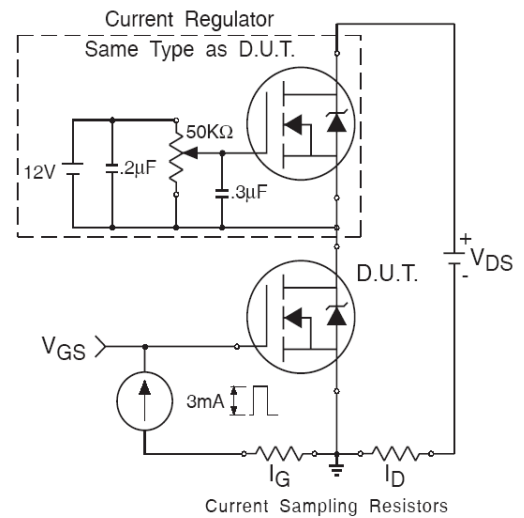


Fig 17b. Gate Charge Test Circuit

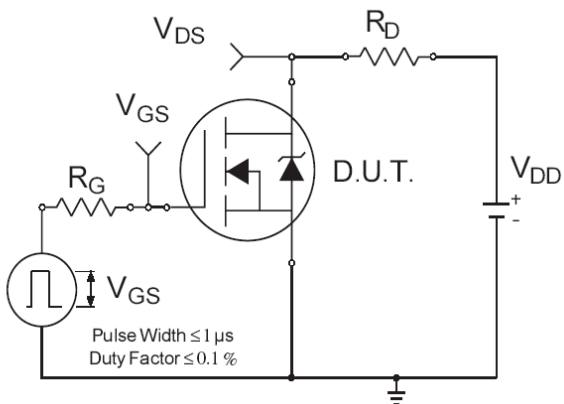


Fig 18a. Switching Time Test Circuit

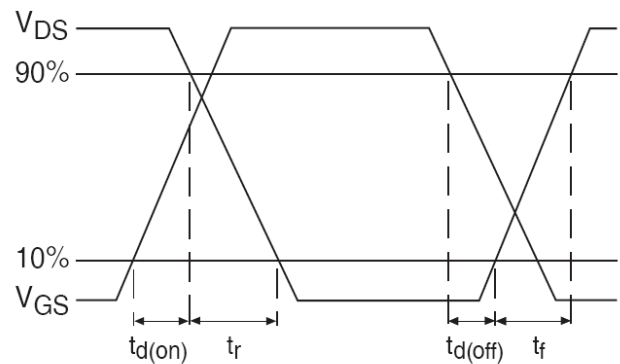
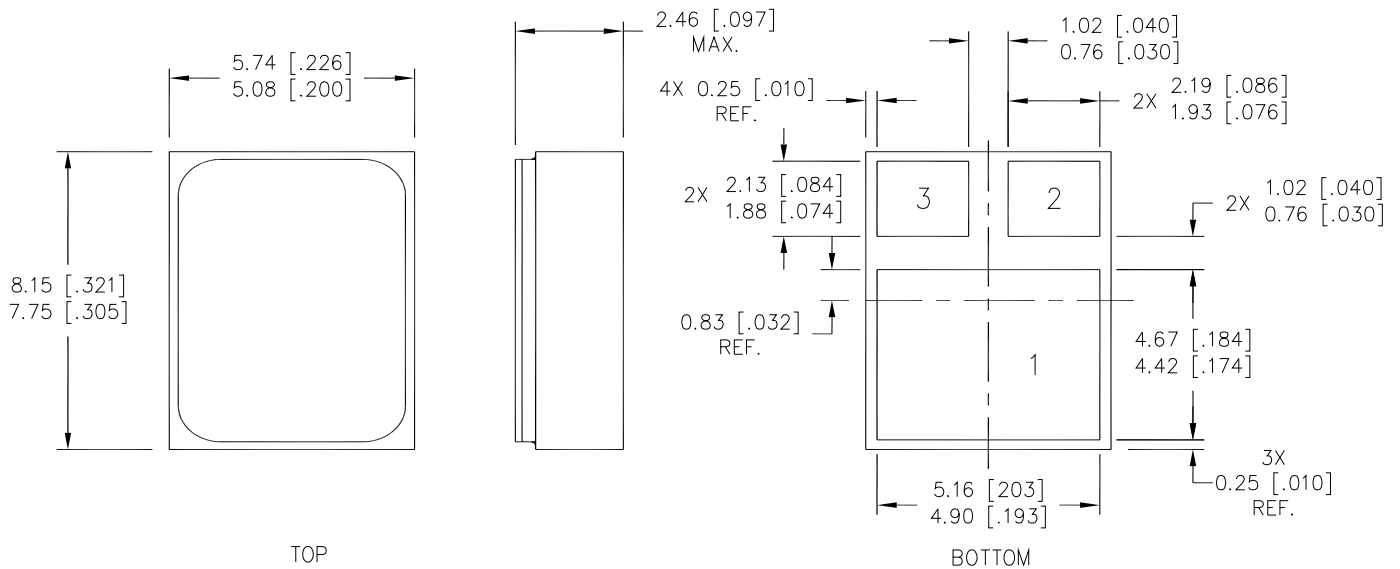


Fig 18b. Switching Time Waveforms

Case Outline and Dimensions - SMD-0.2 (Metal Lid)



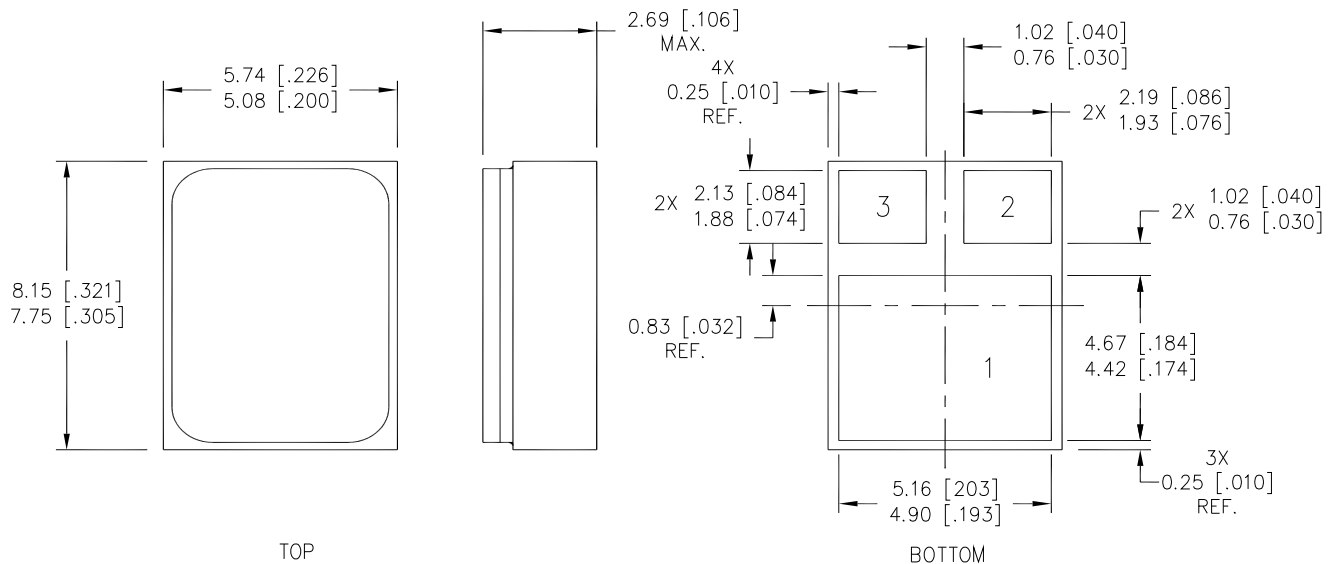
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].

PAD ASSIGNMENTS

- 1 = DRAIN
- 2 = GATE
- 3 = SOURCE

Case Outline and Dimensions - SMD-0.2 (Ceramic Lid)



NOTES:


1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

PAD ASSIGNMENTS

- 1 = DRAIN
- 2 = GATE
- 3 = SOURCE

Additional Product Summary (continued from pages 1 and 3)

Product Summary

Part Number	Radiation Level	RDS(on)	I _D	 <p>SMD-0.2 (CERAMIC LID)</p>
IRHNMC57214SE	100 kRads(Si)	1.7Ω	2.4A	

IMPORTANT NOTICE

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